Testing Flash Memories for Tunnel Oxide Defects

Mohammad Gh. Mohammad
Computer Engineering Department
Kuwait University
P.O. Box 5969, Safat, 13060, Kuwait
Email: mohammad@eng.kuniv.edu.kw

Kewal K. Saluja
Electrical and Computer Engineering Department
University of Wisconsin
Madison, Wisconsin, USA
Email: saluja@ece.wisc.edu

***Abstract*— Testing non volatile memories for tunnel oxide defects is one of the most important aspects to guarantee cell reliability. Defective tunnel oxide layer in core memory cells can result in various disturb faults. In this paper, we study various defects in the insulating layers of a 1T flash cell and analyze their impact on cell performance. Further, we present a test methodology and test algorithms that enable the detection of tunnel oxide defects in an efficient manner.**

I. Introduction

Non volatile memories (NVM) in general and flash memories in particular are becoming the number one memory of choice in applications ranging from cell phones to complex systems such as System-on-Chip (SOC). The market share of flash memory is expected to double in the next few years to reach 20 billion dollars. One of the main reasons for this explosive growth is the low cost of flash memories. However, one of the major concerns in manufacturing such memories is the cost of test. With every new generation, the cost of test is increasing due to the introduction of new failure mode(s) which must be considered to properly test such memories. In today's semiconductor manufacturing, more than 30% of final product cost is due to test requirements [1]. Hence, methods to reduce the test cost are likely to be key factors in the continued growth of flash memories and to maintain its competitiveness in the semiconductor memory market.

Since the introduction of flash memories, substantial research has been directed towards the development of efficient tests [2], [3], [4]. In [2] the authors proposed a logical fault model to model various disturb faults and developed efficient tests for their detection. The authors of [3], [4] expanded the modeled faults to include some traditional faults that are present in other type of memories as well as disturb faults that are described by the IEEE Standard Definitions and Characterization of Floating Gate Semiconductor Arrays [5]. In [3], Built-in Self-Test for flash memories was proposed to reduce the cost of testing. In all these papers, special attention was paid to develop efficient test algorithms in detecting all known faults applicable to flash memories.

In this paper, we analyze various defects at different locations in the core memory cell that are responsible for disturb faults and study their impact on cell performance using a 2D device simulator named Atlas [6]. After analyzing the behavior of the defective cells, we determine fault excitation conditions that allow fast and reliable identification of faulty cells. Using these excitation conditions, efficient tests for testing NOR type flash memories are developed.

In section II of this paper we review the previously developed models for flash memory faults. Section III discusses the experimental setup for defect injection and the study of their impact. Findings of simulation studies are provided in section IV. Test algorithms and their detection capabilities are discussed in section V. Section VI concludes the paper.

II. Flash Memory Program Disturb Fault Models

Semiconductor memories, including all forms of NVMs such as flash memories, suffer from defects that could occur during the manufacturing process. The characteristics of the defects, whether large or small, can alter the correct behavior of the memory cells. However, the manifestation and detection of these defects depends on their physical characteristics. For example, when a defect is large and it results in a short/open between a line and the power supply (V_{cc}) or ground (GND), then it can manifest itself as a stuck-at (SAF) fault [7]. Alternatively, if the short is between two lines and neither of the lines is V_{cc} or GND, then such a short may result in a coupling fault (CF) or address decoder fault (AF) depending on which two memory lines are shorted together. In other instances, the defects may be too small to result into shorts or opens and may manifest as resistive defects which result in more complex faulty behavior, such as Incorrect-Read-Fault (IRF) or Write-Disturb-Fault (WDF) [8], [9]. Even though tests to detect these faults exist, they can be expensive in terms of test time unless careful attention is paid to the derivation of such tests.

In NVMs, particularly in flash memory literature, the faults are classified into two major categories. The first category consists of those faults that are common between flash and all other type of semiconductor memories such as DRAMs and SRAMs. These faults include SAF, SOF, AF, and CF_{st} (state-coupling) faults [3], [4]. The second category consists of faults that are specific only to NVMs, including flash memories, and do not conform to the traditional faults known to occur in other types of volatile memories such as DRAMs. These faults are known as disturb faults and can be classified as either program or read disturbs [10], [11], [12]. A disturb fault is caused by defects in the insulating layer of a core memory element or it may be induced by electric stress conditions during the different modes of operations.

1063-9667/08 $25.00 © 2008 IEEE
DOI 10.1109/VLSI.2008.41

IEEE computer society

The most common memory cell used in today's flash memories is the 1T floating gate transistor (FG). The structure of the 1T transistor is similar to the traditional MOS transistor with an additional floating polysilicon gate that is completely insulated by dielectric from all other conducting terminals. The floating gate is insulated from the substrate by a layer of high quality oxide, called tunnel oxide, whereas it is insulated from the top by a oxide-nitride-oxide (ONO) layer, an interpoly insulator [13]. The logical state of the memory cell is represented by the charge on the floating gate. When there is no charge present on the floating gate, the cell is referred to as erased or containing a logic "1" value. On the other hand, when the floating gate has a negative charge, it is referred to as programmed or having a logic "0" value.

1T flash cells are organized in an array to constitute a memory module. The most common array organizations for flash memories are NOR and NAND array organizations. The NOR array organization is shown in Figure 1. In NOR array organization, Channel Hot Electron Injection (CHEI) mechanism is used to accumulate charge on the floating gate whereas FN-tunneling is used to extract the charge, thus erasing the cell [13]. When accumulating or extracting charge of the floating gate, higher than normal voltages are applied on the various terminals of the memory cell to create high electric field across the tunnel oxide to enable the transfer of charge. These high fields that are used to program and erase the cell pose reliability concerns as well. Due to the way the memory cells are organized in a typical memory array, many of the unselected cells experience the same high electric fields as the selected cell(s). For example, when addressing a cell (i,j), where "i" is the row address and "j" is the column address of a cell, all cells on row *i* will experience the voltage applied on that row. Similarly, all cells in column *j* (whether selected or not) will experience the voltage on that column.

Designers are aware of these high fields and they realize that these could result in disturb behavior. As a result, they consider these effects during memory device characterization and they design operating voltages, array organization, and the cell structure to meet the targeted design specifications and minimize the effect of disturbs [13]. But, some of the issues still remain. For example, the quality of the tunnel oxide must be flawless and the manufacturing process must be nearly perfect to ensure the reliability of the memory cell. However, due to the nature of the manufacturing process, contaminants and other anomalies are unavoidable. When these contaminants or defects are located in the insulating layers of the 1T cell, they pose a reliability concern and amplify the unwanted behavior of disturbs. The *IEEE Standard Definitions and Characterization of Floating Gate Semiconductor Arrays* defines nearly all disturbs for all possible memory array organizations and cell structures [5]. In a set of recent papers [2], [3], [4], [14] the most common disturb behaviors were modeled as logical faults. The following is a short description of four most common program disturbs as well as their fault models for NOR type flash memories. Other disturbs which are not very common or which are applicable to other memory array

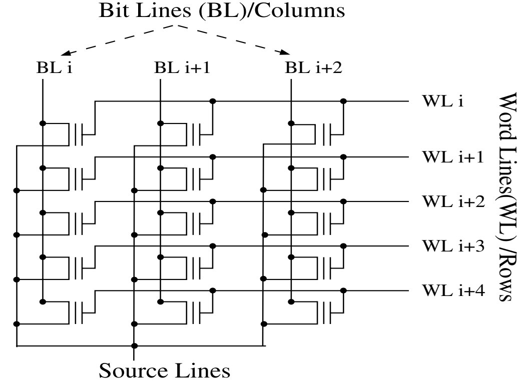

Fig. 1. NOR Array Organization

organizations can be found in [5], [14]. The description below uses the notation $<S_a;S_v/F/R>$ which is commonly used in representing static coupling faults [15]. In this notation: $S_a \in \{$ w0,w1,r0,r1$\}$, is the *sensitizing operation sequence* (SOS) consisting of read/write operations on the state of the aggressor cell, S_v is a SOS for the state on the victim (before fault excitation) cell, "F" $\in \{0,1\}$ is the state of the faulty cell (after excitation), and R $\in \{0,1,-\}$ is the output of the read operation. The value "-" in field R is used in case of write operation.

Word-line erase disturb (WED)
: exists when a cell being programmed (selected cell) causes another unprogrammed cell (unselected cell), sharing the same word-line, to be erased. This fault is modeled as <1w0;0/1/-> fault.

Word-line program disturb (WPD)
: occurs when a cell being programmed causes another unprogrammed cell, sharing the same word-line, to be programmed and is modeled as <1w0;1/0/->.

Bit-line erase disturb (BED)
: which is modeled as <1w0;0/1/-> fault takes place when a cell being programmed causes another unprogrammed cell, sharing the same bit-line, to be erased.

Bit-line program disturb (BPD)
: arises when a cell being programmed causes another unprogrammed cell, sharing the same bit-line, to be programmed <1w0;1/0/->.

Low electric field stresses, such as read disturbs, are also caused by the physical defects in the insulating layer. Thus by identifying defects that cause program disturb faults, we can also detect read disturb faults.

III. 2-D Device Simulation Setup

Two different 2D device simulation tools, namely Athena and Atlas [6], [16], were used to investigate the various defects in 1T cell. Using Athena, we constructed a fault-free $1\mu \times 1\mu$ 1T structure with a tunnel oxide of Å105 and combined ONO stack thickness of Å400. The cell is designed to be programmed by the CHEI using a 1μs pulse

and erased using FN-tunneling with 10ms erase pulse. The bias conditions required to accomplish these operations and the resulting threshold voltages (V_t) are shown in Table I. In this table, labels CG, D, S, and B represent the voltages applied at control gate, drain, source, and base terminals of the memory cell respectively (values given in volts (V)). The erase operation described in Table I is the most common approach used for erasure and is known as *negative gate erase* (NGE). This technique results in lower power consumption as well as better cell reliability [13], [17] when compared to *source side erase* technique which uses high voltage on the source terminal while grounding the control gate of the cell. The

TABLE I
PROGRAM/ERASE BIASES AND THRESHOLD VOLTAGES

Operation	CG	D	S	B	V_t
Program	10	6	GND	GND	7.95
Erase	-8	Floating	7	GND	1.11
Read	3.3	0.5	GND	GND	

number of cells in each row/column in the array organization define the worst case gate/drain stress that a cell can undergo. The duration of the worst case stress can be calculated by multiplying the program time with the number of cells in a row/column (i.e. T_{stress}= $T_P\times$ (N-1)), where T_P and N are program time and number of cells in a row/column respectively (for an NxN array organization) [18]. Common stress time found in today's flash memories varies from 0.1ms-2ms depending on the program time and array organization used. In our experiments, we assume a memory array organized as a 128 x 128 grid. This implies that the duration of the worst case gate/drain stress (for a cell) in such an array is 127μs for a program time of 1μs.

Defect injection was accomplished by injecting a defect in a particular region of the memory cell while maintaining the same processing steps as the fault-free cell. The locations of the defects were limited to the various oxide layers in the structure, namely the tunnel oxide or oxide layers in ONO stack. Five different locations were identified for possible defect injection and corresponding defective devices were created. Thus each defective device had one injected defect in the structure, and these are shown in Figure 2. Defects in the tunnel oxide are located in the oxide area above the diffusion region of the 1T structure (i.e. drain/source overlap) or in the channel region. The ONO layer defects were limited to the bottom (ONO_B) or top (ONO_T) oxide layers.

The defects were characterized by specifying the effective oxide thickness at the defect site. Thus, if the fault free value of the tunnel oxide thickness was Å106, a defect will result in an oxide thickness smaller than this value. For example, a *Å 100 defect* results into effective oxide thickness of Å100 instead of the design value of Å106. All remaining characteristics of the defect size, such as "x" (length) and "z" (along the width of transistor), are kept constant. A total of 11 defective devices were created for simulation as shown in table II. Two studies were carried out on defective cells. The first study was to

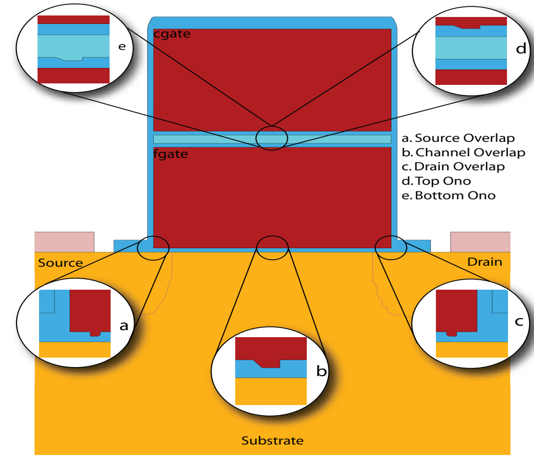

Fig. 2. Defects and Their Locations

determine the impact of the shape of the defects on the cell performance to identify characteristics of killer defects. In the second study, killer defects were injected in different regions of the insulating layers of the 1T cell and their impact on cell operation during normal as well as stress modes were analyzed. The results of these are given below.

TABLE II
TUNNEL OXIDE OF VARIOUS DEFECTS

Defect location	Effective thickness (Å)
ONO_B	67
ONO_T	71
Drain Overlap	100, 80, 60
Source overlap	100, 80, 60
Channel	100, 80, 60

IV. RESULTS AND DISCUSSION

The simulation studies targeted three different objectives. 1) To identify the size of the defects that can adversely impact the reliability of the cell under any mode of operation (i.e. normal operation or stress conditions). 2) To assess the effectiveness of various stress tests on detecting defects. 3) To develop efficient test(s) that detect(s) all defects being investigated in this paper.

For each simulation study, the defect is first injected in the specified region (e.g. drain overlap), and then an operation is performed on the cell (e.g. gate stress). After that, the I-V characteristics are measured and the threshold voltage is extracted. The process is repeated for all combinations of different operations and defect locations.

A. Cell Performance of Cells With Defects

In order to analyze the effect of defect size on cell performance, defects of different shape/size (but of identical total volume) were simulated. Instead of conducting experiments for all defect locations, we inserted defects only in the drain overlap region to carry out these studies. The outcomes are

shown in Table III. In this table, the first column represents the operation performed and the remaining columns represent the resulting threshold voltages for three different defects (labeled by their effective tunnel oxide thickness) under various modes of operations. Moreover the rows labeled "Gate/Drain Stress$_E$" in the table represent cells that underwent a 127μs of stress when they were assumed to be initially erased cells. Rows labeled "Gate/Drain Stress$_P$" correspond to cells that underwent stress assuming they were initially programmed cells. Also, the erase operation in this study was performed using the commonly used NGE method. It is apparent from

TABLE III
DRAIN DEFECT SIZE CHARACTERIZATION

Operation \ Defect	Threshold Voltage (V)			
	Fault Free	**Å99**	**Å81**	**Å49**
Program	7.9581	6.3197	7.1271	6.4617
Erase	1.1066	0.36456	-1.9736	-8.0953
Gate Stress$_E$	1.1066	0.36456	-1.9736	-1.5950
Drain Stress$_E$	1.1066	0.36456	-1.9736	-1.7851
Gate Stress$_P$	7.9581	6.3197	7.1271	6.4617
Drain Stress$_P$	7.9577	6.3181	7.1026	3.7307

the table that the oxide thickness of the defect plays a major role in determining the performance (in this case threshold voltage) of the cell. In the case of Å81 and Å49 defects, the cells were depleted when they were erased, depicting the well known over-erase phenomenon [13], [19], [17]. Furthermore, the Å49 defect was the only defect that was identified as a detectable defect using the *Drain Stress$_P$* experiment. As for all other cells, no significant shift in the threshold voltage before and after stress experiment was noticed. In particular, the Å49 defect shifts the threshold voltage of the cell from a programmed V_t of 6.4 to 3.7, i.e. in excess of a 2 volts shift, whereas all other defects cause only a marginal and insignificant shift in the threshold voltage. Interestingly the 2 volts threshold shift does not result in value flip in the memory cell and hence it will not be detected using normal read operation. However, other techniques, such as margin reads [18], can detect such defects. The main conclusion of this set of experiments is that a defect which reduces the effective tunnel oxide thickness to Å80 or less represents a killer defect and such defects must be properly excited and detected.

B. Tunnel Oxide Defects

The second set of experiments was carried out on defective cells with effective tunnel oxide thickness (at defect site) to be Å80, and located in one of the various tunnel oxide regions as specified in section III. For all these cases, we used the NGE erase approach discussed in section III. The experiments were carried out on tunnel oxide defects in source/drain overlaps and in the channel regions. The cells were simulated to see the impact of each defect on the cell program/erase characteristics as well as their behavior under stress conditions. Table IV summarizes the findings. It is evident from this table that only the source overlap defect can potentially be identified in these experiments as explained below. For this defect, the erase

TABLE IV
NEGATIVE GATE ERASE EXPERIMENTS

Operation \ Defect	Threshold Voltage (V)			
	Fault Free	**Source**	**Drain**	**Channel**
Program	7.9581	7.9094	7.1271	7.9764
Erase	1.1195	-0.3050	1.1627	1.4534
Gate Stress$_E$	1.1195	-0.3050	1.1627	1.4534
Drain Stress$_E$	1.1195	-0.3050	1.1627	1.4534
Gate Stress$_P$	7.9581	7.9094	7.1271	7.9764
Drain Stress$_P$	7.9577	7.9091	7.1026	7.9761

operation resulted in a depleted cell (cell with negative V_t), causing a faulty cell behavior, whereas for all other defects, the threshold shift is only marginal. Thus in the case of source overlap defect, when reading a cell in the same column as the depleted cell, the read data will be corrupted if the addressed cell has a logic "0" value. The stress time for all defective cells was increased to five time ($5 \times 127\mu$s) the worst case stress duration in order to see if an undetected defect would become detectable. However, the defects did not show different behavior under such stress conditions (only a minor shift in V_t for Drain Stress$_P$ experiment). Even though the drain overlap and channel defects do not seem to impact the performance of the memory cell, they will pose reliability concerns. Further, these undetected defects most likely will be excited by cycling and will result in an in-field failure, one of the major concerns in flash memory reliability.

The above study suggests that the stress experiments may not be the most efficient way to detect tunnel oxide defects. In particular, we notice that stress tests do not result in any noticeable shift in the I-V characteristics for any of the defects. Further, it is clear that source overlap defect does impact cell performance (cell becomes depleted after erase). This suggests that the erase operation could be the key to efficient detection of tunnel oxide defects. In the next section we describe a method that can be used to detect these defects.

C. Channel Erase and Tunnel Oxide Defect Detection

In the previous section, it was shown that the drain-overlap and channel defects could not be detected by neither stress condition nor erase/program operation, thus they may remain undetected. The source overlap defect, on the other hand, could be detected because it resulted in a depleted cell when the cell was erased. Investigating further for the reason for this behavior, we found that during erase operation, the overlap area undergoes high electric field stress due to the biases applied to the gate/source terminals of the memory cell. Therefore, we felt that in order to excite and detect defects in any of the tunnel oxide regions, appropriate electric field stress must be present in every region that needs to be tested. One possible approach that offers the opportunity to stress all regions of the cell is the channel erase operation discussed below.

Unlike the commonly used NGE operation, which utilizes negative-gate-positive-source bias condition, channel erase concept results in a uniform electric field stress in all regions of

the tunnel oxide. The NGE technique restricts the high electric field region to only the source overlap area. The channel erase approach is accomplished by biases applied either to the control gate only, or by using gate and substrate biases (i.e. in triple well technology). In our study, we chose to use the method where only control gate is biased with -20V while grounding the substrate and floating the source and drain terminal. Further, for the cell structure created in our study, a channel erase approach would require 70ms erase time, which is substantially longer time compared to the NGE approach which requires only 10ms.

In order to analyze the effectiveness of channel erase technique in identifying tunnel oxide defects, we ran the same experiments that were performed previously, but this time using the channel erase approach. The results of this study are shown in Table V. It is evident that every defect in this case results in a depleted cell. These observations suggest that the channel erase technique is far more effective and superior in detecting all tunnel oxide defects.

TABLE V
CHANNEL ERASE EXPERIMENTS

Operation \ Defect	Threshold Voltage (V)			
	Fault Free	**Source**	**Drain**	**Channel**
Program	7.9581	7.9094	7.1271	7.9764
Erase	1.1066	-1.4758	-1.9736	-2.3726
Gate Stress$_E$	1.1066	-1.4758	-1.9736	-2.3726
Drain Stress$_E$	1.1066	-1.4758	-1.9736	-2.3724
Gate Stress$_P$	7.9581	7.9094	7.1271	7.9764
Drain Stress$_P$	7.9577	7.9091	7.1026	7.9761

D. ONO Defects and Impact of Cell Performance

Next we expanded our investigation to study defects in the ONO layer. We used the same approach as before and faulty cells with ONO defects were constructed and simulated. Two type of defects were simulated. First, a defect is created in the bottom oxide layer of the ONO layer (see Figure 2e). The fault free value of this layer was approximately Å96 and in the presence of a defect it has an effective thickness of Å67. Second, a defect in the top oxide layer of the ONO layer (see Figure 2d) was also created and simulated. The fault free thickness in this case was Å100 and that of the defective cell was Å71. The results of the study of these defects are compared to the fault free case in Table VI. It is apparent that defects in the ONO layers do not impact the performance of the flash memory cell and hence can be ignored. This finding supports what was previously argued and suggested in [2], [14] using logical reasoning only.

E. Simulation Summary

We summarize the important findings about various defects as follows. These findings are used to develop efficient tests for various defects in the 1T cell based flash memories.

- **Defect Excitation**: Stress tests are not very effective in defect excitation. It was shown that the erase operation is a more effective way to excite tunnel oxide defects.

TABLE VI
ONO DEFECTS SIMULATION

Operation \ Defect	Threshold Voltage (V)		
	Fault Free	**ONO$_B$**	**ONO$_T$**
Program	7.9581	8.5420	8.5437
Erase	1.1066	1.1765	1.1434
Gate Stress$_E$	1.1066	1.1765	1.1434
Drain Stress$_E$	1.1066	1.1765	1.1434
Gate Stress$_P$	7.9581	8.5420	8.5437
Drain Stress$_P$	7.9577	8.5413	8.5431

- **Fault Detection**: Channel erase technique is superior in detecting all defects compared to NGE method.
- **Depleted Cell Behavior**: All tunnel oxide defects result into depleted threshold voltages when channel erase technique is used. Therefore, a test for depleted cell, rather than erased/programmed cell, as previously suggested in [2], [3], [4], is likely to be a more efficient method for detecting such defects.
- **ONO Defects**: No single defect in the ONO layer will result in faulty behavior. Hence, tests for ONO defects can be simplified by removing those patterns.

V. TEST ALGORITHMS

After considering the above findings, we conclude the following for testing flash memories: 1) we must consider all tunnel oxide defects and 2) we must utilize channel erase technique to excite the various defects in tunnel oxide region. We also conclude that ONO defects can be ignored and ONO layer can be assumed to be fault-free. We further conclude that to develop a test to detect tunnel oxide defects, the following conditions must be met:

Programmed Initial State
: All cells to be tested must be programmed (i.e. set to logic "0" state).

Channel Erase Fault Excitation
: Programmed cells to be tested must be erased using channel erase technique.

Figure 3 gives a new test procedure called Flash-CE test, which can be used to detect all defects in the tunnel oxide layer of 1T cells organized in a NOR array. Since most disturb faults are assumed to be caused by defects in the tunnel oxide, we can claim that this algorithm can detect all disturb faults. In Figure 3, n and m represent the number of rows and columns in the memory array, respectively. The working of the algorithm is as follows. Step 1 initializes the array to a programmed state. Step 2 erases all cells in the array using channel erase approach, hence exciting all tunnel oxide defects. The third step programs each cell in the first row ($i = 0$) of the array and reads each element of that row, expecting a value of "0". In case there is any depleted cell in any column (defective cell), the read operation will fail and the value will be read as "1". This is so because of the excessive depletion of the defective cell and as a result the column containing the defective cell will read a logic 1 value.

```
1. For (i=0; i < n; i++)       \* Initialize array                *\
      For (j=0; j < m; i++)
         (w0)_{i,j}
2. For (i=0; i < n; i++)       \* Erase array                     *\
      For (j=0; j < m; i++)    \* using channel erase             *\
         (w1)_{i,j}
3. For (j=0; j < m; j++)       \* Program then read row 0         *\
      (w0,r0)_{i=0,j}
4. For (i=1; i < n; i++)
      For (j=0; j < m; j++)    \* Program remaining cells         *\
         (w0)_{i,j}
5. For (i=0; i < n; i++)       \* Erase array                     *\
      For (j=0; j < m; i++)    \* using channel erase             *\
         (w1)_{i,j}
6. For (j=m-1; j ≥ 0; j- -)    \* Program then read row n-1       *\
      (w0,r0)_{i=n-1,j}
```

Fig. 3. Algorithm Flash-CE

After this step, the only cells that remain to be tested are those in the first row. Steps four, five and six initialize, excite, and detect these remaining faults in a similar manner.

In recent years "March tests" have gained popularity and have been used in many test algorithms for testing flash memories [4], [3], [14]. This is due to their simplicity, fault detection capability, and ease of implementation. We have developed an efficient (minimum length) march algorithm, called March_{CE}, which can detect all tunnel oxide defects and is as follows:

$$March_{CE} = <\Uparrow w0; E_{Ch}; \Uparrow (w0, r0); E_{Ch}; \Downarrow (w0, r0)>$$

In this algorithm, the term E_{Ch} represents a "w1" on the whole array since a selective "w1" in flash memories is not permissible. Further, the subscript "Ch" in the erase operation signifies the fact that the erase operation uses channel erase instead of the conventional source side or NGE operation. March-CE algorithm is inefficient in detecting other types of faults, such as SAF and SOF (only 50% of SAF, 0% of SOF). However, by adding few additional read operations, the algorithm March_{CERR} given below, can detects 100% of SAF, AF, SOF, TF, and CF_{st} faults.

$$March_{CERR} = \\ <\Uparrow w0; E_{Ch}; \Uparrow (r1, w0, r0); E_{Ch}; \Downarrow (r1, w0, r0)>$$

The detection capabilities were computed using RAMSES [20] memory simulator assuming a 1-bit wide memory. In order to implement the channel erase approach in the March algorithms proposed, the design of the memory array may need to be modified. The modification requires the addition of new high voltage switches to the row decoders and additional control logic and the discussion of such design for testability (DFT) concepts is beyond the scope of this paper.

VI. Conclusion

In this paper we first studied different defects that are responsible for disturb faults in 1T flash cell using a 2D device simulator. It was found that stress tests are not efficient when it comes to detecting tunnel oxide defects. Oxide-Nitride-Oxide layer defects were found to be benign and did not result into faulty behavior and hence they can be ignored. Efficient tests based on channel erase techniques were developed to detect tunnel oxide defects (hence disturb faults) as well as other type of faults such as SAF and AF faults.

Acknowledgment

The authors would like to thank Faisal Al-Hasawi of the Public Authority of Applied Education and Training-Kuwait for his help in preparing this manuscript. This work was support by Kuwait University research grant No. [EO01/04].

References

[1] M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*, 1st ed. Norwell, Massachusetts: Kluwer Academic Publishers, 2000.

[2] M. Mohammad, K. Saluja, and A. Yap, "Fault Models and Test Procedures for Flash Memory Disturbances," *Journal of Electronic Testing: Theory and Applications*, vol. 17, no. 6, pp. 495–508, December 2001.

[3] J.-C. Yeh, C.-F. Wu, K.-L. Cheng, , Y.-F. Chou, C.-T. Huang, and C.-W. Wu, "Flash Memory Built-In-Self-Test Using March-Like Algorithms," 1st *international workshop on Electronic Design, Test, and Applications (DELTA'02)*, pp. 137–141, 2002.

[4] S.-K. Chiu, J.-C. Yeh, C.-T. Huang, and C.-W. Wu, "Diagonal Test and Diagnostic Schemes for Flash Memories," *Proc. International Test Conference*, pp. 37–46, 2002.

[5] *IEEE 1005 Standard Definitions and Characterization of Floating Gate Semiconductor Arrays*, 2nd ed. Piscataway: IEEE Standard Department, 1999.

[6] *ATLAS User's Manual: Device Simulation Software*, Silvaco International, April 1997.

[7] A. van de Goor, *Testing Semiconductor Memories: Theory and Practice*. Gouda, The Netherlands: ComTex Publishing, 1998.

[8] Z. Al-Ars and A. van de Goor, "Test Generation and Optimization for DRAM Cell Defects Using Electrical Simulation," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, no. 10, pp. 1371–1384, October 2003.

[9] M. Azimane and A. L. Ruiz, "A Special March Test to Detect Delay Coupling Faults for RAMs," 8th *IEEE International Conference on Electronics, Circuits and Systems*, vol. 2, pp. 995–999, 2001.

[10] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, "Flash Memory Cells-An Overview," *Proc. of IEEE*, vol. 85, no. 8, pp. 1248–1271, August 1997.

[11] S. Aritome, R. Shirota, G. Hemink, T. Endoh, and F. Mausouka, "Reliability Issues of Flash Memory Cells," *Proc. of IEEE*, vol. 81, no. 5, pp. 776–787, May 1993.

[12] A. Brand, K. Wu, S. Pan, and D. Chin, "Novel Read Disturb Mechanism Induced by Flash Cycling," *International Reliability Physics Symposium*, pp. 127–132, 1993.

[13] P. Cappelletti, C. Golla, P. Olivo, and E. Zanoni, *Flash Memories*, 1st ed. Norwell, Massachusetts: Kluwer Academic Publisher, 1999.

[14] M. Mohammad and L. Al-Terkawi, "Techniques for Disturb Fault Collapsing," *Journal of Electronic Testing: Theory and Applications*, vol. 23, no. 4, pp. 263–268, August 2007.

[15] A. van de Goor and Z. Al-Ars, "Functional Memory Faults: A formal Notation and a Taxonomy," 18th*IEEE VLSI Test Symposium*, pp. 281–289, 2000.

[16] *ATHENA User's Manual: 2D Process Simulation Software*, Silvaco International, November 1998.

[17] A. Sharma, *Advanced Semiconductor Memories: Architectures, Designs, and Applications*, 1st ed. IEEE Press, 2003.

[18] M. Mohammad and K. Saluja, "Optimizing Program Disturb Faults Test Using Defect-Based Testing," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, no. 6, pp. 905–915, June 2005.

[19] A. Chimenton, P. Pellati, and P. Olivo, "Overerase Phenomena: An Insight Into Flash Memory Reliability," *Proceedings of The IEEE*, vol. 91, no. 4, pp. 617–626, April 2003.

[20] C.-F. Wu and C.-W. Wu, "RAMSES: A Fast Memory Fault Simulator," *IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems*, pp. 165–173, 1999.