Testing in Nanometer Technologies

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Abstract

The last 25 years have been a very exciting time for the people involved in testing. As an industry we had a very difficult time generating tests for boards which had only 1000 logic gates on them with packages which had only a few logic gates per module. Because of these difficulties a number of people started to look for different approaches to testing. It was clear to many that automatic test generation for sequential networks could not keep up with the rate of increasing network size. This resulted in many changes in the way designs were done. This increase in gate count resulted in the development of the area of Design for Testability. Test in these 25 years was driven by the increase in gate count coupled with the inability of automatic sequential test generation to keep pace.

Today we are looking at an era before us which also has the gate count increasing at virtually the same rate. The Design for Testability techniques such as Full Scan, LSSD, etc. seems to be well in place. However, there is a significant difference brought on by the technology developments facing us. The onset of deep sub-micron (now currently alluded to as Nanometer Technology) is changing the way chips are being designed and manufactured. Because of the large capacity of these new chips, plus the expense of new designs, embedded systems are setting the pace for today and the future. New problems are arising that are driving design automation to integrate all the tools that are needed to successfully take a design from concept to reality in this new design environment. Test is one part of this process that is getting significant attention. An area once classified as a "back end" process in the design flow is moving closer to the "front end". Design methodologies are incorporating test-related structures in the beginning of the design cycle. In addition, standards to manage the test complexity of these large designs are being proposed. For example, IEEE P1500 is working towards defining a structure for embedded cores such that tests can be delivered to these cores. This alone is a strong challenge for the Test Community. It is clear that design and testing of Embedded Systems is the key challenge to the Test Community as we face these new technologies. This includes both the tools that are required to test these designs and the testers to deliver these tests to the device under test. In addition these Nanometer Technologies bring a number of issues which the Semiconductor Industry Association (SIA) Roadmap refers to as Grand Challenges. These include > 1GHz Cycle time, higher sensitivity to Crosstalk, and tester costs. This paper will examine the challenges that face testing in this New Frontier.

As we proceed from 250nm technology the SIA Roadmap points out – “In the GHz frequency regime, circuit elements can no longer be treated as discrete elements, and transmission line approaches will be increasingly required.” Scaling at this stage is very different than it was 6 years ago. Today we have the situation that with normal scaling the gate plus line delays will result in lower performance chips than we had at technology levels, which were less aggressive. This is contrary to what the industry had been used to over the last 15 years of designs following Moore’s Law. As one scales a technology the dimensions become smaller and smaller, a new issue of electromagnetic coupling begins to play a very major role.

It is clear that doing just DC Stuck at Fault testing will not be adequate to obtain the kind of quality that we need at the chip and at the board levels. The easy answer is to buy a very high performance tester to do the job. As pointed out in the 1994 SIA Roadmap, the testers are not capable of fully keeping up with the technology performance as we go into nanometer designs. Even with the higher performance of the testers, the cost can very quickly become prohibitive. This is an excellent opportunity for Self-Test designs, which can have very high fault coverage of stuck at and delay faults with low tester bandwidth. However, because of the high demands made on the designers with respect to performance, one must also be able to introduce these test structures in a way that does not adversely impact the design performance

space. As was stated in the 1989 Keynote presentation of the IEEE International Test Conference, synthesis and test become very interrelated. This is in fact what the industry must do to obtain the very best in quality of test with the highest results. The designer must have interactive control of how and where test structures are put into the design. This implies that test points and test structures are inserted in such a way that they do not violate the target cycle time of the design. Thus we have to add in the Scan and BIST while still controlling the cycle time of our designs. This also requires that the design community is given tools that will allow him or her to monitor the insertion and impact both from a test and design standpoint. In an effort to eliminate test from the critical path in the design flow Static Verification is becoming more and more important. This allows the designer to test the quality of their designs without having to go through all the efforts of test generation. There are many challenges facing our industry as we drive towards implementing nanometer technologies.