Testing Mixed-Signal Cores: A Practical Oscillation-Based Test in an Analog Macrocell

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A formal set of design decisions can aid in using oscillation-based test for analog subsystems in SoCs. The goal is to offer designers testing options that don't have significant area overhead, performance degradation, or test time.

With the advent of system-on-a-chip (SoC) designs, the semiconductor industry wants to solve problems that constrain the coexistence of analog and digital cores on a single chip. This is an interesting activity, mainly for the so-called IP companies that offer complex building blocks to system designers. These system integrators must combine logic, memory, data converters, analog processing circuits, and even (for the telecommunications market) RF front ends. Merging so many different technologies poses new challenges, such as developing design and test methodologies capable of ensuring system performance and reliability for a reasonable design effort.

The goal is to ensure minimal production difficulties, even though a variety of licensee partners will use cores for many designs and many potential applications. Reusability is the objective of all IP vendors, and testing is essential to achieving this objective. A key component for a complex core, whether digital or analog, is a test methodology that the system integrator can easily and effectively use in various application scenarios.

Testing embedded building blocks is far more difficult than testing their stand-alone counterparts, and it is usually impossible to use conventional testing techniques. Of mixed-signal IC components, analog cores are the most affected by this problem, because analog testing relies on checking functional specifications. Such testing can be time-consuming and requires extensive access to the core's inputs and outputs. These requirements can put functional testing in conflict with the realities of SoCs, which require short test times, have a limited number of available pins, and offer only limited access to a core's input and output terminals.

Furthermore, functional testing techniques differ greatly, depending on the type of analog component. Such diversity makes it almost impossible to define a general (functional) testing methodology that is applicable to any analog block. Consequently, the testability of analog cores plays a crucial role in the feasibility of a complex system. So an analog core's market appeal depends on the development of test strategies that work across different application environments.

In digital circuits, structural or fault-driven test methods and built-in self-test (BIST) alternatives have proven helpful. These strategies increase accessibility, and provide core isolation and access to test resources. But they can have a high cost in terms of area overhead, wasted power, performance degradation,

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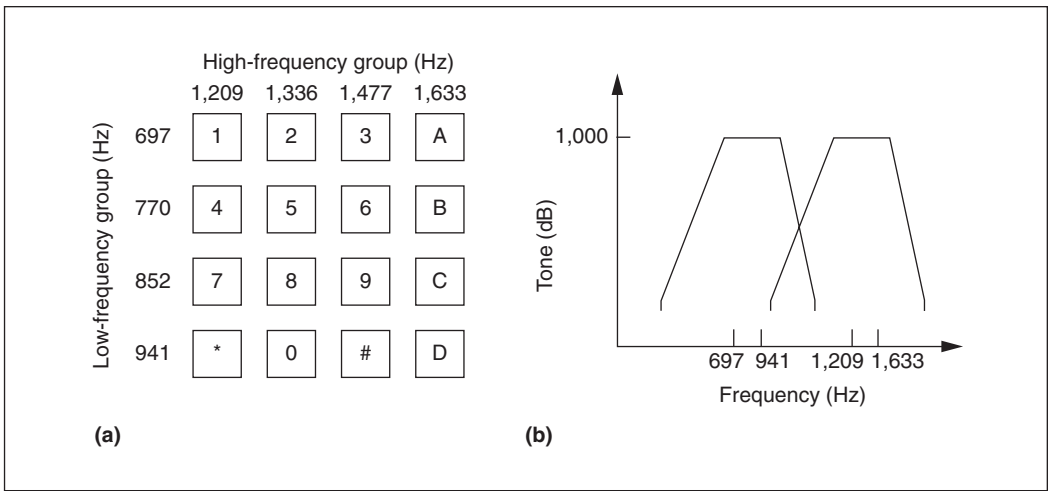

Figure 1. Dual-tone multifrequency (DTMF) receiver keyboard and frequencies (a), and signal derived from keyboard inputs (b).

noise, and parasitic penalties.

In analog circuits, neither moving from functional to structural testing nor incorporating BIST is a trivial issue. Such strategies are still far from wide acceptance in the analog-circuit design community. This acceptance will depend on several factors, such as compatibility with functional test approaches, test efficiency, test confidentiality, and additional design effort. However, developing structural test approaches is essential for IP providers. In the IP market, it is appealing to offer a range of solutions to users, giving them the opportunity to either select among or combine these possibilities, ranging from functional to structural options.

Among the emerging structural test solutions, oscillation-based test (OBT) deserves attention because it is conceptually simple, does not require extensive circuit modifications for testing, and can handle BIST without the penalty of dedicated, additional, on-chip hardware for signal generation. OBT is essentially a defect-driven test approach, and researchers have successfully applied it to significant examples, such as biquadratic filters and basic data converter circuits.[1-3]

Here, we extend OBT to a system whose complexity is far higher than that reported to date. The macrocell we studied is intended for use as an IP core, so this work extends our earlier results.[4,5]

Demonstrator core cell

Many SoCs for communications use a complex macrocell that serves as a dual-tone multifrequency (DTMF) receiver to decodify telephony dialing information. Vendors intend such receivers for broad use in dedicated terminals. These cells are gaining importance in telecommunications, finding use in paging systems, repeaters, mobile radio, credit card systems, remote control, personal computers, and answering machines. Vendors sell them as stand-alone, mass-produced chips or as cores for embedding in complex SoCs. In the latter case, the test support around the cell must be flexible enough to let users select a test strategy based on their needs rather than mandating the use of a fixed test methodology.

The DTMF receiver's input is a composite audio signal produced by superposing two tones selected by the line-and-column addressing of a keyboard like that shown in Figure 1a. The receiver's output is a digital code derived from the input signals.

A band-splitting filter first processes the DTMF signal, separating high- and low-band frequencies, as Figure 1b shows. A decoder then modifies the signal to be square-shaped and decodes it. The decoder's task is to establish whether the present frequencies are recognizable as a DTMF tone.

Figure 2 illustrates the system configuration, which has low- and high-pass filter paths. The

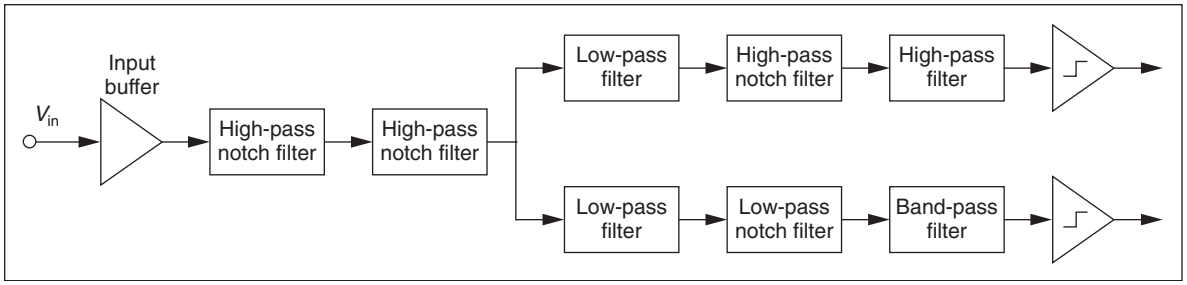

Figure 2. Analog subsystem of a DTMF receiver.

filter bank consists of a cascade of several second-order functions, including many typical transfer-function types (low pass, band pass, high pass, low-pass notch, and high-pass notch). Two comparators form the interface to the system's digital part, which detects the presence of correct dial tones and validates a tone that satisfies the requirements for tone duration.

Our work addresses only the analog subsystem, because designers use conventional techniques to design and test the digital subsystem. We have implemented every second-order function in Figure 2 using a switched-capacitor (SC) biquadratic filter.[6] Because the analog part of this macrocell is essentially a filter bank, we can extend our earlier work[7] to develop a DFT methodology for every component stage in the system given in Figure 2.

Oscillation-based test

OBT and oscillation-based BIST (OBIST) both rely on transforming the system under test (SUT) into an oscillator by adding a feedback path and modifying the circuit (adding or removing some passive components).[1-5] These approaches then split operation into two modes:

- operational, in which the system connects to its regular input, and
- test, in which a closed feedback loop encircles the SUT, and the regular input is disconnected.

Removing components can render them untestable,[7] leading to the following rule:

Design decision 1. Apply OBT without removing components from the normal signal path.

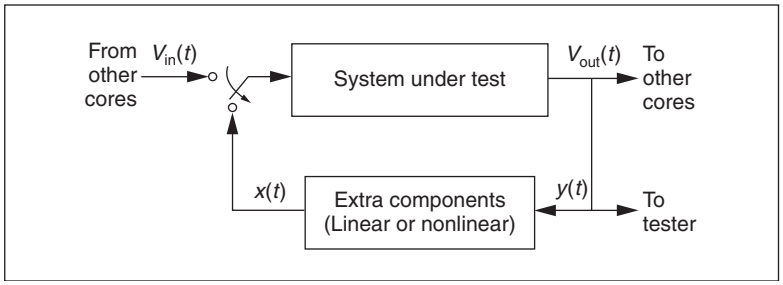

Figure 3. Block diagram showing the modification to convert a system under test to an oscillator.

Figure 3 shows the block diagram for a system modified to apply OBT. As the figure shows, the only modification affecting the signal path arises from the need to switch between operational and test modes. During test mode, the added feedback loop and extra circuitry included within the feedback block produce self-sustained oscillations. An internal or external tester connects to the SUT output and detects deviations from the nominal oscillation frequency, indicating faulty behavior. Because the circuit generates its own test stimuli, the only difference between OBT and OBIST lies in whether the procedure carries out test interpretation on- or off-chip. We thus use the term OBT to refer to both techniques.

Designers must view implementing the system and added circuitry as a global design problem. Besides achieving the system's functional specifications, they must strive to build a robust yet precise oscillator that exists around the system when the feedback loop is closed.

OBT seems appealing in our demonstrator because it lets us test the cell more or less independently of external testers and requires only a few extra components. The circuit internally generates test signals, eliminating the need for

specific tester hardware or dedicated on-chip resources. In addition, we can preprocess test interpretation using the digital circuitry available within the cell.

Applying OBT methodology

Let us first focus on how to modify OBT basic concepts to work in an actual system.

Basic considerations

In the case of a complex cell, we must account for aspects such as system partitioning, feedback type, number and type of extra components, necessary measurements (essentially the cost of applying them), required test support at the system and subsystem levels, fault coverage, and compatibility with functional approaches.

All these issues require clever decisions that depend on the particular core or application. For example, no matter what we decide about other issues, splitting the system into smaller components is necessary because we cannot otherwise predict the fulfillment of oscillation conditions or the main oscillation properties (frequency and amplitude).

Our first approach to testing the DTMF cell was to convert the complete SUT into an oscillator. This resulted in a 10th-order transfer function, $H(z)$, because this is the order of each filter path. However, high-order oscillators are quite complex, so it's difficult to develop an analytical design. We also need an accurate model to determine the oscillator parameters, another difficult task. Of course, the overall SUT can oscillate as long as one pair of complex poles is in the unit circle. But we've found it difficult to control the specific pair that originates the oscillation, especially when all these poles differ by a relatively small value and are very close to one another (as is the case with DTMF). Furthermore, relating the oscillatory behavior to specific faults is far more difficult, complicating test interpretation. This reasoning leads to another rule:

Design decision 2. Applying OBT requires decomposing any filter into component biquadratic filters.

Keeping design decision 2 in mind, we consider two complementary problems. One relates to the biquadratic level—that is, how to make any biquadratic filter oscillate independently of its transfer function and (if possible) using a common feedback element. Another problem concerns the filter level, specifically the difficulty of combining the biquadratic-level tests to verify the entire filter. Earlier work has extensively considered the first problem and demonstrated a general solution for building robust oscillators using nonlinear feedback.[5,7] Here, we concentrate on system-level considerations in employing such a nonlinear mechanism.

We can formally describe the nonlinear block by using a 1-bit A/D converter followed by a 1-bit D/A converter,[7] and implementing an analog comparator and some switches. In such an implementation, we can control the oscillation amplitude and force every biquadratic filter to oscillate. The describing-function approach usually yields an accurate approximation to an oscillation's analytical description, so we postulate a third rule.

Design decision 3. Use a nonlinear-feedback block formed by cascading a 1-bit A/D converter and a D/A converter to force oscillations.

Another issue is determining what properties to measure during the test. Frequency-only measurements can lead to insufficient fault coverage,[4,7] making OBT of little use. The alternative is the combined measurement of both the oscillation's frequency and amplitude. In our case, we have validated how to apply OBT to the DTMF cell by extensive fault simulation using the simulation tool called Swittest.[8] For the most common faults affecting any of the cell's biquadratic components, we can summarize the measured frequency and amplitude of the oscillation's first harmonic. Table 1 displays these results, comparing the percentage of faults detected by measuring only frequency or amplitude, or by measuring both quantities simultaneously. In either case, we assumed a 5% test accuracy. From this table, it should be clear that taking two measurements is advantageous.

Design decision 4. Evaluate both the frequency and amplitude of oscillations to obtain high fault coverage.

System considerations

After identifying a unified manner for forcing any biquadratic filter to oscillate, we must examine how to efficiently support this technique in a filter formed by cascaded biquadratic filters. To use OBT on such a cascaded filter, we disconnect each biquadratic filter from the filter signal path and connect it to the nonlinear feedback loop. Two possibilities exist for accomplishing these modifications. One is to simultaneously convert all biquadratic filters to oscillators, as Figure 4a shows (a parallel test). Another alternative is to convert them sequentially, as Figure 4b shows. The former relies on closing a feedback path around every biquadratic filter after isolating that filter from the rest of the circuit. This parallel test requires one comparator per biquadratic filter. Sequential testing, on the other hand, requires only one comparator.

Figure 4 shows that this strategy requires several switches to connect and disconnect all local feedback loops. An effective design for such switches is critical because their inclusion can degrade overall circuit performance. Later, we will discuss how to minimize this problem by using the so-called switchable opamp (sw-opamp) concept.

To come up with a new design decision, we must consider this potential performance degradation and the area or power penalty of

Table 1. Fault coverage for every biquadratic filter in the DTMF core.

Filter number	Detected faults (%)	
	Only frequency or amplitude measured	Both frequency and amplitude measured
1	76.7	100
2	78.3	98.3
3	86.7	98.3
4	83.4	100
5	80.0	100
6	71.7	98.3
7	88.3	100
8	81.6	100

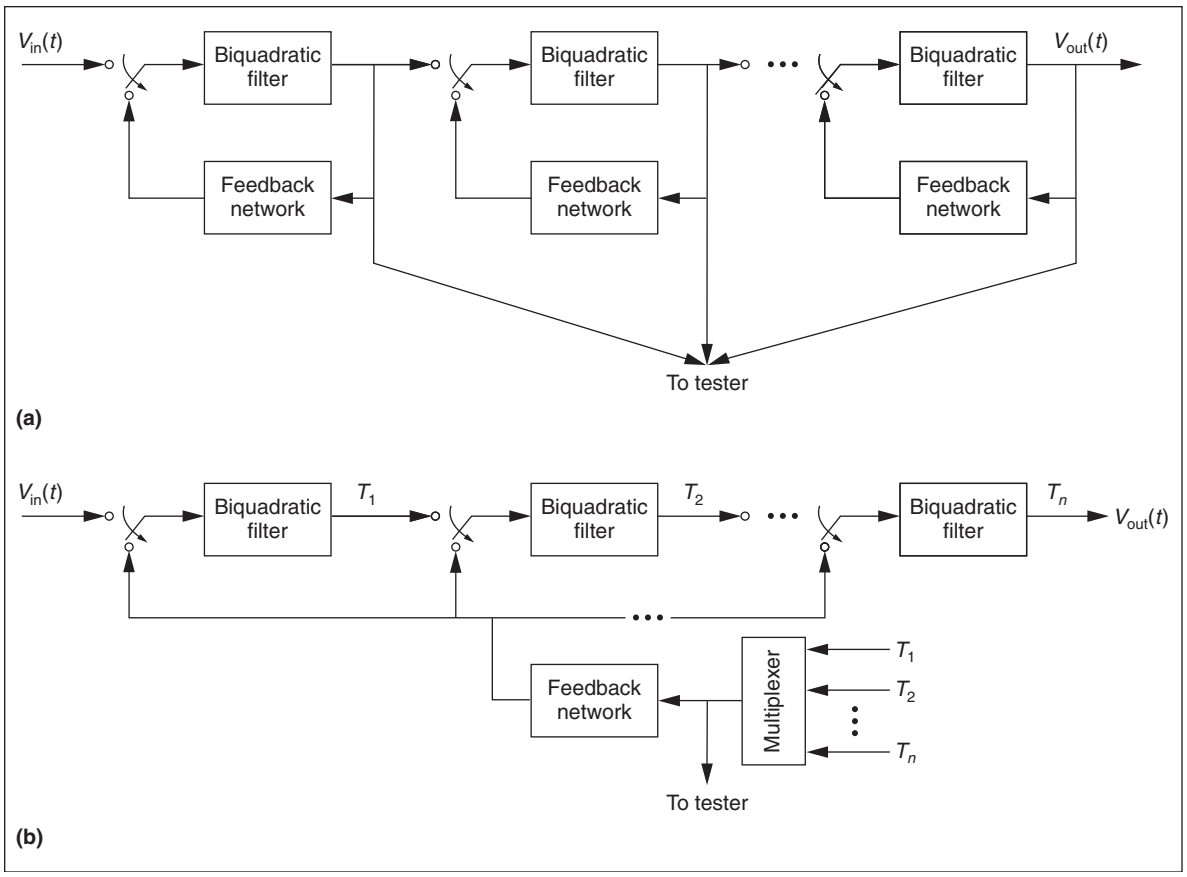

Figure 4. Block diagram of SUT converted to an oscillator: parallel (a) and sequential (b) cases.

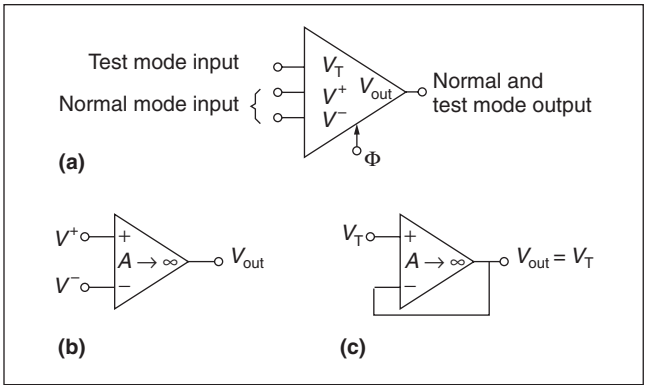

Figure 5. Switchable opamp (a); the device has $\Phi = 0$ to act as an opamp for normal mode (b); in test mode (c), $\Phi = 1$, and the device acts as a buffer.

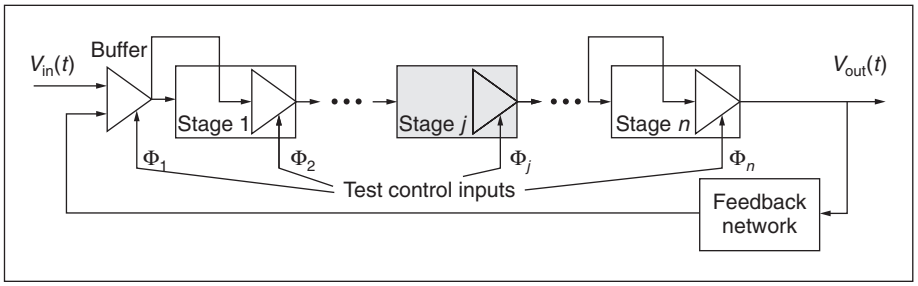

Figure 6. Block diagram of SUT converted to an oscillator using sw-opamps.

each approach. In our example, we can reuse existing comparators for testing and employing a global feedback loop (as we will prove later in the article).

Design decision 5. Use a sequential test structure to minimize the number of additional components.

The next step is to implement the sequential test concept with a minimal cost in terms of area, power, and performance. Fortunately, we can apply an idea reported a few years ago; researchers have successfully applied it to DFT.[9,10]

Figure 5 shows an sw-opamp, a device that operates in two modes controlled by a logic signal. In its normal mode, the sw-opamp performs like a conventional opamp, amplifying the difference between its regular inputs. In test mode, the control signal enables a third signal, V_T. The sw-opamp circuit actually copies V_T at the output; this is because in test mode, the device operation is similar to that of a unity-gain buffer.

Keeping this functionality in mind, we can substitute the second opamp—the opamp providing the output to the next stage—in every biquadratic filter with an sw-opamp. Then, we can connect the test input of every sw-opamp to the previous stage. Others have reported on a similar structure.[10] This leads to our sixth design rule:

Design decision 6. Use sw-opamps to selectively close the feedback loop.

Figure 6 shows the filter structure after this change. This filter now has a single feedback loop, but only one stage (the *j*th stage) can act as an oscillator. The other stages act as buffers either to pass the feedback signal to the *j*th stage input or to pass the oscillator output to the filter's primary output. This change also simplifies the sequential structure in Figure 6 because the filter no longer requires multiplexing at the feedback block's input.

Control is very simple: When the *j*th stage is under test, the test control signals for all sw-opamps, excluding the sw-opamp that belongs to this particular stage, must be high. Therefore, the test control signals are always a bitstream of 1, and are exclusively 0 in the stage under test position *j*. An important advantage of this procedure is that it inherently tests all the added components. When the *j*th biquadratic filter is under test, the test loop contains all the added switches within an opamp, so the test checks them too. Hence, along the entire test process, the test checks all the elements. So our next design rule recommends this single-loop configuration:

Design decision 7. Transform the OBT sequential structure into a single-loop, complex oscillator.

Modified system architecture

We can incorporate the preceding design decisions into the core demonstrator. Because this circuit has two paths, we implement the design decisions through the double oscillation

loop shown in Figure 7. As this figure shows, we propose using the comparators available in the circuit connected to a 1-bit D/A converter. Thus, we can test particular biquadratic filters by closing the appropriate loop. For instance, closing the upper loop will test the biquadratic filters in the upper path. Closing the lower loop will test the lower path of filters. Closing either loop, on the other hand, will test the two biquadratic filters shared by both paths.

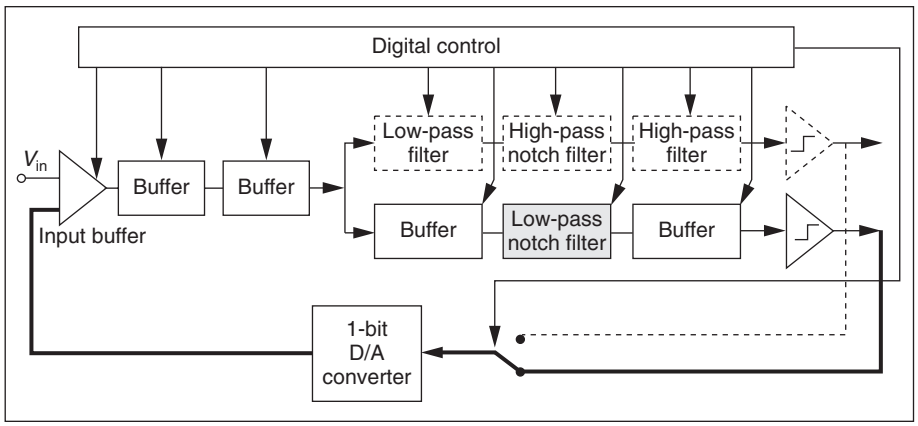

Figure 7. Modified DTMF receivers showing the test of a biquadratic filter, the low-pass notch filter represented by the shaded box.

This implementation requires only the addition of a D/A converter in the common part of the feedback loops, plus a (simple) control circuit. These minor modifications make the silicon area overhead quite small. Those elements present in both the conventional and the OBT design should be designed to have a similar performance, which means that the design effort does not increase. These observations lead to two more design rules:

Design decision 8. Consider how to reuse every block in the complete filter structure to reduce the cost of OBT.

Design decision 9. Reuse every comparator in the oscillator feedback path.

To understand the proposed OBT-DTMF structure, consider how we must program the system to test the low-pass notch filter located in the lower path in Figure 7. We close a loop using the corresponding comparator, and the biquadratic filter under test remains unaltered. All the remaining stages in the loop emulate a buffer through their sw-opamps, in accordance with Figure 6. Thus, the overall closed-loop system (emphasized by the thicker lines in Figure 7) corresponds to the oscillator associated with this biquadratic filter. A dashed line represents blocks placed in the upper path because they are not part of the oscillating loop for this case. We use these upper blocks to read the test signal output from the second stage.

This approach has some practical limitations. First, in test mode, every buffer in the chain introduces a delay at the test frequency. Nevertheless, for frequencies much lower than the unity-gain frequency, this delay is quite small, and we can neglect the accumulated loop delay. If the frequencies are not much lower than the unity-gain frequency, we can estimate the delay and account for it in the analytical calculations. Simulation can also model delay.

A second problem comes from the describing function's limited accuracy and the signal purity at any point of the global feedback loop. This problem leads to a distorted oscillator signal, but remains insignificant in most cases. As far as the DTMF demonstrator is concerned, there is enough filtering, but it does not actually matter, because we can model (to a reasonable approximation) the distorted signal at any biquadratic filter's output.

One other important feature is worth considering: We must guarantee that every component, either in the filter or in the feedback network, is tested. It should be clear from Figure 7 and the test operation described here that this procedure tests every biquadratic filter once. Additionally, this procedure tests all the sw-opamps in both modes (operational and testing). In fact, it tests the test path $n - 1$ times (where n is the number of biquadratic filters), and this practice can help in diagnosis, reducing the impact of the extra components on system testability. Only the input terminal and its connection to the signal path require additional checking.

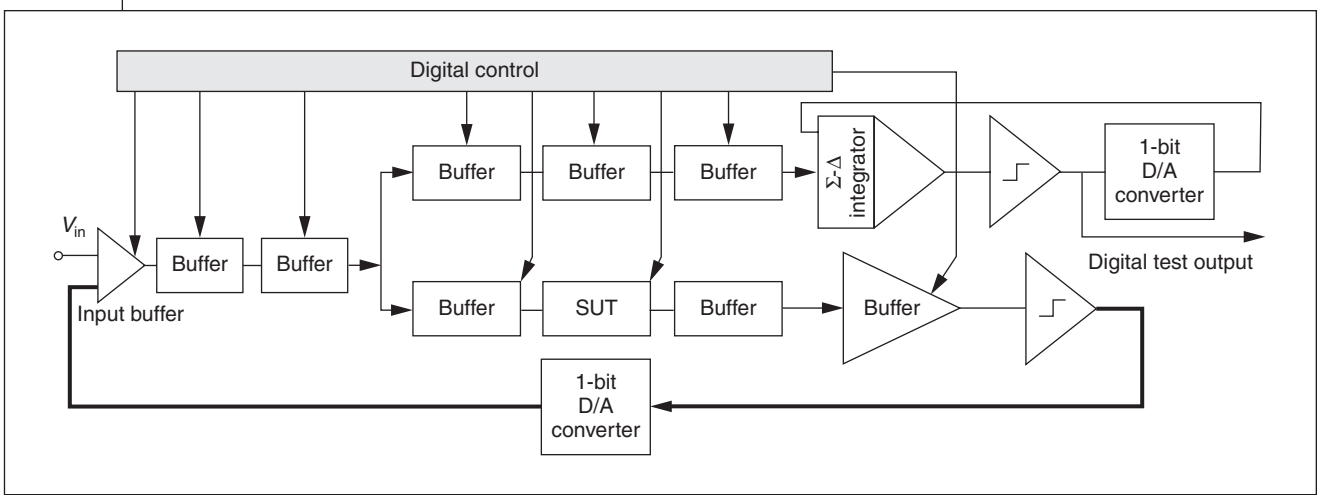

Figure 8. Generation of a bitstream output for test.

Extension to OBIST

The next issue to consider is how to support frequency and amplitude measurements. Reading an analog signal is feasible, but noise limits measurement accuracy. Increasing the accuracy imposes extra, undesirable, design requirements. Although frequency information is easily coded in digital information, the same is not true for amplitude information. But good fault coverage requires that we measure both, meaning we must translate all the signal information into digital data.

A convenient way to achieve such coding is to use an oversampling A/D converter.[11] For our purposes, a medium-resolution converter should suffice. Using blocks similar to those necessary for the nonlinear feedback previously discussed, we can synthesize a Σ-Δ modulator capable of providing a 1-bit digital version of the test output.

The complete circuit in Figure 7 has two available comparators. Although not explicitly shown in the figure, an extra buffer connects every filter channel and the corresponding comparator. Thus, we can again use an sw-opamp instead of a regular buffer. In one of its operational modes, such an sw-opamp acts as a buffer; in the other mode, we use it to implement a discrete-time integrator. In this latter mode, a closed, local feedback loop provides a simple Σ-Δ modulator that generates a digital bitstream for reading by an external tester or for feeding into a digital interpretation circuit. We can switch the integrators at a higher frequency to comply with the oversampling requirements, although most practical situations can use the same sampling rate as that for the filter.[11]

In particular, Figure 8 illustrates the case in which a biquadratic filter in the lower filter bank is under test (specifically, the same notch filter shown in Figure 7). We then use one of the comparators to close the oscillation feedback loop; the other comparator implements the A/D converter for testing. An equivalent connection can test the biquadratic filters in the upper filter bank. These observations lead us to our last design rule:

Design decision 10. Around every comparator, build up a low-accuracy Σ-Δ modulator for readout.

Test strategies

To qualify the OBT approach for IP, we must

- compare it to a functional test strategy, and
- define a way to use both basic strategies (structural OBT and functional test) in a cooperative way.

Our intention is to discuss how the design community can use the best of both approaches for any particular case. We must consider the testing cost for each approach in terms of required resources and test application time, as well as its suitability for BIST.

As a first consideration for comparison, we

Table 2. Test feature comparison.

Test	Type	Fault coverage	Time	Signal generation	Signal interpretation
Complete test	Functional	Very high	Very high	External, complex	External
Functionality test	Functional	Very high	High	External, 16 tones	External
Two-tone test	Functional	Reasonable	Medium	External, two tones	External or internal
Serial OBT	Structural	High/very high	Medium	Internal	External or internal
Parallel OBT	Structural	High/very high	Low	Internal	External or internal

must describe typical test routines for the functional test of a stand-alone DTMF chip. Besides a complete set of measurements giving the transfer functions associated with the twin filter channels, industry uses an extensive characterization test.[12] This characterization test determines how the circuit can separate the 16 tone combinations (high and low band). Such a test is functionally sufficient, but the time required to apply it is prohibitive for mass-produced ICs.

For production testing, a simpler alternative involves detecting the separation between a subset of these combinations. A possible subset could be tone pairs in one of the diagonals on the keyboard, or even a two-tone signal formed by the highest frequency of the low-frequency group and the lowest frequency of the high-frequency group. We must also evaluate a burst of periods to eliminate transient effects; the burst time duration depends on the filter's settling time.

In terms of equipment, all the procedures we discussed require precise tone generation hardware outside the chip. Test interpretation can basically execute on-chip by taking advantage of the DTMF digital subsystem.

BIST, on the other hand, requires significant modifications to incorporate signal generation. Apparently, multitone digital oscillators are a good option, but digital generation usually requires huge hardware resources that are not always available or readily usable for on-chip testing.[13]

OBT basically makes few demands of external testers, because it does not need test stimuli. Instead, we must modify the DTMF digital subsystem to interpret the signals coming from the test. However, because we can digitally encode these signals, it takes only one digital pin to move them out of the chip.

As explained earlier, there are two alternatives—parallel and sequential—for applying OBT. The former requires one comparator per biquadratic filter. The latter requires only one comparator—a significant savings in area. However, test time differs for both cases. The parallel case carries out all measurements simultaneously; the sequential case's test time can be far longer, because its total test time is the sum of the test time for the individual biquadratic filters in the DTMF.

Oscillation startup could be a problem if it is not given special attention. In practice, using sw-opamps facilitates forcing a start-up condition and shortening the oscillation buildup time. In any case, this extra time can influence overall test time. But again, in the parallel case, this time equals the highest start-up time of the eight oscillators. For the sequential case, the oscillation settling is the sum of the start-up times for every oscillator. The difference between both cases depends on the frequencies to be measured, the biquadratic structures, and the required measurement accuracy (relative to the number of measured cycles).

Converting OBT to OBIST is relatively simple; it only requires extending the digital subsystem to perform some extra processing of the bitstream coming from the Σ-Δ modulator. Digital-transition counting seems a promising yet simple way to provide a fault-free digital signature.[7] Table 2 summarizes the main features of these different test approaches.

For an IP core, it is worth considering the use of OBT combined with a simplified functional test. Both options should be available so that designers can choose either one (or a combination), depending on the particular application. The main limitations in tradeoffs between external and internal test options are

- external tester demands,
- number of pins,
- internal memory,
- extra internal circuitry, and
- test time.

Tester demands can vary greatly, but you should typically avoid scenarios that require using a mixed-signal tester for just a small part of a chip. Another important constraint is the number of available pins. Normally, pins are a scarce, shared resource when a chip contains several cores. However, sharing pins increases test time proportionally, so it should be appealing to devise methodologies with low-cost, internal generation of test stimuli.

We intend Table 2 as a complete set of possibilities from which users can select a test strategy. Depending on pin availability, intended test time, external equipment cost, internal resources, and so on, the IP customer can choose a procedure or combine procedures.

THIS WORK SHOWS that OBT is a potential candidate for IP providers to use in combination with functional test techniques. We have shown how to modify the basic concept of OBT to come up with a practical method. Using our approach, designers can use OBT to pave the way for future developments in SoC testing, and it is simple to extend this idea to BIST. The next steps in this research area will involve investigating how to decompose more complex mixed-signal cores to incorporate OBT OBIST strategies. ■

Acknowledgment

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