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Testing of mixed-signal systems using dynamic stimuli — Source link

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Topics: Transient response, Impulse response, Transient (oscillation), Test method and Linear circuit

Absorption spectra are produced using a linear ramp generator to create a frequency variation. Because the positions of the iodine absorption lines are well known [6], a scaling of the frequency axis is possible. Variations in the line shapes due to temperature fluctuations ($\Delta T \leq 0{\cdot}1$ K) are not significant [7] for the conditions presented here. Using the absorption spectrum the laser light tuning coefficient for our laser was estimated to be 1·510 GHz/V.

As can be seen from Fig. 2, near the low frequency turning point of absorption line 1104, a light intensity variation of 1% indicates a laser frequency variation of 6·95 MHz. By observing the light intensity passing the iodine cell, frequency drift measurements can be made. For example, about 30 min after switching on the free running laser, the frequency shows a drift rate of 450 kHz/min.

Fig. 3*a* illustrates the operational mode of the automatic frequency control (AFC) after switching on the laser. The frequency deviation which is shown as a function of time is

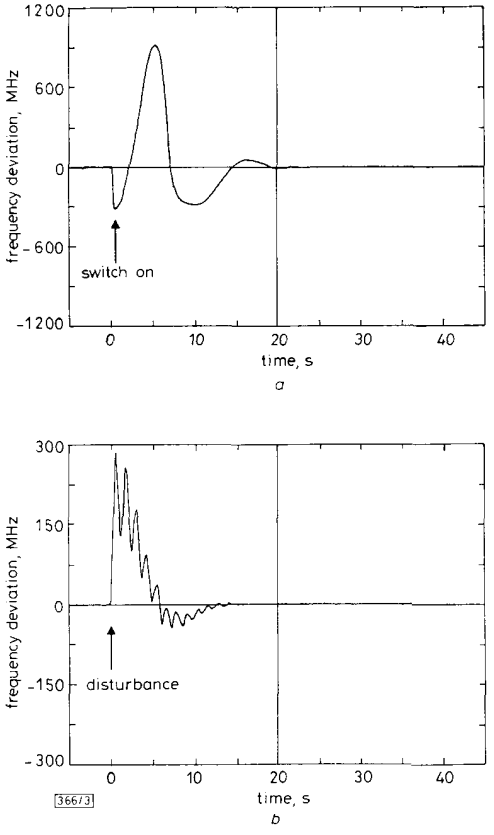

Fig. 3 *Laser frequency deviation with respect to time (frequency search process)*

a After laser is switched on

b After an externally induced frequency disturbance

proportional to the voltage measured at the temperature control input, at low response times (~1 s). The initial frequency of the laser was set about 1 GHz below where the frequency of the laser should be locked. About 20 s after switch on, the frequency is then locked. The remaining frequency jitter was measured to be less than 17 MHz, i.e. a relative frequency stability $\Delta f/f \geq 6 \times 10^{-8}$ has been achieved.

Fig. 3*b* shows the frequency response of a locked laser after a disturbance which was induced externally by a voltage pulse directed into the temperature control input. A frequency deviation of ~300 MHz is compensated for within 15 s. The superposed oscillation, having a frequency of 0·8 Hz, arises from the internal temperature control of the laser.

It was found that the locking frequency should be fixed, or be close to the turning point of an absorption line, because there, the slope of the flank in addition to the capture range of the AFC is as large as possible. Considering calibration problems [6, 7], inaccuracy of the measuring instruments, external electrical disturbances etc., the laser frequency can be determined and reproduced with an absolute accuracy of ~30 MHz, translating to $\Delta f/f \simeq 10^{-7}$. To accurately measure the absolute frequency stability, two completely independent locking systems need to be built, because their heterodyne beat signal observed with an RF spectrum analyser directly shows their frequency behaviour.

Conclusion: In summary, a simple method of frequency locking of a diode pumped Nd : YAG laser to an iodine absorption line has been presented. Because the concept can be realised in a relatively robust, compact, light and inexpensive arrangement, application to coherent free-space communication or lidar systems should be possible. To test the method presented here, in conjunction with other principles of frequency changing (piezoelectric transducer or light induced thermal frequency variation [8]), further investigations are in progress.

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TESTING OF MIXED-SIGNAL SYSTEMS USING DYNAMIC STIMULI

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Indexing terms: Integrated circuits, Testing

The impulse response of a linear circuit element contains enough information to functionally characterise that element. A technique for comparison of observed and expected (reference) transient responses, which results in an absolute measure of device functionality, is presented. Comparisons of transient response test results with the results from existing test programs are also presented.

Introduction: Mixed-signal testing is a complex subject since it encompasses all of the problems associated with digital testing, all of the problems associated with analogue testing

and some additional problems which are specific to mixed-signal testing and involve the internal connections between the analogue and digital domains. The inclusion of an interface scan (IS) path [1] partitions the analogue and digital test problems and provides controllability and observability of the internal analogue/digital interface. Assuming that the digital sections of a circuit can then be tested using existing test techniques the mixed-signal test problem reduces to an analogue test problem.

Transient response testing (TRT) [2–4] has been identified as a powerful technique for testing linear circuit elements. This technique is particularly useful in mixed-signal testing because the simple logic amplitude stimuli employed can be propagated through digital circuitry or injected via the interface scan path.

This Letter describes a technique for the automatic comparison of observed and reference transient responses and the generation of an absolute measurement of similarity, termed the index of functionality I_F.

Comparison of observed and reference transient responses: The analysis of transient responses employs a correlation technique which means that sample rates and intervals can be inferior to those dictated by the Nyquist criteria.

If X_n is an array of n evenly spaced data samples from an observed transient response at time intervals τ, and Y_n is a set of similar data samples taken from a reference (expected) transient response (either simulated or from a 'golden' device) the crosscorrelation function R_{xy} is formed by

$$R_{xy} = \frac{1}{n} \sum_{K=1}^{n} x(K\ \Delta t - \tau)y(K\ \Delta t)$$

and the autocorrelation function R_{yy} is formed by

$$R_{yy} = \frac{1}{n} \sum_{K=1}^{n} y(K\ \Delta t - \tau)y(K\ \Delta t)$$

The index of functionality is then given by comparing R_{xy} with R_{yy}:

$$I_F = \left(1 - \frac{1}{n\zeta} \sum_{K=1}^{n} |R_{xy} - R_{yy}|\right) \times 100\%$$

where ζ is a figure computed to normalise the index of functionality.

The constant ζ is derived from a comparison of the reference response and the 'most faulty' response which might reasonably be observed from a device under test. Under normal circumstances this will be a response where the output is permanently stuck-at one of the supply rails. A device which exhibits a perfect (reference-like) transient response will therefore generate an index of functionality of 100% and a device with a catastrophic fault will generate an index of functionality approaching 0%.

Having arrived at this absolute measurement of functionality, the problem is then in defining the limit, I_{FL}, for passing and failing devices, where 100% > 0%. By simulating functional faults which take the response of a device outside the limits defined by its specification the effect of such faults can be mapped into the index of functionality. Simulations have shown that this limit will usually be in the range 90–99%. Therefore if the response from a device under test produces an index of functionality $I_F \geq I_{FL}$ that device is said to be functional and if a device response produces an index of functionality $I_F < I_{FL}$ that device is defined as faulty.

Comparison of transient response tests with conventional tests: As part of a DTI/SERC LINK project involving GEC Plessey Semiconductors, Wolfson Microelectronics, the University of Huddersfield and UMIST, a mixed-signal test vehicle (MSTV) has been developed and fabricated. In addition to digital and analogue functions this device features an interface scan for control of the digital/analogue interface. The results presented here concentrate on an 8 bit D/A convertor which was one subsystem of the MSTV, the output of which can be treated as linear with the test sequence employed.

A production run of 200 devices was used as a reasonable statistical sample. Over and above simple pass/fail measurements the results for the D/A convertors were datalogged by GEC Plessey and the performance of each device assessed in relation to the rest of the sample. These results included measurements of linearity, gain and DC supply parameters.

The D/A convertors were tested using a transient response test, and the results compared to those obtained using a conventional test program. The transient response test involved accessing the input of the D/A convertor via the interface scan path, clearing it then propagating a stream of logic '1's through the input lines. This test sequence was designed to test the linearity and gain of the device, and for the presence of stuck-at or bridging faults on the digital input lines.

Shown in Fig. 1 are the ordered index of functionality results from the transient response tests of 200 D/A convertors. The devices towards the origin of the x-axis with an

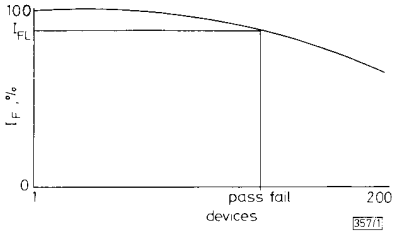

Fig. 1 *200 D/A convertors ordered in decreasing index of functionality*

index of functionality approaching 100% are good devices, and the devices towards the right of the graph are faulty devices with reduced index of functionality. However, the most faulty device in the sample of 200 generates an index of functionality of 70%. This is because the normalised index of functionality is heavily dependent on the DC level of the reference response. For this particular test, a device where the output node is stuck at the positive supply rail would generate an index of functionality of 0%.

In this case the limit I_{FL} is set at 92% and the pass/fail decisions are shown in Fig. 2. The devices highlighted on the

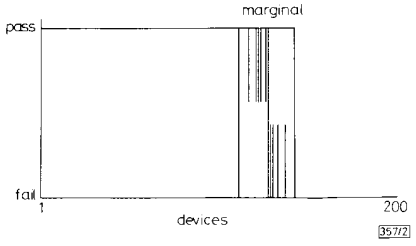

Fig. 2 *Pass/fail decisions and discrepancies with conventional test program*

graph are devices where the results of the transient response test disagree with the results of the conventional test program. In total there are nine such devices all clustered around the limit I_{FL}.

Conclusions: This work demonstrates that the results of the transient response tests are in close agreement with the results of the conventional test program. The discrepancies around the limit I_{FL} are tolerable and can be attributed to devices with marginal functionality, and therefore marginal responses. The results from the 40 devices within $\pm 10\%$ of the limit I_{FL} are in fact so similar as to make ordering meaningless.

However, the most significant aspect of these results is that the conventional test program would run on a £1 M LTX tester whereas the transient response tests were performed using a £15 K digitising oscilloscope and a 486 PC. Transient response testing, as it stands, can be used as a quick and inexpensive wafer probe test prior to packaging, however the

next phase of this work is to further develop and characterise transient analysis into an accurate production test technique.

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REALISTIC FAULT MODEL FOR EXTERNAL SHORTS IN MOS TECHNOLOGIES

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Indexing terms: Integrated circuits, Digital circuits, Logic testing

The Letter focuses on the fault modelling of external shorts in *n*-, C- and BiC-MOS digital circuits. In the context of functional testing, it is demonstrated that eight different electrical configurations may appear depending on the topological and technological parameters of the fault. Therefore, eight new logical models are defined showing that the wired-OR and wired-AND models, classically used for test pattern generation, fault simulation and defect coverage evaluation are not sufficient.

Introduction: As the density of devices on VLSI chips increases, shorts are expected to become a predominant defect [1–5]. Moreover, it has been demonstrated that more than 85% of all the likely to occur shorts are shorts between the outputs of different logic gates (external shorts) [6]. The fault model for external shorts is not clearly defined. In fact, even the electrical behaviour of the fault circuit has not been clearly analysed due to the important number of parameters such as MOS technological and topological parameters. In this context, this Letter provides an accurate theoretical analysis of the static behaviour of MOS gates in the presence of external shorts. The detectability of such faults is studied with respect to functional detection techniques (voltage test). The analysis applies to any MOS technology such as *n*MOS, CMOS, BiCMOS....

In particular, the electrical analysis will show that the fault is detectable as a logic error for a given range of short resistance values. However, in this range, the fault model to be used is independent of the short resistance value. In the case of a logically detectable fault, it is demonstrated that eight different cases must be considered. Therefore, eight fault models are defined with a generic name 'dominance'.

Electrical analysis: Fig. 1 shows an external short between the outputs A and B of two gates. Two detection conditions creating an unwanted conducting path from V_{DD} to GND, are possible. Under condition 1 (2), A is set to 0 (1) and B to 1 (0). Under condition 1 (2), we have $AB = 01$ (10) and the potentials are V_a^{01} and V_b^{01} (V_a^{10} and V_b^{10}). It is very important to note that under conditions 1 and 2 the conducting paths are different and the resulting potentials are different: $V_a^{01} \neq V_a^{10}$ and $V_b^{01} \neq V_b^{10}$.

Of course, the potentials V_a^{01}, V_b^{01}, V_a^{10} and V_b^{10} depend not only on the electrical parameters of the different transistors included in the path, but also on the value R_{sh} of the short as

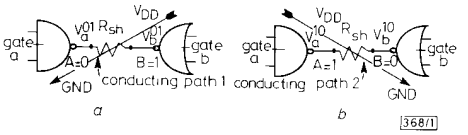

Fig. 1 *Two conditions of short detection and corresponding paths*
a Condition 1
b Condition 2

illustrated in Fig. 2. Three regions are defined according to the intersection with V_H and V_L: the noise margin of the cells connected to A and B. For high R_{sh} values (region 1), V_a^{01} is recognised as a logic 0 and V_b^{01} as a logic 1. The cell operates correctly and the fault cannot be detected. For intermediate values (region 3), V_b^{01} is correct and V_a^{01} (between V_H and V_L) does not correspond to any logical value. The cell does not operate correctly but the fault is not detectable using functional techniques. Finally, for low values (region 2), V_b^{01} is correct and V_a^{01} is recognised as a logic 1. Thus, in this case, the cell exhibits a faulty logical behaviour and the short can be detected using classical functional test techniques.

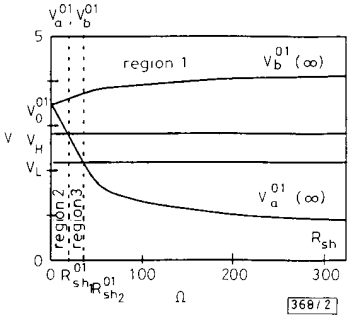

Fig. 2 *SPICE simulation of V_a and V_b against R_{sh} characteristics under condition 1*

Logical fault model: In region 2 of Fig. 2, V_a^{01} is recognised as a logic 1 whatever the value of the short resistance. That implies that the logical behaviour and consequently the fault model are the same whatever the value of the short resistance. Therefore, we can consider a nonresistive short to determine the fault model. Note that the resistance of the short determines the logical detectability of the fault (i.e. the region) but the fault model to be used is independent of this resistance value.

For a nonresistive short, V_a^{01} and V_b^{01} have the same value called V_0^{01}. The fault model depends not only on the relative location of V_0^{01} (condition 1) but also V_0^{10} (condition 2). As previously mentioned V_0^{01} and V_0^{10} are different due to the different conducting paths. They may be greater than V_H, smaller than V_L or somewhere in between implying nine different cases. Fig. 3 gives the values A^* and B^* of the shorted nodes for the two conditions of detection: $AB = 01$ and $AB = 10$. To construct the truth table for each case, we must consider the two other combinations which, of course, do not ensure the detection of the fault: $AB = 00$ implying $A^* = B^* = A = B = 0^*$ and $AB = 11$ implying $A^* = B^* = A = B = 1^*$.

It clearly appears that the classical wired-OR and wired-AND models correspond to cases 3 and 7. But they only constitute a *subset* of all the possible cases: 2 among 8. Note that case 5 corresponds to the limit when region 3 reaches the 0 resistance short ($V_L < V_0^{10} < V_H$ and $V_L < V_0^{01} < V_H$); it is not considered because it is not testable using voltage test techniques. Cases 1 and 9 have been recently reported by some authors [7] and compared to a vote configuration where