Testing the Temperature Limits of GaN-Based HEMT Devices

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(Invited Paper)

***Abstract*—The high temperature stability of AlGaN/GaN and lattice-matched InAlN/GaN heterostructure FETs has been evaluated by a stepped temperature test routine under large-signal operation. While AlGaN/GaN high-electron mobility transistors (HEMTs) have failed in an operating temperature range of 500 °C, InAlN/GaN HEMTs have been operated up to 900 °C for 50 h (in vacuum). Failure is thought to be still contact metallization stability related, indicating an extremely robust InAlN/GaN heterostructure configuration.**

***Index Terms*—GaN heterostructures, high-temperature electronics, InAlN/GaN high-electron mobility transistor (HEMT), reliability.**

I. Introduction

GALLIUM nitride (GaN)-based heterostructures have become the basis of a number of high-power electronic and optoelectronic device structures. Aluminum gallium nitride/gallium nitride (AlGaN/GaN) high-electron mobility transistors (HEMTs) have demonstrated state-of-the-art microwave power performance and are also promising candidates for the use in power electronics, microelectromechanical systems actuators, and sensors [1], [2]. In this configuration, they possess a large bandgap and large conduction band discontinuity, leading to high channel charge densities, 2-D electron gas (2DEG) transport properties with a high carrier mobility, and high breakdown fields. In addition, the material matrix and surface exhibit high thermal and chemical ceramic-like stability. The surface can form stable oxides, for example, gallium oxide (Ga_2O_3) which is being used in high temperature sensing up to 800 °C [3], [4].

AlGaN/GaN heterojunctions used in HEMT design are highly strained, and stress may therefore also influence the chemical/thermal stability of the films and interfaces, particularly in the presence of high temperatures and high electrical fields.

HEMT structures designed with this heterojunction commonly do not contain extrinsic doping. The countercharge to the channel charge is therefore a polarization-induced surface donor and may be located in surface traps. If this donor charge is not stable across the entire parameter field of operation, it may cause drift, current compression, or radio frequency (RF) power slump. Passivation and the properties of the dielectric/semiconductor interface, which may be considered an amorphous/crystalline heterojunction, are therefore rather critical. High lateral electrical fields may lead to lateral charge injection, compensating the surface donor in the gate/drain high field drift region and giving rise to the virtual gate effect [5], [6]. Furthermore, the growth of the GaN buffer layer commences usually on a highly disordered nucleation layer on substrates reaching from silicon carbide (SiC) and sapphire to (111) oriented silicon (Si).

The failure and reliability analysis of AlGaN/GaN HEMTs has therefore identified a large number of elements in the structure, which could cause degradation and failure [8]–[10]. A rather comprehensive overview can be found in [11]. Several studies have centered on the electrical degradation induced by the heterojunction and buffer layer properties on the one hand and surface- and gate-contact-related effects on the other hand [6], [8], [12]–[14]. Usually, activation energies are extracted from the operation at an elevated temperature. These have been rather low in the beginning (0.38 eV [15]) and mostly related to the high material dislocation and defect density. However, the material quality has been improved essentially and steadily, and recent experiments have indicated activation energies of up to around 3 eV [16], [17], indicating extremely long lifetimes under normal operating conditions and making the extraction of an activation energy already difficult.

However, during the past years, also the lattice-matched InAlN/GaN (indium aluminum nitride/gallium nitride) heterojunction has been used in HEMT design, the main motivation being a high 2DEG channel sheet charge density of 2.8×10^{13} cm^{-2} and the absence of mechanical stress in the

Manuscript received January 28, 2010; revised April 27, 2010; accepted August 6, 2010. Date of publication September 13, 2010; date of current version January 26, 2011. This paper was supported in part by the EU FP 6 program UltraGaN and in part by the FP 7 program MORGAN.

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Digital Object Identifier 10.1109/TDMR.2010.2072507

heterojunction [18]. The first initial experiments have also already indicated that this heterostructure and its surface are thermally, chemically, and electrically highly stable as could be demonstrated by short time operation at 1000 °C in vacuum [19]. The first analysis of degradation mechanisms has also already been reported [20].

The initial high temperature tests of InAlN/GaN HEMTs may indicate that the heterostructure material itself may not dominate reliability, robustness, or failure and may not limit the high temperature performance at present but that this is limited by the contact and passivation schemes used. Therefore, a temperature stepping test routine and setup has been developed to identify failure mechanisms within a reasonable time of testing. With this routine, AlGaN/GaN as well as InAlN/GaN HEMTs had been tested at 1 MHz under large-signal conditions at temperatures of up to failure.

II. Properties of Material and Technology

The robustness of an HEMT component may be dominated by the stability of its individual building blocks. The electrical, chemical, and thermal stability of these building blocks is usually analyzed separately before and during integration into a complete fabrication routine resulting, in cases, in rather standard material configurations, surface treatments, and processing sequences. They will be discussed shortly hereinafter.

A. Buffer Layer

GaN heterostructures for high-power electronic applications are usually grown with a gallium-face (Ga) orientation on SiC via an aluminum nitride (AlN) nucleation layer. It contains usually a high defect density and is partially compensated to obtain semi-insulating characteristics. The Debye temperature of GaN is around 750 °C, and no change in the bond strength is expected below this temperature [21]. In atmosphere, it can decompose into metallic Ga and nitrogen (N_2) above 650 °C [22], although mostly grown at 1000 °C by metal organic vapor phase epitaxy (MOCVD), when ammonia gas (NH_3) is used as a nitrogen precursor. Exposed to an atmosphere with a high H-radical density such as an H-plasma, a reduction is already observed above approximately 500 °C [23]. In oxygen, Ga_2O_3 will form widely, passivating the surface [24]. The thermal and chemical stability of the GaN buffer layer surface outside the active device mesa, usually by silicon nitride (Si_3N_4), will therefore strongly depend on its passivation properties. Changes in stoichiometry and loss of nitrogen will lead to residual conduction and irreversible degradation.

B. Ohmic Contacts

Ohmic contact metallization schemes have been intensively investigated during the 1990s, and a stack of titanium/aluminum/nickel (Ti/Al/Ni) covered with gold (Au) has emerged as the most used layer system, usually annealed at temperatures between 800 °C and 900 °C [25]. Many phases are formed between Ti and Al on the one hand and Al and Ni on the other hand in a temperature range above 900 °C, and the deposition in the layers will result in mixing and the formation of individual grains, initiated by the melting of Al at 680 °C.

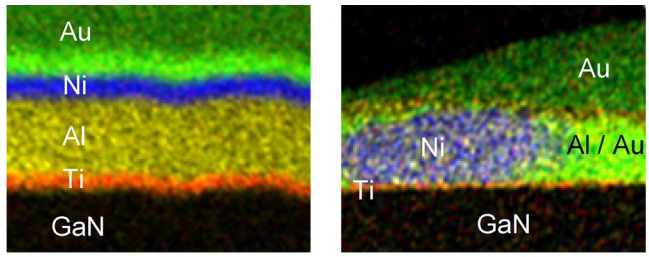

Fig. 1. Elemental energy dispersive X-ray spectroscopy maps of cross sections of ohmic contact stack (Ti/Al/Ni/Au, 10 nm/200 nm/40 nm/100 nm) on 8-nm InAlN/GaN without AlN spacer, after (left) RTA and (right) 30-min testing at 800 °C.

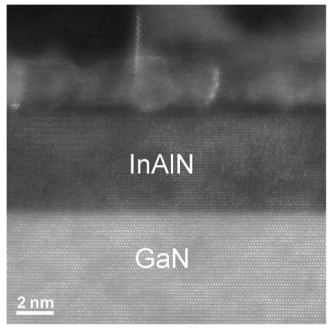

Fig. 2. HAADF STEM image of cross section of Ti/Al/Ni/Au contact annealed at 800 °C on InAlN/GaN heterostructure.

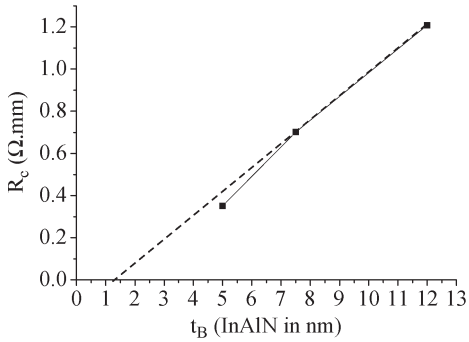

Fig. 3. Dependence of planar contact resistance as function of InAlN barrier thickness [27].

Fig. 1 shows a TEM cross section of an ohmic contact layer stack with 10-nm Ti, 200-nm Al, 40-nm Ni, and 100-nm Au overlays before and after annealing at 800 °C in nitrogen.

Intermixing is observed and also the accumulation of Au at the interface and at the contact edges. Nitride alloys like titanium nitride (TiN) formed at the interface are thought to generate the ohmic contact behavior [26]. However, in the case of InAlN, despite the intermixing, the alloys do not penetrate the barrier layer, as may be seen from Fig. 2. Here, no spike alloying or roughening of the interface is seen, indicating also that the alloy front will not penetrate to the heterointerface, and the polarization discontinuity generating the 2DEG channel will not be touched.

The contact resistance will therefore be formed by the metal/InAlN interface resistance and the series resistance reaching from the 2DEG channel across the InAlN barrier. Thus, the planar contact resistance displays a strong dependence on the barrier layer thickness, as shown in Fig. 3. The linear relationship indicates a negligible metal interface resistance

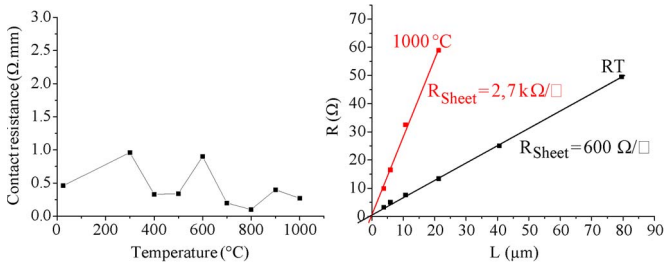

Fig. 4. (Left) Change of contact resistance with operating temperature. (Right) Extrapolation of planar contact resistance and sheet resistance from TLM measurements at measurement temperatures of RT and 1000 °C.

by tunneling. Thus, for a low planar contact resistance, a thin doped barrier is beneficial. However, the barrier layer is also part of the Schottky gate input, and a compromise needs to be found to limit the gate leakage and breakdown.

Thinner Al films in the stack will lead to phases of higher thermal stability, and higher annealing temperatures are needed to form low resistive contacts. Such a contact with the reduced Al-layer content and the substitution of the Au overlay by copper (Cu) (15-nm Ti/100-nm Al/40-nm Ni/100-nm Cu) annealed for 30 s at 900 °C have been operated up to 1000 °C in vacuum without a major change in the contact resistance, as seen with Fig. 4. The high temperature measurements have been taken with tungsten carbide (WC) needles, and the fluctuations in value may be due to measurement uncertainties. These uncertainties are caused by mechanical fluctuations in the chamber at high temperature. Moreover, the increase in the sheet resistance with temperature (see Fig. 4, right) was dominating at temperatures higher than 500 °C, which made the extrapolation of the contact resistance value from the TLM measurements marginal. Thus, it seems that these contacts can be operated up to their annealing temperature after stable phases are formed during the annealing process.

C. Schottky Contacts

The Schottky contact is one of the main sources of failure in FET devices. A number of metals have been investigated for AlGaN/GaN and InAlN/GaN HEMT structures, such as Ni, platinum (Pt), molybdenum (Mo), Cu, and iridium (Ir) [28]–[31] with Ni being the most commonly used contact metal. Usually, Au is used as a conductive overlay. On AlGaN, the thermal stability has frequently been investigated up to approximately 350 °C [8], [10], [16]. However, early experiments had also already indicated that the failure of the devices could be due to the degradation of the heterostructure rather than the gate diode [32]. The high stability of gate contacts is also confirmed by the use of Pt–AlGaN/GaN diodes in high temperature gas sensors of up to 800 °C in hydrogen/nitrogen (H_2/N_2) atmospheres [33]. In this paper, the temperature limit is thought to be reached by the alloy formation between the Pt Schottky metal and AlGaN semiconductor material, particularly Ga. In this paper, Ni contacts have been used.

InAlN/GaN HEMT structures were found to be stable at annealing temperatures of up to 1000 °C even with a 3-nm lattice-matched barrier tested under identical conditions as the one applied to the AlGaN/GaN HEMTs previously described, where the gate contact becomes ohmic [33].

It is particularly worth mentioning that the ohmic contact properties have not changed essentially, indicating no spike alloying even through the 3-nm barrier layer. Due to the thin barrier, the device operated in the semienhancement mode with a pinchoff voltage of −1.0 V, which remained also unchanged. Thus, also the interfacial polarization discontinuity had been preserved.

In the literature, many reports can be found indicating the degradation of Schottky diodes on AlGaN or InAlN well below the temperature range applied in this paper [10], and indeed, alloying may be expected, particularly with Ga- and indium (In)-forming grains with ohmic behavior, by tunnelling. Thus, stabilizing the barrier layer conditions is essential. This may also be indicated by a recent experiment reporting on AlGaN/GaN MISFET technology, where the gate metal had been deposited prior to the ohmic contact formation (and alloying at 850 °C) [35].

D. Passivation

The technical surface, being in contact with the atmosphere, will be oxygen terminated or will form a thin oxide film. Stoichiometric oxides are Ga_2O_3, aluminum oxide (Al_2O_3), and indium oxide (In_2O_3), the chemical activity of their surface being mainly generated by hydroxyl (OH) groups. The In oxide is the most unstable among the three and can be reduced to indium in H-plasmas or etched in wet solutions [36]. Ga oxide is considerably more stable and used in gas sensing up to 800 °C, as mentioned earlier. However, polycrystalline Ga_2O_3 in reducing atmosphere will become instable above 700 °C [37]. The most stable oxide is Al_2O_3 with a melting temperature of more than 2000 °C but can nevertheless be slowly etched in hot HCl [38] or in high density H-plasmas.

On AlGaN, the native oxide formed is only a few monolayers thin and a mixture of Al and Ga oxides [38]. In HEMT devices, it has also been used to stabilize the gate diode [39]. However, it has exhibited only limited stability under accelerated lifetime tests. The interface and bulk of the passivation materials are usually the location of the surface donor in AlGaN/GaN HEMTs [4], [5]. This surface donor is the state of the counter charge of the polarization discontinuity at the GaN interface, forming up to 40% of the 2DEG channel charge density, depending on the Al content of the barrier layer. A lateral charge injection into these states from the gate contact edge forms the virtual gate effect, which is the most severe instability in these devices [40]. It has therefore been the focus of a number of degradation studies [41]. Native oxides are thus usually removed from the surface by wet chemical cleaning prior to the deposition of a Si_3N_4 passivation layer in an H-rich plasma [42]. Other passivation materials are manganese oxide (MgO) [43], SiO_2 [44], and Al_2O_3 [45]. In most cases, the passivation layer is applied after the device is fully processed and after all contacts (including the gate contact) are deposited. The critical spot is therefore the gate metal edge on the strained AlGaN barrier layer toward the drain.

On InAlN, the weakly bonded In-oxide needs to be removed by chemical treatments, leaving an Al-rich oxide coverage. This surface can be further oxidized thermally to form a stable oxide

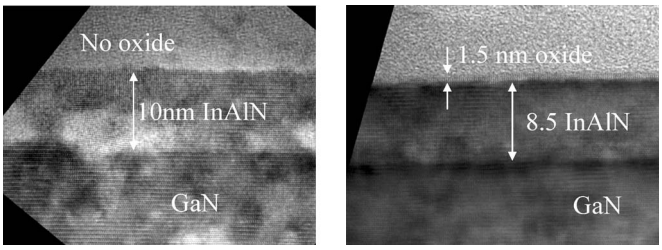

Fig. 5. TEM cross section of lattice-matched InAlN/GaN heterostructure with 10-nm barrier thickness. (Left) Heterostructure before oxidation. (Right) Heterostructure after oxidation at 800 °C in O_2 for 4 min [46].

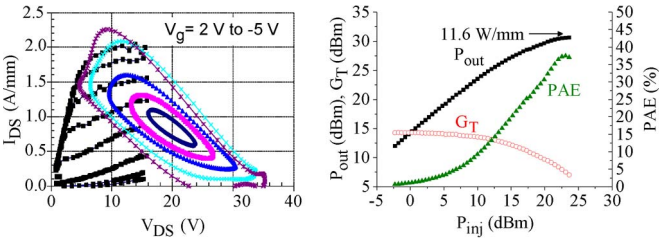

Fig. 6. Large-signal 4-GHz power performance of InAlN/GaN MISHEMT structure, including hard input overdrive conditions. Device data: $t_{\mathrm{InAlN}} = 10$ nm, $T_{\mathrm{oxide}} = 1.5$ nm, $L_G = 0.25$ μm, and $W_G = 2{*}50$ μm. In part after [48].

with a thickness of a few nanometers. Grown at 800 °C in O_2 for 4 min, the oxide is highly ordered and is approximately 1.5 nm thick (see Fig. 5).

The growth mechanism can be described by a diffusion-limited process [46], [47]. The growth rate will therefore slow down with growth time. Such native oxide films have been used in two cases: first, as an interfacial layer for passivation by PCVD Si_3N_4 and, second, as an oxide barrier in MISHEMT structures. In the MISHEMT structure, this gate contact may also be considered a dielectric-assisted Schottky contact, reducing the reverse gate leakage current by approximately four orders of magnitude [46].

The PCVD Si_3N_4-passivated MISHEMT configuration (with a self-aligned oxide gate recess [48]) has lead to a high input overdrive tolerance, drain-lag-free pulse performance, a full RF current drive above 2 A/mm (at 4 GHz), and a saturated output power density of 11.6 W/mm at a drain bias of 20 V. Fig. 6 (left) shows the output load line for various input power levels of up to saturation at a fixed load impedance superimposed on the cold point pulsed dc characteristics. This near-ideal performance is attributed to the absence of mechanical stress in the heterostructure and the high structural quality of the native oxide.

III. Temperature Cycling Measurements

The thermal oxidation properties and high contact annealing temperatures require indeed high thermal stability of the lattice-matched InAlN/GaN HEMT material system. In the case of AlGaN/GaN, the mechanical stress is thought to be one of the main causes for failure at RF under a high drain bias [49].

To test the high temperature limit of the InAlN/GaN system, a temperature stepping experiment has been designed, where the temperature has been ramped up in steps of 100 °C until failure (with a starting temperature chosen between room temperature (RT) and 500 °C). The time intervals had been chosen to 250 h at each temperature to obtain a final result within a reasonable testing time. In view of earlier experiments, the focus was on temperatures above 500 °C. The operating temperatures have been measured by thermocouples and calibrated by the melting point of specific metals. Nevertheless, temperature differences of up to 30 °C are estimated, caused by the WC needle probes (causing either a better thermal contact to the substrate by their pressure setting on the one hand or thermal losses due to their thermal conductivity on the other hand). Since, for a temperature range above 500 °C, no bonding and packaging technologies had been available, the devices had been tested individually on a chip with WC needles in vacuum and operated under 1-MHz large-signal conditions with the input driven between zero gate bias and pinchoff, as sketched in Fig. 7. The wave form of the output signal was recorded every 60 s, and the mean current $(I_{\mathrm{DS\,mean}})$ is calculated. In general, $I_{\mathrm{DS\,mean}}$ is less than half of the $I_{\mathrm{DS(VGS=0\,V)}}$ peak output current, with its ratio to the maximum open channel current being, in addition, determined by the pinchoff voltage.

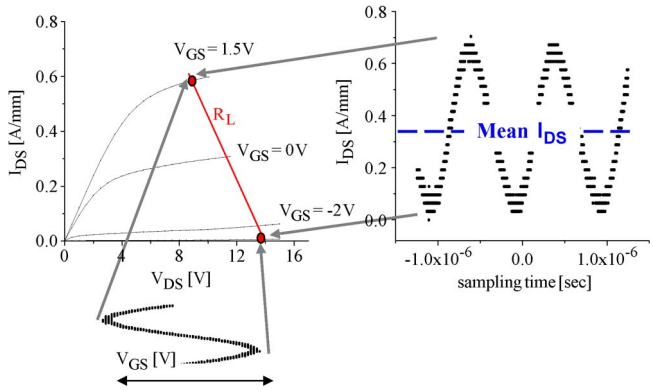

Fig. 7. Test arrangement of temperature stepping experiment. Input signal 1 MHz; bias point and amplitude adjusted as shown. Output terminated by R_L. Output waveform recorded every 60 s.

A. Cycling of AlGaN/GaN HEMTs

The AlGaN/GaN HEMT devices investigated in this paper have been supplied by Alcatel–Thales III–V Lab. Their structural and technological data can be summarized as follows. The heterostructure had been grown by MOCVD on a SiC substrate with a 1-nm AlN interfacial smoothing layer and an AlGaN barrier layer with 24% Al and a 22-nm thickness. Device isolation was achieved by helium (He) ion implantation. The source and drain contacts have been standard Ti/Al/Ni/Au contacts annealed at 900 °C, and the gate contact metal was Mo/Au. The gate length (L_g) was 0.25 μm. The devices were passivated by a low stress PCVD SiO_2/Si_3N_4 stack. The devices contained two parallel fingers in a Π arrangement $(W_{\mathrm{total}} = 200$ μm). The two sources were connected by a BCB bridge.

Fig. 8 illustrates the last temperature cycle before the failure at 500 °C. The testing had commenced at 300 °C. Thus, prior to this cycle, the device had already been stressed for 250 h at 300 °C and 250 h at 400 °C without noticeable changes. The peak drain current at RT $I_{D(\mathrm{VG=0\,V})}$ had been 1.4 A/mm,

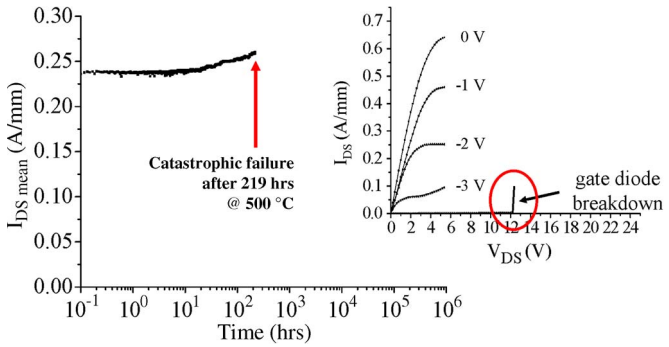

Fig. 8. Failure cycle of AlGaN/GaN HEMT device as described in the text. Operation conditions: $R_L = 500\ \Omega$, $V_{\rm DS} = 20$ V, $V_{\rm GS} = -3.6$–0 V, $f_{\rm in} = 1$ MHz, and temperature stepping from 300 °C to 500 °C.

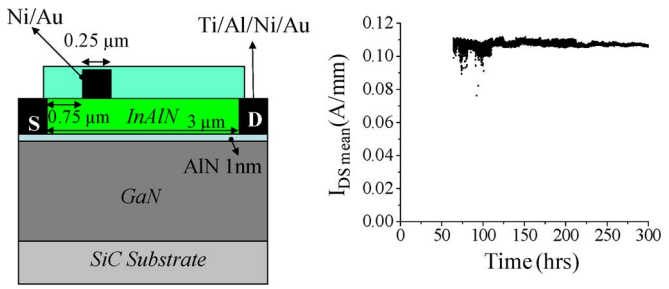

Fig. 9. (Left) Device cross section of the InAlN/GaN HEMTs. First- and second-generation devices differ only in the ohmic and gate contact metallization schemes. (Right) 500 °C test step of a typical InAlN/GaN device with lattice-matched barrier layer.

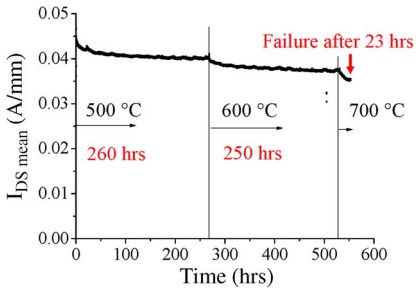

Fig. 10. Test cycles of InAlN/GaN HEMT up to failure. Failure occurred after 23 h at 700 °C.

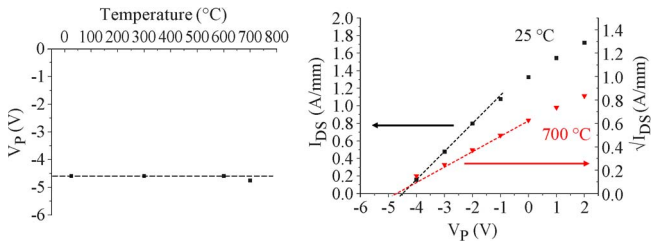

Fig. 11. (Left) Change of extracted pinchoff voltage (see right) at operating temperature of $L_g = 0.25$ μm FET. (Right) Extraction of pinchoff voltage at the onset of saturation: At 25 °C from linear transfer characteristic (high-mobility short-channel case and at 700 °C extraction from the square root plot of the transfer characteristics (low-mobility long-channel case).

reduced to approximately 0.65 A/mm at 500 °C. The device failed after 219 h due to gate shortage, as illustrated by the insert. This monitor measurement (see Fig. 8, right) could be taken shortly before the failure occurred. The raise in the mean output current during the last cycle could be associated with the increasing gate leakage.

Although the test is individual and does not allow any statistical interpretation, it had been a typical temperature regime of failure for these AlGaN/GaN devices, the failure being mostly gate diode breakdown related.

B. Cycling of InAlN/GaN HEMTs

The InAlN/GaN devices had been experimental device structures, usually processed on 1/4 of the 2-in diameter wafers. Heterostructures and buffer layers were grown by MOCVD on SiC substrates, the heterostructure containing a 1-nm AlN smoothing layer and a 7 to 10-nm-thick lattice-matched barrier. Device isolation has been obtained by dry etching (see Fig. 9, left). The contact technology was first based on the one used in AlGaN/GaN HEMTs and refined in a second-generation technology.

1) Devices Based on Conventional Metallization Systems: In the first generation of technology, the ohmic contacts were based on a layer stack usually employed in AlGaN/GaN HEMTs comprising of Ti/Al/Ni/Au (10 nm/200 nm/40 nm/100 nm) annealed at 850 °C for 2 min in N_2. The gate metallization has been Ni/Au (50 nm/100 nm). The final passivation had been by PCVD Si_3N_4.

Testing these device structures, usually, no change could be detected up to 500 °C, as may be seen from Fig. 9 (right), and no failure information could be extracted. Thus, usually, tests on InAlN/GaN devices have commenced directly at 500 °C. However, at such high temperatures, jitter from needle displacement is often observed, strongly influenced by traffic in the laboratory. The devices failed typically during the 700 °C cycle or at the beginning of the 800 °C cycle. In this temperature range, the output current (at $V_G = 0$ V) is typically reduced to 0.5 A/mm due to the decrease of the channel mobility (see discussion on ohmic contact behavior).

Fig. 10 shows the data of a device failing after 23 h at 700 °C. Again, the failure is sudden. The slight decrease in current at each temperature is thought to be related to the thermal transient of the furnace after temperature ramping.

Up to breakdown, no degradation of the pinchoff voltage is observed (see Fig. 11, right and left). Several effects may contribute to a change in the pinchoff voltage with temperature: 1) change of N_S caused by a change in polarization; 2) change of the Schottky barrier height; and 3) temperature-activated buffer layer leakage. The test indicates that the polarization discontinuity is not degraded and that no gate metal sinking has taken place even under the large-signal RF operation. In this case, the slight increase in the value of the pinchoff voltage (V_P) at 700 °C is related to a slight increase in the buffer layer leakage.

Fig. 12 shows the topography of the failed device. The failure mode is the breakup of the contact metallization, which seems only possible when liquid phases are formed. Damage seems to concentrate on the source ohmic contact region. It is however also seen that no metal ballup is observed in the unbiased part of the device. Thus, strong field-induced electromigration seems to be the triggering mechanism.

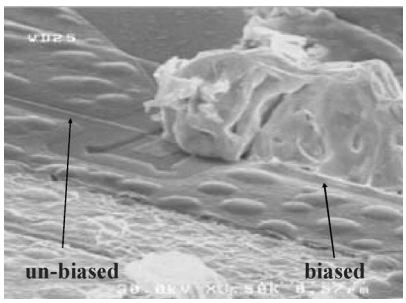

Fig. 12. Failure topology of the device discussed in Fig. 10.

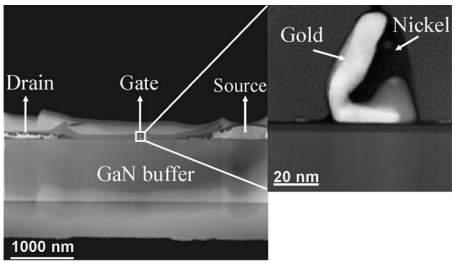

Fig. 13. HAADF STEM image of cross section of the gate, source/drain region after 30 min annealing at 800 °C.

On similar devices stored under identical conditions and thus simulating the unbiased case of temperature stressing, TEM cross sections have been taken. The ohmic contact areas reveal metallic intermixing as already seen after the ohmic contact annealing. However, the intermixing is also observed in the case of the Ni/Au gate metallization, as shown in Fig. 13. Au has moved and replaced Ni from the InAlN barrier layer surface, surprisingly not causing a gate diode breakdown, again indicating the high chemical stability of the barrier layer. On the other hand, in the identical planar structure, also the ohmic source drain contact behavior is generated by different metals and a distinctly different surface treatment. Nevertheless, in this configuration, Au is already highly mobile in the 700 °C range and is the prime failure source. The temperature stability limit of the heterostructure is not reached.

2) Devices With Refined Metallization Concept: For the second-generation devices, a metallization concept replacing Au as the conductive overlay metal by Cu has been developed. The melting temperatures of both metals are only slightly different (1064 °C versus 1084 °C for Au and Cu, respectively). However, Au is substantially more ductile below melting. In addition, the Al-layer thickness in the ohmic contact stack has been reduced by 50%. This has made a higher ohmic contact annealing temperature of 900 °C necessary. The gate contact metal was changed to Cu only.

Implementing these changes, the maximum temperature of the operation has been pushed up to 50 hrs operation at 900 °C. Fig. 14 shows the 800 °C cycle and 900 °C failure event. The recording is extremely noisy, indicating the difficulty to contact the metal pads reliably at this high temperature.

In Fig. 15, the output characteristics of the device in question are shown taken at RT before the test and at the end of the 800 °C test cycle, including the biasing condition and load line setting applied. The maximum output current level at RT

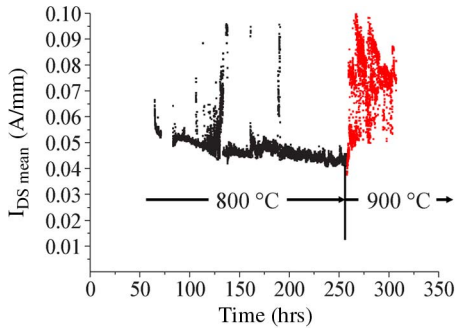

Fig. 14. High temperature cycling up to failure of InAlN/GaN HEMT with Cu-based metallization.

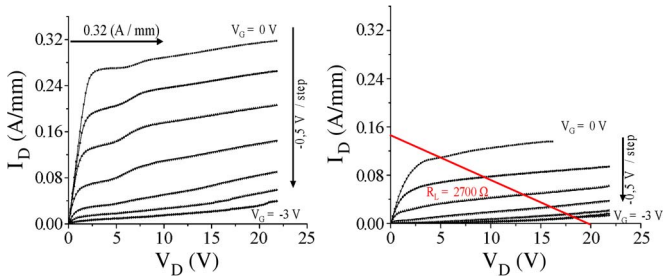

Fig. 15. Output characteristics of the InAlN/GaN HEMT device discussed in Fig. 14. (Left) Device at RT. Kink in the output characteristics is related to charge injection into the buffer, leading to a shift in the internal gate voltage. (Right) Device with 800 °C load line selected for 800 °C operation.

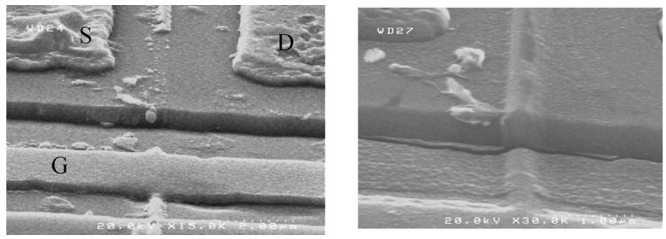

Fig. 16. Topography of InAlN/GaN HEMT after failing at 900 °C large-signal RF operation. (Left) After removal of Si_3N_4 passivation. (Right) Passivated.

was 0.32 A/mm (at $V_G = 0$ V in semi-enhancement mode, $t_{\mathrm{InAlN}} = 7$ nm). The reduction of approximately 50% is mainly reflecting the change in the 2DEG channel sheet resistance and, thus, the carrier mobility and not related to a degradation of the contact resistances as previously discussed. As can be seen, some degradation of the output signal level is already noticeable during the 800 °C cycles, which is thought to be mainly caused by residual charge injection into the buffer layer and the residual conduction activated in the buffer layer. Again, no major change in the pinchoff voltage is observed. Thus, also in this case, it seems that the stability limit of the heterostructure itself has not been reached yet.

The topography of the failed device is illustrated in Fig. 16. Two failure sources can be identified. On the right-hand side rupture of the Si_3N_4, the passivation at the mesa edge can be seen; on the left side, the electromigration of the gate metallization is evident, but no major breakup of the metallization like in the case of the Au overlay is observed. The testing temperature (900 °C) is already close to the melting temperature of Cu (1084 °C), and the electromigration is therefore expected to be

amplified. Moreover, the unbiased stored devices did not show any kind of degradation when testing at RT after the heating cycle. Therefore, the degradation mechanism is connected to the electromigration.

IV. Discussion and Conclusion

GaN-based heterostructures in their AlGaN/GaN wide bandgap configuration possess high chemical and thermal stability and are therefore thought to be ideal candidates for robust high-power operation and operation at extremely high temperatures. Many technological details have been refined during the past, and the material quality essentially improved. The reliability and time of failure have been improved accordingly. Activation energies of accelerated lifetime tests have reached 3 eV but are still lower than the bandgap energies. Nevertheless, with such activation energies, extremely high lifetimes are expected for RT operation, and even at an elevated temperature, the extrapolation becomes difficult. Furthermore, the degradation and failure mechanisms may change for operation at an elevated temperature, and feedback to RT operation may be inconclusive. All material structures are highly polar and essentially undoped, and many studies have centered around the stability of the polarization-induced channel charge and the related donor counter charge located at the surface or within the passivation layer and, in this paper, particularly the piezopart generated by the mechanical stress of the AlGaN barrier layer. In fact, the mechanical stress is thought to be a main source of degradation under large-signal RF operation at high electrical fields.

An alternative to the common AlGaN/GaN heterostructure is the lattice-matched InAlN/GaN heterostructure, and other degradation and failure mechanisms may dominate. Early experiments with short time curve tracer FET operation of up to 1000 °C in vacuum had already indicated the exceptional thermal stability of the heterojunction. Thus, failure and reliability may be dominated by other elements in the structure than the material itself, still leaving room for improvement by their optimization. To distinguish whether the dominant failure sources are related to the heterostructure material properties or the device fabrication technology adopted from the AlGaN/GaN counterpart, the previously discussed stepped temperature experiment was designed, testing the device up to failure within a reasonable time frame. Changes in the performance were, in general, (after the optimization of the processing routine) only observed for operation above 500 °C (within a 250-h time frame). Since no standard test equipment has been available for RF power operation at such high temperatures, the testing had to be confined to 1-MHz large-signal operation contacted by WC needles. The results may be summarized as follows.

1) Using the standard metallization schemes of AlGaN/GaN for the ohmic and gate contacts for InAlN/GaN HEMTs, the dominant temperature range for failure was between 700 °C and 800 °C. The dominant failure mode had been diffusion, intermixing, and electromigration caused by the Au overlay. The failure has, in general, resulted in the total breakup of the metallization pattern. Such catastrophic damage was not observed for unbiased devices.
2) The redesign of the metallization schemes based on Cu as the conductive overlay has resulted in operation of up to 900 °C. The failure could be associated with Cu electromigration. This is not surprising since this is only approximately 150 °C below its melting point.
3) Cracks in the Si_3N_4 passivation layer at the mesa edge after 900 °C operation indicated also that an uncontrolled stress had developed between the passivation and the semiconductor surface.
4) Up to the failure, only minor changes in the pinchoff voltage have been observed even for the semienhancement mode of the operation. Thus, the polarization discontinuity between GaN and InAlN has remained stable throughout all tests. The changes could be associated with the buffer layer leakage at high temperatures. No gate sinking effect could be observed.
5) The thermal/chemical stability of the lattice-matched InAlN/GaN material system seems indeed outstanding. The 3-nm-thin barrier layers (with a thickness close to the tunneling limit) had been highly stable throughout the entire range of temperature, acting as barrier layer to the gate metallization as well as the passivation of the free surface. (The InAlN/GaN devices used in Section III contained barrier layers between 7 and 10 nm.)

Certainly, the test routine chosen relies on individual devices and is destructive. Nevertheless, the results have indicated that, even for temperatures above 500 °C and up to 900 °C, the failure is dominated by the device processing technology and not the heterostructure material stability. This picture is not so clear for the strained AlGaN/GaN heterosystem, where the mechanical stress may lead to premature material degradation.

How far the high temperature performance of these FET devices is reflected in their high-power operation under ambient conditions is not clear at present. The mobility of the channel electrons decreases with temperature due to increased phonon scattering, reducing the dc current levels (see, for example, Fig. 15) and RF gain at high frequencies. Furthermore, the buffer layer leakage needs to be suppressed also at high temperatures; otherwise, this will seriously impair the RF performance. Assuming that the saturated velocity will be less affected, high dc current levels and RF gain may be maintained by a reduced gate length.

Devices are usually operated with a safe margin from breakdown, induced by high electrical fields, high junction temperatures, and also effects like electrochemical corrosion. In this paper, the temperature is only one criterion. In this paper, the devices had not been operated under forward gate bias conditions and not deeply in the subthreshold regime, and dispersion effects at large-signal high-frequency operation, like the microwave power slump, have not been addressed. Certainly, more elaborate testing routines are needed. Testing in a temperature range above 500 °C represents a new field, and equipment as well as device technologies need optimization and refinement. This paper is thought to stimulate further experiments in this new regime and serve as a feasibility study for ultrahigh temperature applications out of reach for other semiconductor materials presently.

ACKNOWLEDGMENT

The authors would like to thank I. Daumiller and F. Medjdoub for their early contributions to this paper and W. Ebert and Y. Men for their technological support for the device processing. The authors would also like to thank the partners of the EU FP 6 program UltraGaN and the FP 7 program MORGAN for their contributions to this paper.

REFERENCES

[1] Y.-F. Wu, M. Moore, A. Saxler, T. Wisleder, and P. Parikh, "40-W/mm double field-plated GaN HEMTs," in *Proc. 64th Device Res. Conf.*, Jun. 2006, pp. 151–152.

[2] T. Zimmermann, M. Neuburger, P. Benkart, F. J. Hernandez-Guillen, C. Pietzka, M. Kunze, I. Daumiller, A. Dadgar, A. Krost, and E. Kohn, "Piezoelectric GaN sensor structures," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 309–312, May 2006.

[3] J. Song, W. Lu, J. S. Flynn, and G. R. Brandes, "Pt–AlGaN/GaN Schottky diodes operated at 800 °C for hydrogen sensing," *Appl. Phys. Lett.*, vol. 87, no. 13, pp. 133 501-1–133 501-3, Sep. 2005.

[4] K. J. Duxstad, E. E. Haller, and K. M. Yu, "High temperature behavior of Pt and Pd on GaN," *J. Appl. Phys.*, vol. 81, no. 7, pp. 3134–3137, Apr. 1997, DOI:10.1063/1.364091.

[5] M. Neuburger, I. Daumiller, M. Kunze, M. Seyboth, T. Jenkins, J. Van Nostrand, and E. Kohn, "Influence of polarization on the properties of GaN based FET structures," *Phys. Stat. Sol. (C)*, vol. 0, no. 6, pp. 1919–1939, Sep. 2003.

[6] I. Daumiller, D. Theron, C. Gaquière, A. Vescan, R. Dietrich, A. Wieszt, H. Leier, R. Vetury, U. K. Mishra, I. P. Smorchkova, S. Keller, C. Nguyen, and E. Kohn, "Current instabilities in GaN-based devices," *IEEE Electron Device Lett.*, vol. 22, no. 2, pp. 62–64, Feb. 2001.

[7] A. Dadgar, M. Poschenrieder, A. Reiher, J. Blasing, J. Christen, A. Krtschil, T. Finger, T. Hempel, A. Diez, and A. Krost, "Reduction of stress at the initial stages of GaN growth on Si(111)," *Appl. Phys. Lett.*, vol. 82, no. 1, pp. 28–30, Jan. 2003, DOI:10.1063/1.1534940.

[8] G. Meneghesso, G. Verzellesi, F. Danesin, F. Rampazzo, F. Zanon, A. Tazzoli, M. Meneghini, and E. Zanoni, "Reliability of GaN high-electron-mobility transistors: State of the art and perspectives," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 2, pp. 332–343, Jun. 2008.

[9] R. Menozzi, "Reliability of GaN-based HEMT devices," in *Proc. COMMAD*, Jul. 28–Aug. 1, 2008, pp. 44–50.

[10] J. Würfl, V. Abrosimova, J. Hilsenbeck, E. Nebauer, W. Rieger, and G. Trankle, "Reliability considerations of III-nitride microelectronic devices," *Microelectron. Reliab.*, vol. 39, no. 12, pp. 1737–1757, Dec. 17, 1999, DOI: 10.1016/S0026-2714(99)00181-X.

[11] R. Quay, *Gallium Nitride Electronics*. Berlin, Germany: Springer-Verlag, 2008, ch. 7.

[12] G. Verzellesi, M. Faqir, A. Chini, F. Fantini, G. Meneghesso, E. Zanoni, F. Danesin, F. Zanon, F. Rampazzo, F. A. Marino, A. Cavallini, and A. Castaldini, "False surface-trap signatures induced by buffer traps in AlGaN–GaN HEMTs," in *Proc. IEEE Int. Reliab. Phys. Symp.*, Apr. 26–30, 2009, pp. 732–735.

[13] S. J. Pearton, J. C. Zolper, R. J. Shul, and F. Ren, "GaN: Processing, defects, and devices," *J. Appl. Phys.*, vol. 86, no. 1, pp. 1–78, Jul. 1999, DOI:10.1063/1.371145.

[14] G. Meneghesso, F. Rampazzo, P. Kordos, G. Verzellesi, and E. Zanoni, "Current collapse and high-electric-field reliability of unpassivated GaN/AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 2932–2941, Dec. 2006.

[15] R. Gaska, Q. Chen, J. Yang, A. Osinsky, M. Asif Khan, and M. S. Shur, "High-temperature performance of AlGaN/GaN HFETs on SiC substrates," *IEEE Electron Device Lett.*, vol. 18, no. 10, pp. 492–494, Oct. 1997.

[16] T. Ohki, T. Kikkawa, Y. Inoue, M. Kanamura, N. Okamoto, K. Makiyama, K. Imanishi, H. Shigematsu, K. Joshin, and N. Hara, "Reliability of GaN HEMTs: Current status and future technology," in *Proc. IEEE Int. Reliab. Phys. Symp.*, Apr. 26–30, 2009, pp. 61–70.

[17] S. Lee, R. Vetury, J. D. Brown, S. R. Gibb, W. Z. Cai, J. Sun, D. S. Green, and J. Shealy, "Reliability assessment of AlGaN/GaN HEMT technology on SiC for 48 V applications," in *Proc. IEEE IRPS*, Apr. 27–May 1, 2008, pp. 446–449.

[18] J. Kuzmik, "Power electronics on InAlN/(In)GaN: Prospect for a record performance," *IEEE Electron Device Lett.*, vol. 22, no. 11, pp. 510–512, Nov. 2001.

[19] F. Medjdoub, J.-F. Carlin, M. Gonschorek, E. Feltin, M. A. Py, D. Ducatteau, C. Gaquière, N. Grandjean, and E. Kohn, "Can InAlN/GaN be an alternative to high power/high temperature AlGaN/GaN devices?" in *IEDM Tech. Dig.*, Dec. 11–13, 2006, pp. 1–4.

[20] J. Kuzmik, G. Pozzovivo, C. Ostermaier, G. Strasser, D. Pogany, E. Gornik, J.-F. Carlin, M. Gonschorek, E. Feltin, and N. Grandjean, "Analysis of degradation mechanisms in lattice-matched InAlN/GaN high-electron-mobility transistors," *J. Appl. Phys.*, vol. 106, no. 12, p. 124 503, Dec. 2009, DOI:10.1063/1.3272058.

[21] M. O. Manasreh, Ed., *GaN and Related Materials (Optoelectronic Properties of Semiconductor and Superlattices)*. New York: Gordon and Breach, 1997.

[22] A. Pisch and R. Schmid-Fetzer, "In situ decomposition study of GaN thin films," *J. Cryst. Growth*, vol. 187, no. 3/4, pp. 329–332, May 15, 1998, DOI: 10.1016/S0022-0248(98)00006-2.

[23] P. W. May, H. Y. Tsai, W. N. Wang, and J. A. Smith, "Deposition of CVD diamond onto GaN," *Diamond Related Mater.*, vol. 15, no. 4–8, Diamond 2005, pp. 526–530, Apr.–Aug. 2006, DOI: 10.1016/j.diamond.2005.11.036.

[24] S. D. Wolter, S. E. Mohney, H. Venugopalan, A. E. Wickenden, and D. D. Koleske, "Kinetic study of the oxidation of gallium nitride in dry air," *J. Electrochem. Soc.*, vol. 145, no. 2, pp. 629–632, Feb. 1998, DOI:10.1149/1.1838314.

[25] S. Ruvimov, Z. Liliental-Weber, J. Washburn, K. J. Duxstad, E. E. Haller, Z.-F. Fan, S. N. Mohammad, W. Kim, A. E. Botchkarev, and H. Morkoc, "Microstructure of Ti/Al and Ti/Al/Ni/Au Ohmic contacts for n-GaN," *Appl. Phys. Lett.*, vol. 69, no. 11, pp. 1556–1558, Sep. 1996, DOI:10.1063/1.117060.

[26] H. Cordes and Y. A. Chang, "Interfacial reactions and electrical properties of Ti/n-GaN contacts," *MRS Internet J. Nitride Semicond. Res.*, vol. 2, 1997, Article 2. [Online]. Available: http://www.mrs.org/s_mrs/doc.asp?CID=26415&DID=321052

[27] F. Medjdoub, J.-F. Carlin, M. Gonschorek, E. Feltin, M. A. Py, M. Knez, D. Troadec, C. Gaquière, A. Chuvilin, U. Kaiser, N. Grandjean, and E. Kohn, "Barrier layer downscaling of InAIN/GaN HEMTs," in *Proc. 65th Annu. Device Res. Conf.*, Jun. 18–20, 2007, pp. 109–110.

[28] A. C. Schmitz, A. T. Ping, M. Asif Khan, Q. Chen, J. W. Yang, and I. Adesida, "Metal contacts to n-type GaN," *J. Electron. Mater.*, vol. 27, no. 4, pp. 255–260, Apr. 1998, DOI: 10.1007/s11664-998-0396-5.

[29] A. C. Schmitz, A. T. Ping, M. Asif Khan, Q. Chen, J. W. Yang, and I. Adesida, "Schottky barrier properties of various metals on n-type GaN," *Semicond. Sci. Technol.*, vol. 11, no. 10, pp. 1464–1467, Oct. 1996, DOI: 10.1088/0268-1242/11/10/002.

[30] H. F. Sun, A. R. Alt, and C. R. Bolognesi, "Submicrometer copper T-gate AlGaN/GaN HFETs: The gate metal stack effect," *IEEE Electron Device Lett.*, vol. 28, no. 5, pp. 350–353, May 2007.

[31] E. Arslan, S. Butun, and E. Ozbay, "Leakage current by Frenkel–Poole emission in Ni/Au Schottky contacts on $Al_{0.83}In_{0.17}N$/AlN/GaN heterostructures," *Appl. Phys. Lett.*, vol. 94, no. 14, p. 142 106, Apr. 2009, DOI:10.1063/1.3115805.

[32] I. Daumiller, C. Kirchner, M. Kamp, K. J. Ebeling, and E. Kohn, "Evaluation of the temperature stability of AlGaN/GaN heterostructure FETs," *IEEE Electron Device Lett.*, vol. 20, no. 9, pp. 448–450, Sep. 1999.

[33] F. Medjdoub, M. Alomari, J.-F. Carlin, M. Gonschorek, E. Feltin, M. A. Py, N. Grandjean, and E. Kohn, "Barrier-layer scaling of InAlN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 29, no. 5, pp. 422–425, May 2008.

[34] J. Song and W. Lu, "Operation of Pt/AlGaN/GaN-heterojunction field-effect-transistor hydrogen sensors with low detection limit and high sensitivity," *IEEE Electron Device Lett.*, vol. 29, no. 11, pp. 1193–1195, Nov. 2008.

[35] O. I. Saadat, J. W. Chung, E. L. Piner, and T. Palacios, "Gate-first AlGaN/GaN HEMT technology for high-frequency applications," *IEEE Electron Device Lett.*, vol. 30, no. 12, pp. 1254–1256, Dec. 2009.

[36] H.-J. Cho, S.-Y. Lee, J.-W. Lee, J.-Y. Lee, S.-H. Chon, Y.-S. Choi, Y.-C. Park, J.-S. Kim, K.-S. Kim, D.-U. Choi, and K.-T. Lim, "Etchant composition for indium oxide layer and etching method using the same," U.S. Patent 7 329 365 B2, Feb. 12, 2008.

[37] M. Fleischer, L. Hollbauer, and H. Meixner, "Effect of the sensor structure on the stability of Ga_2O_3 sensors for reducing gases," *Sens. Actuators B, Chem.*, vol. 18, no. 1–3, pp. 119–124, Mar. 1994, DOI: 10.1016/0925-4005(94)87069-1.

[38] R. Sohal, P. Dudek, and O. Hilt, "Comparative study of NH_4OH and HCl etching behaviours on AlGaN surfaces," *Appl. Surf. Sci.*, vol. 256, no. 7, pp. 2210–2214, Jan. 15, 2010, DOI: 10.1016/j.apsusc.2009.09.075.

[39] J. L. Jimenez and U. Chowdhury, "X-band GaN FET reliability," in *Proc. IEEE IRPS*, Apr. 27–May 1, 2008, pp. 429–435.

[40] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the dc and RF characteristics of AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 560–566, Mar. 2001.
[41] R. Trew, D. Green, and J. Shealy, "AlGaN/GaN HFET reliability," *IEEE Microw. Mag.*, vol. 10, no. 4, pp. 116–127, Jun. 2009.
[42] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 21, no. 6, pp. 268–270, Jun. 2000.
[43] J. Kim, B. Gila, R. Mehandru, J. W. Johnson, J. H. Shin, K. P. Lee, B. Luo, A. Onstine, C. R. Abernathy, S. J. Pearton, and F. Ren, "Electrical characterization of GaN metal oxide semiconductor diodes using MgO as the gate oxide," *J. Electrochem. Soc.*, vol. 149, no. 8, pp. G482–G484, Aug. 2002, DOI:10.1149/1.1489689.
[44] G. Simin, A. Koudymov, H. Fatima, J. Zhang, J. Yang, M. Asif Khan, X. Hu, A. Tarakji, R. Gaska, and M. S. Shur, " SiO_2/AlGaN/InGaN/GaN MOSDHFETs," *IEEE Electron Device Lett.*, vol. 23, no. 8, pp. 458–460, Aug. 2002.
[45] F. Medjdoub, N. Sarazin, M. Tordjman, M. Magis, M. A. di Forte-Poisson, M. Knez, E. Delos, C. Gaquière, S. L. Delage, and E. Kohn, "Characteristics of Al_2O_3/AlInN/GaN MOSHEMT," *Electron. Lett.*, vol. 43, no. 12, pp. 691–692, Jun. 7, 2007.
[46] M. Alomari, A. Chuvilin, L. Toth, B. Pecz, J.-F. Carlin, N. Grandjean, C. Gaquière, M-A. di Forte-Poisson, S. Delage, and E. Kohn, "Thermal oxidation of lattice matched InAlN/GaN heterostructures," *Phys. Stat. Sol. (C)*, vol. 7, no. 1, pp. 13–16, Jan. 2010.
[47] T. Hashizume, S. Ootomo, S. Oyama, M. Konishi, and H. Hasegawa, "Chemistry and electrical properties of surfaces of GaN and GaN/AlGaN heterostructures," *J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct.*, vol. 19, no. 4, pp. 1675–1681, Jul. 2001.
[48] M. Alomari, F. Medjdoub, J.-F. Carlin, E. Feltin, N. Grandjean, A. Chuvilin, U. Kaiser, C. Gaquière, and E. Kohn, "InAlN/GaN MOSHEMT with self-aligned thermally generated oxide recess," *IEEE Electron Device Lett.*, vol. 30, no. 11, pp. 1131–1133, Nov. 2009.
[49] J. Joh and J. A. del Alamo, "Critical voltage for electrical degradation of GaN high-electron mobility transistors," *IEEE Electron Device Lett.*, vol. 29, no. 4, pp. 287–289, Apr. 2008.

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In 1978, she was with the Central Research Laboratory of Thomson-CSF. She is currently with Alcatel-Thales III–V Lab, Marcoussis, France, where she manages the team responsible for the "epitaxial growth of wide bandgap materials." She successfully coordinated the Brite–Euram project RAINBOW (Gallium Aluminium Indium Nitride for Multicolor Sources) and other national GaN-based projects. She is involved in the MOVPE epitaxy of III–V compounds. She is interested in the growth, characterization, and device applications of a variety of ternary compounds. Her past achievements include the growth of high-power 94-GHz InP Gunn diodes, the first realization of a linear array of a thousand p-i-n photodiodes at 1.72 μm for the SPOT IV satellite, 980-nm high-power laser diodes based on strained quantum wells, and GaInAs/GaInAsP/GaInP heterostructures or GaInP/GaAs-based HBT epitaxial structures for high-power S-band and X-band amplifiers. She has authored or coauthored more than 100 papers and several patents. She has been involved for several years in many French or European projects such as HERO'S, MIGHT, ISCE-MOVPE, EURONIM (Brite) or AGHETA (IST), Korrigan, HYPHEN, UltraGaN, and MORGaN.

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Christian Dua received the Engineer degree in physics from the University of Clermont-Ferrand, Clermont-Ferrand, France, in 1980.

He worked in different units of the Thomson-CSF Group (previous name of Thales) in the field of microwave devices and optoelectronic components. From 1982 to 1996, he gained experience in crystal growth and physical and electrical characterization of semiconductor materials. Since 1997, he has been with the research unit of Alcatel-Thales III–V Lab, Marcoussis, France, which is called TRT, where is participating in the development of wide bandgap semiconductor technologies. His current activities include the study of the reliability of GaN HEMTs.

Andrey Chuvilin, photograph and biography not available at the time of publication.

David Troadec, photograph and biography not available at the time of publication.

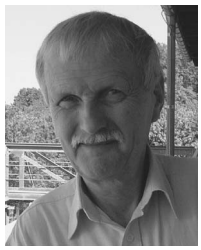
Christophe Gaquière received the Ph.D. degree in electronic from the University of Lille, Lille, France, in 1995.

From 2003 up to 2007, he was responsible for the microwave characterization part of the common laboratory between TRT and the Institut d'Electronique de Microélectronique et de Nanotechnology (IEMN), Lille University of Science and Technology, Villeneuve d'Ascq, France, which focuses on wide bandgap semiconductors (GaN, SiC, and diamond). He is currently a Professor with the Lille University of Science and Technology, where he carries out his research activity in the IEMN. He is also currently in charge of the silicon millimeter-wave advanced technologies part of the common laboratory between ST microelectronics and IEMN. The topics concern the design, fabrication, and characterization of HEMTs and HBT devices. He works on GaAs, InP, and metamorphic HEMTs, and he is currently involved in GaN activities. His main activities include microwave characterizations (small and large signals between 1 and 220 GHz) in order to correlate the microwave performances with the technological and topology parameters. His current activities include mainly the investigation of 2-D electronic plasmons for terahertz solid-state GaN-based detectors and emitters, AlGaN/GaN nanowires for microwave applications, and MEMS activities based also on GaN. He is the author or coauthor of more than 100 publications and 200 communications. He has collaborations with the U.S., Russia, Germany, Italy, Spain, Austria, and U.K. in the frame of European contracts.

Ute Kaiser, photograph and biography not available at the time of publication.

Sylvain L. Delage received the Ph.D. degree from University Paris VII, Paris, France, in 1985, for his work carried out at CNET-Meylan on the demonstration of the first monolithic $Si/CoSi_2/Si$ metal base transistor grown by molecular beam epitaxy.

For two years, he was a Research Staff Member with the IBM T. J. Watson Research Center, where he did participate to the first demonstration of Si/SiGe HBTs, which were later on developed and manufactured worldwide by major semiconductor companies. In 1988, he was with the Central Research Laboratory of Thomson-CSF, now Thales Research and Technology, where he was in charge of the Power Transistor Programme for Microwave Applications which is based on InGaP/GaAs HBT devices and microwave circuits. This technology has been successfully transferred to UMS. He is currently with the Alcatel-Thales III–V Lab, Marcoussis, France, where he is in charge of the Microelectronics Group, which includes about 25 permanent scientists working on GaN and InP materials and devices. These technologies are mostly developed for wireless telecommunications, professional electronics, optical fiber networks, and power switching electronics. He has been in charge or strongly involved in various European or French projects: AIMS, Andro, Korrigan, GAMMA, UltraGaN, MIGHT, EURONIM, TERAGAN, MORGaN, TOPOGaN, E3Car, Attitude 4G+, etc. He had contributed to more than 100 publications and 25 international patents.



Erhard Kohn (M'89) was born in Berlin, Germany, in 1943. He received the Ph.D. (Dr.-Ing.) degree from the Technical University of Aachen, Aachen, Germany, in 1975.

After two years of postdoctoral studies at the University of Newcastle upon Tyne, Newcastle upon Tyne, U.K., and many years in the industry in Germany, France, and the U.S., he joined the University of Ulm, Ulm, Germany, as a Full Professor and Director of the Institute of Electron Devices and Circuits in 1989, where he also serves as the Director of the Microelectronics Technology Center of the Engineering Faculty. His research activities include the design and technology of advanced electronic device structures in a number of semiconductors like Si, GaAs, InP, and, recently, III-nitride heterostructures and diamond for high-temperature, high-power, and high-speed applications. This is accompanied by work on advanced packaging technologies and MEMS sensor and actuator devices, mainly based on CVD diamond for RF applications and applications in electrochemistry and life science. He has been a Visiting Fellow with the University of Wales, Cardiff, U.K., the Norwegian Institute of Technology, Trondheim, Norway, the Cornell University, Ithaca, NY, the National Cheng Kung University, Tainan, Taiwan, and the Air Force Research Laboratories, Dayton, OH, and has been an Adjunct Professor of physics with the New Jersey Institute of Technology, Newark, NJ. He is the Director of the Steinbeis Technology Transfer Centre "Semiconductor Devices." His activities have led to two spin-off companies, Gesellschaft für Diamantprodukte and MicroGaN.

Dr. Kohn has served as an IEEE EDS Distinguished Lecturer.