128-Channel Fully Differential Digital Neural Recording and Stimulation Interface

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***Abstract*— We present a fully differential 128-channel integrated neural interface. It consists of an array of 8×16 low-power low-noise signal recording and generation channels for electrical neural activity monitoring and stimulation, respectively. The recording channel has two stages of signal amplification and conditioning with a programmable gain of 54dB to 73dB, and a fully differential 8-bit column-parallel successive approximation (SAR) analog-to-digital converter (ADC). The design is implemented in a 0.35μm CMOS technology with the channel pitch of 200μm. The total measured power consumption of each recording channel including the SAR ADC is 15.5μW. The measured input referred noise is 6.08μV_{rms} over a 5kHz bandwidth.**

I. Introduction

There is a great demand for miniature implantable integrated microsystems that treat neurological disorders such as epilepsy, depression and Parkinson's disease. Brain neural activity recording facilitates early diagnosis. Neural stimulation may prevent the onset of detrimental neural activity such as that resulting in tremor.

Extracellular action potentials have a wide dynamic range with signal amplitudes approximately between 20μV to 5mV [1]–[3]. Most of the neural activity lies within the frequency range of 0.1Hz to 5kHz. The dynamic range of the neural recording interface is approximately 48dB requiring 8 bits of resolution.

In recent years, there has been a significant progress in developing low-noise low-power integrated neural interfaces. Generally single-ended designs suffer from interference from any digital circuits implemented on the same chip. Fully differential architectures are advantageous as they suppress common-mode noise and interference from the power supply and on-chip digital circuits.

A number of fully differential single-channel implementations have been reported where the channel area is not a significant constraint [4], [5]. A one-stage recording channel with programmable cutoff frequency is described in [4] where signal distortion is minimized. A two-stage recording channel is reported in [5] where high gain is achieved by using one OTA in the first stage and three OTAs in the second stage.

Multi-channel fully differential designs allow for spatial neural recording and stimulation at multiple sites [6]–[10]. A 16-channel recording interface without ADCs is presented in [6]. The design in [7] has 16 channels of bandpass amplifiers with $\Delta\Sigma$ ADCs that occupy an area of 3mm×3mm and consume 1.8mW of power. A 128-channel wireless neural recording interface is reported in [8] where signal quantization, spike detection and sorting, and wireless telemetry are performed on-chip. A low power consumption of 6mW is obtained within the die area of 8.8mm×7.2mm. A 64-channel programmable deep brain stimulator with 8-channel neural amplifiers and a logarithmic ADC is developed in [9]. A 6.5mm×6.5mm 128-channel array with column-parallel ADCs performs recording and stimulation with a total power consumption of 120mW [10].

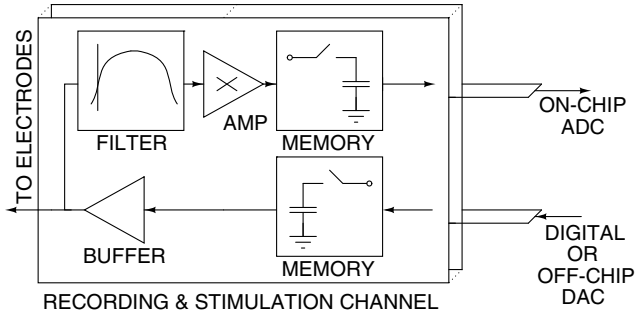

Fig. 1. Column architecture of the neural recording and stimulation interface.

We present a 128-channel fully differential array which performs simultaneous recording and simultaneous stimulation on all channels. The neural microsystem has a fully digital interface including on-chip SAR ADCs and biphasic voltage stimulators. The neural interface has an input-referred noise of 6.08μV_{rms} over a 5kHz bandwidth, occupies an area of 3.4mm×2.5mm and has a total power consumption of 2.4mW and 7mW for the recording and stimulation modes, respectively.

The rest of this paper is organized as follows. Section II describes the architecture of the neural interface. Section III presents the VLSI circuit implementation of the recording channel, the analog-to-digital converter, and the stimulator. Section IV demonstrates the experimental results.

II. Architecture

The presented neural recording and stimulation interface consists of an array of 8×16 channels with column-parallel ADCs. Low power dissipation and channel area are the key design constraints. Figure 1 depicts the column architecture.

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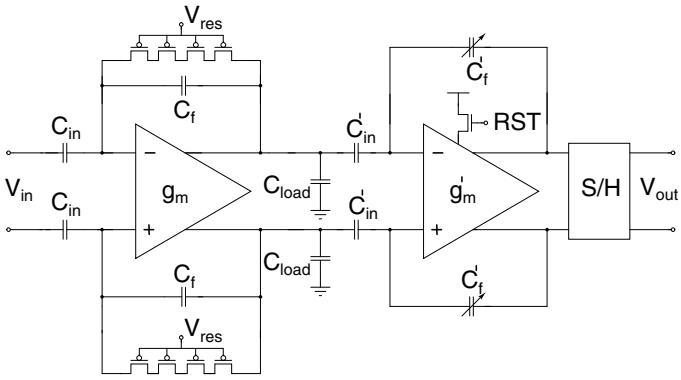

Fig. 2. Recording channel architecture.

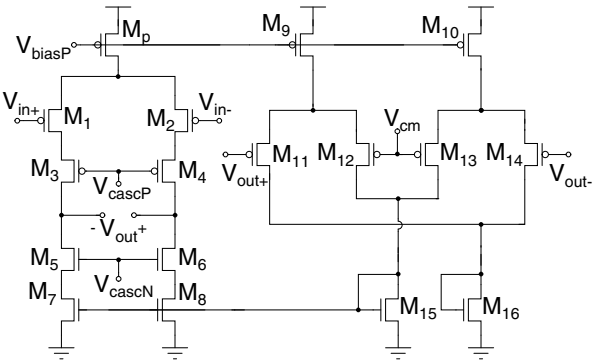

Fig. 3. Fully differential telescopic OTA.

The channel has a fully differential low-noise amplifier with a bandpass filter. Both the low-pass and high-pass frequencies are adjustable. The gain can be digitally tuned from 54dB to 73dB with eight programable gain modes. The column parallel ADCs are fully differential SAR ADCs. The stimulation circuit performs monophasic or biphasic stimulation. In-channel memory circuits enable simultaneous recording and simultaneous stimulation among all channels.

III. VLSI Circuit Implementation

A. Recording Channel

The neural recording channel combines two stages of fully differential signal amplification in order to achieve high gain without degrading the channel linearity. Figure 2 illustrates the architecture of the recording channel where the first stage acts as a high pass filter and the second stage provides a programmable gain. The output of the second stage is fed to a sample-and-hold circuit [11] in order to ensure simultaneous sampling among all array channels. Fully differential signaling is utilized to reduce common-mode noise and reduce interference from on-chip digital circuitry.

The first stage is implemented as a high-pass filter (HPF) with DC rejection in order to remove the DC offset that typically appears at the electrode tissue interface. The large input capacitance of the first stage rejects DC offset signals and prevents the amplifier from saturation. The first stage HPF is implemented by utilizing PMOS transistors biased in subthreshold region and a capacitor in the feedback [1]. In order to reduce the distortion caused by large output signals across subthreshold transistors, four PMOS transistors are placed in series with their bulk connected to V_{DD}. In this manner, the drain-to-source voltage of each transistor is lowered and the non-linearity is reduced. The HPF cut-off frequency is tunable from 0.5Hz to 50Hz by changing the bias voltage of the PMOS transistors.

The first stage has a low-pass filter (LPF) cut-off frequency tunable between 500Hz and 10kHz which is controlled by the bias current of the operational transconductance amplifier (OTA). The LPF acts as an anti-aliasing filter for the on-chip ADC. The closed loop mid-band gain of the first stage is 33dB.

A fully differential telescopic OTA shown in Figure 3 with common-mode feedback circuit [12] is employed in the first stage. The width of the input transistors is made large to bias them in the subthreshold region [1] to maximize their transconductance. The transconductance of the load transistors is minimized by using narrow devices. This reduces the overall thermal noise. The flicker noise is minimized by using PMOS for the input transistors and maximizing the area of their gates. Power dissipation is minimized by selecting the telescopic OTA architecture operating in the subthreshold region.

The second stage is a folded cascode amplifier as it requires a higher output voltage swing and its noise contribution is negligible. In order to avoid limiting the amplifier's output voltage swing, the common-mode feedback circuit uses a capacitive divider that is reset to the common-mode voltage value once every thousand cycles [13]. The second stage provides a programmable closed loop gain for the overall channel gain of 54dB to 73dB with eight different gain modes.

B. Analog-to-Digital Converter

Implantable neural interfaces require ultra-low power signal digitization to ensure long battery life. In order to avoid anti-aliasing, the sampling rate of the ADC has to be higher than the Nyquist rate by a margin accounting for the anti-aliasing filter pass-band roll-off. A sampling rate of 14kHz per channel for a 5kHz signal bandwidth is achieved by designing column-parallel ADCs sampling at 111kS/s.

The column-parallel analog-to-digital converter is a fully differential successive approximation (SAR) ADC. SAR ADCs offer low power dissipation for medium resolutions and medium sampling rates, 8 bits and 100kS/s, respectively, in this design. Column parallel ADCs are advantageous over a single ADC as they allow for design scalability.

Figure 4 shows the architecture of the ADC. The differential input signal is sampled when SAMPLE goes high and is applied to the differential capacitor array through the analog switch network. The output of the capacitor array is fed to the comparator. The comparator consists of a preamplifier and a latch. Once the comparator makes a decision, its output is sent to the SAR register where the digital output bits are evaluated after eight clock cycles and fed back to the capacitor array.

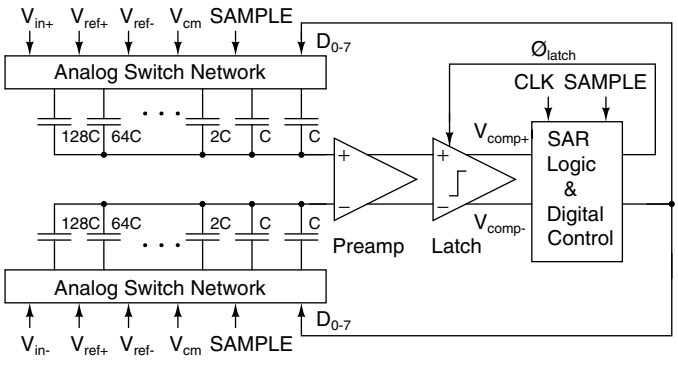

Fig. 4. Self-timing successive approximation ADC architecture.

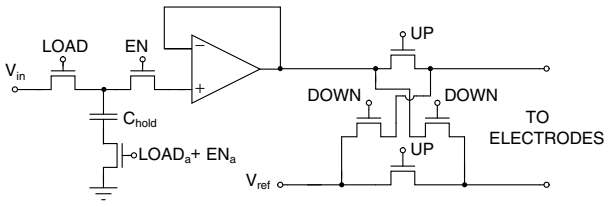

Fig. 5. In-channel biphasic stimulator.

In order to further reduce the power dissipation, self-timing methodology is incorporated to start bit-cycling immediately after the comparator makes a decision [14] [15].

C. Stimulator

The voltage-mode stimulator on each channel consists of a sample-and-hold circuit, a class AB amplifier [10], and a switch network as shown in Figure 5.

The sample-and-hold circuit allows for simultaneous stimulation on all channels. A 128-sample stimulation frame is sequentially loaded onto the capacitor array when LOAD is high and is activated on all channels at the arrival of an EN pulse. Charge injection is minimized by opening the capacitor bottom plate slightly in advance of the other two switches.

Voltage stimulation can be configured as a monophasic or biphasic sequence. Monophasic stimulation leads to charge accumulation at the electrode-tissue site and can damage the tissue. Biphasic stimulation where each pulse is followed by a pulse of reversed polarity ensures charge balancing and prevents damage at the electrode-tissue interface. The cross-coupled switches implement monophasic and biphasic voltage stimulation [16]. The stimulator input can be a digital or analog voltage. Analog input voltage stimulation allows for stimulation with arbitrary-shaped analog waveforms that are of particular importance in neurological research applications.

IV. Experimental Results

The 3.4mm×2.5mm 128-channel fully differential digital recording and stimulation neural interface was fabricated in a standard 0.35μm double-poly CMOS technology. Figure 6 shows the micrograph of the die.

The input-referred noise density of the first stage of the recording channel is experimentally measured in the frequency

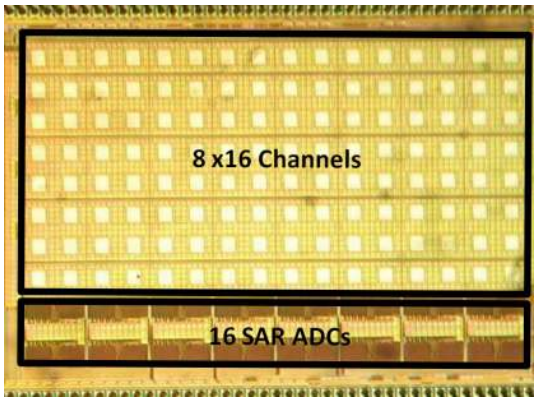

Fig. 6. Micrograph of the neural recording and stimulation interface.

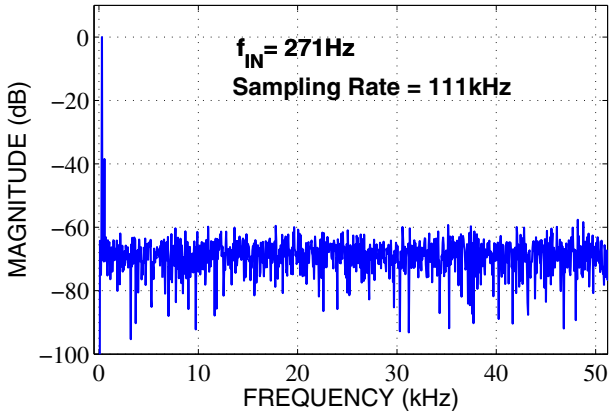

Fig. 7. Measured output spectrum of ADC for a 271Hz sinusoid input sampled at 111kS/s.

range of 10Hz to 5kHz. Integrating the noise over this bandwidth yields an RMS noise voltage of 6.08μV.

A 271Hz full-range sinusoid was applied to the ADC. The experimentally measured output spectrum is depicted in Figure 7. The second harmonic reduces the effective number of bits (ENOB) of the ADC to 6.2 bits. The differential nature of the ADC suppresses the second harmonic. Removal of the second harmonic yields an ENOB greater than 7 bits. Static DC testing revealed that there were no missing codes for the ADC.

The functionality of the full 8×16 neural recording interface was experimentally validated when recording an entire signal frame with all channels connected to the same input. A neural spike waveform was emulated with a signal generator to model extracellular neural activity. An emulated neural spike with an amplitude of 1mV$_{pp}$ was the input signal to all channels. The input signal was amplified and digitized using the on-chip amplifiers and ADCs. The digitized output corresponds to a differential output of 440mV and is depicted in Figure 8. In this figure the digitized output shows an amplitude of 22 percent of the ADC full signal range.

The experimental results for the recording channel are summarized in Table I. The experimental results for the whole

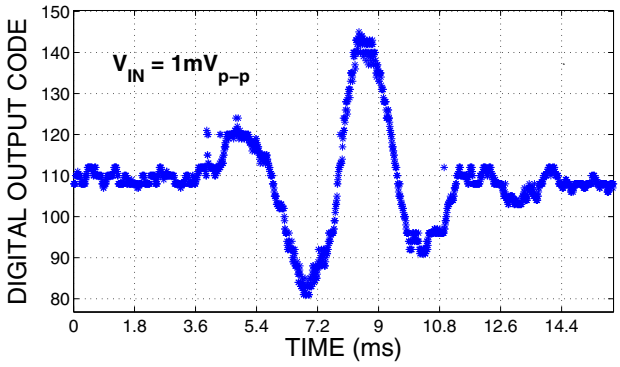

Fig. 8. Measured digitized output of the full recording channel including the amplifier and ADC with an emulated neural spike input of 1mV_{pp}.

TABLE I
RECORDING CHANNEL EXPERIMENTAL CHARACTERISTICS

Programmable Gain	54-73 dB
Low Frequency Cut-off	0.5-50Hz
High Frequency Cut-off	500Hz-10k
Input Referred Noise	$6.08\mu V$, 10-5kHz
Power Dissipation per Channel	$12.75\mu W$
NEF of 1st Stage	5.6

chip are shown in Table II.

V. Conclusions

We have presented a 128-channel fully differential integrated neural interface for neural recording and stimulation. In the recording mode, the fully differential channels simultaneously amplify neural signals and convert them to the digital domain. In the stimulation mode, the buffered stimulation signal can be configured to perform simultaneous monophasic or biphasic stimulation on differential electrodes. The total measured power dissipation of the recording and the stimulation modes is 2.4mW and 7mW, respectively. The noise efficiency factor is 5.6.

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TABLE II
SYSTEM-LEVEL EXPERIMENTAL RESULTS

Technology	0.35μm CMOS
Supply Voltage:	
Recording Array	3.0V
Stimulation Array	3.3V
Die Dimensions	3.4mm$\times$2.5mm
Area per Channel	$200\mu m \times 200\mu m$
Number of Recording Channels	128
Number of Stimulation Channels	128
ADC Input Range	2V_{pp}
Sampling Rate of ADC	111kS/s
ENOB of ADC	6.2 bits
Power Dissipation:	
Recording Array	1.63mW
Stimulation Array (Quiescent)	6.59mW
Read-out Circuits	0.44mW
ADC Bank	0.36mW

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