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The ALICE Silicon Pixel Detector: readiness for the first proton beam

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ABSTRACT: The Silicon Pixel Detector (SPD) is the innermost element of the ALICE Inner Tracking System (ITS). The SPD consists of two barrel layers of hybrid silicon pixels surrounding the beam pipe with a total of $\approx 10^7$ pixel cells. The SPD features a very low material budget, a 99.9% efficient bidimensional digital response, a 12 μm spatial precision in the bending plane (rϕ) and a prompt signal as input to the $L0$ trigger. The SPD commissioning in the ALICE experimental area is well advanced and it includes calibration runs with internal pulse and cosmic ray runs. In this contribution the commissioning of the SPD is reviewed and the first results from runs with cosmic rays and circulating proton beams are presented.

KEYWORDS: Large detector systems for particle and astroparticle physics; Particle tracking detectors; Hybrid detectors; Heavy-ion detectors

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1 Introduction

ALICE [1] (A Large Ion Collider Experiment) is the LHC (Large Hadron Collider) experiment devoted to the investigation of strongly interacting matter at high energy density and temperature that is expected to be produced in ultra-relativistic nucleus-nucleus collision.

The ALICE Inner Tracking System [2] consists of six cylindrical layers of silicon detectors placed around the 800 μm-thick beryllium beam-pipe. The different silicon technologies, the number of layers and their distance to the interaction point were optimized for efficient tracking and high impact-parameter resolution. Starting from the beam axis, two layers of hybrid Silicon Pixel Detector (SPD), two layers of Silicon Drift Detector (SDD) and two layers of double-sided Silicon micro-Strip Detector (SSD) are installed.

The SPD will play a key role in the ALICE apparatus providing the track position resolution required for the reconstruction of the primary interaction vertex and of the secondary vertices from weak decays of open charm and beauty particles. For this scope the two layers of silicon pixel detector were placed as close as possible to the beam pipe at a radius of 3.9 and 7.6 cm from the interaction point respectively. The detector modules are mounted on a rigid low-mass carbon composite structure 200 μm thick to fulfill the required low material budget (2.28% X_0 for the full SPD).

2 Overview of components and system

The average distance of the inner pixel layer from the beryllium beam pipe is less than 5 mm. The SPD is composed of two half-barrels that are installed and attached in their nominal position before the cylindrical structure that holds the other two ITS detectors is slided on top of it to reach the final position. Each half-barrel is segmented in 5 sectors. Each sector supports 6 staves (4 in the outer layer and two in the inner layer) with cooling pipes embedded in the support structure and running

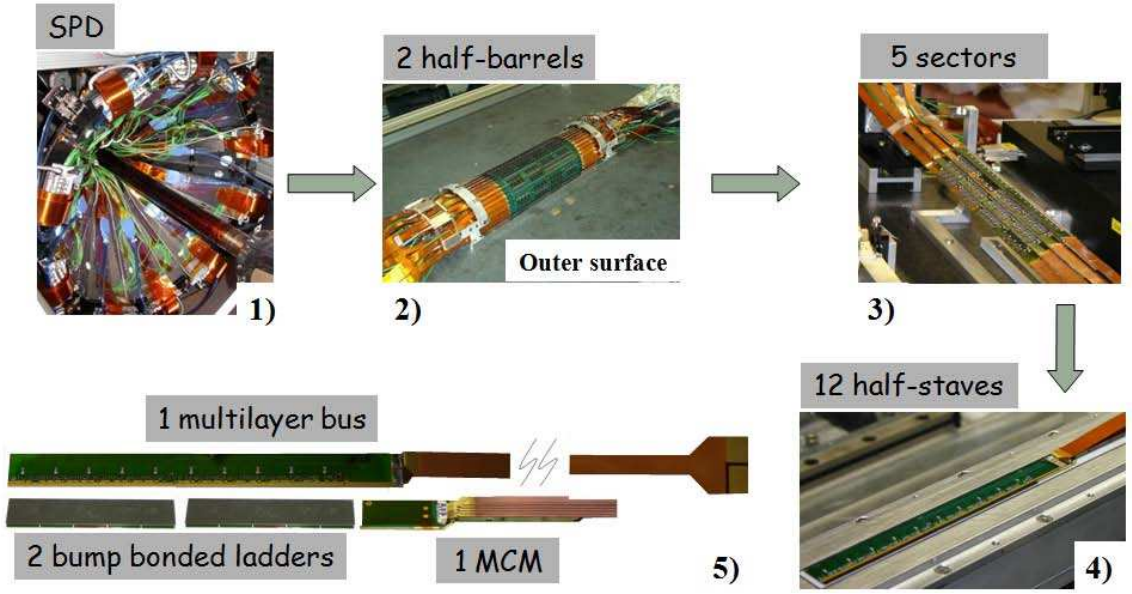

Figure 1. The SPD segmentation. Clockwise: 1) the detector in its final position around the beam pipe; 2) the outer surface of the first completed half-barrel; 3) the first assembled sector; 4) one half-stave just glued and 5) all the components constituting the half-stave.

underneath the staves. Each stave consists of two half-staves with the active region in the middle section and the cabling (optical and power connections) at the two ends (see figure 1).

The half-stave consists of two ladders and a multi-chip module (MCM) glued and wire bonded [3] to an aluminium-polyimide multi-layer laminate (pixel bus) 280 μm thick.[1]The detector element of the SPD is the ladder: a two-dimensional matrix of reverse-biased diodes bump-bonded to 5 front-end chips named ALICE1LHCb [4]. The sensor matrix includes 256 x 160 pixel cells having size of 50 μm (rϕ) x 425 μm (z). The front-end chip reads out a sub set of detector cells, 256 (rϕ) x 32 (z). The MCM contains the on-detector electronics which distributes timing signal, provides the required analog references and performs the data multiplexing and serialization [5]. The communication between the MCM and the counting room is via optical links with three single-mode fibers (one to receive the clock from LHC, one for the serial and one for the data transfer). The communication between the MCM and the front-end chips is through the pixel bus.

The total power dissipated in the SPD front-end electronics is about 1.35 kW. Due to the low mass and high density of components, the requirements on the cooling system are very demanding: in the event of a cooling failure, the detector temperature would increase at a rate of 1°C/sec. An evaporative C_4F_{10}-based cooling system has been developed and thin pads of thermal grease are placed on the cooling ducts in correspondence with the front-end chip to achieve the required cooling efficiency [6]. The detector operating temperature is around 30°C. Two PT1000 chains are embedded in the top of the pixel bus to monitor the half-stave temperature. The two chains are read out separately to provide a redundant hardware interlock. The first is managed with a PLC based system and the second is read out through the SPD off-detector electronics. Both systems are wire

[1]See http://morel.web.cern.ch/morel/cgi-bin/alice.htm for a detailed description of the pixel bus structure and technologies.

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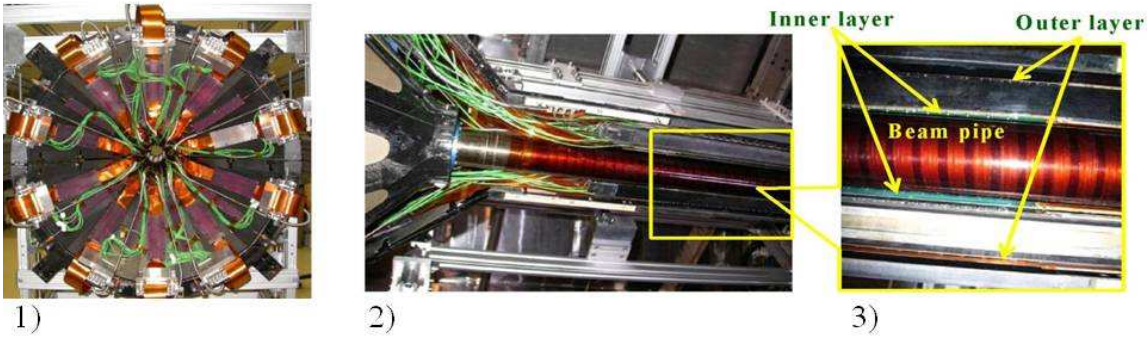

Figure 2. From left to right: 1) the first integration test of the SPD in the Departmental Silicon Facilities (in ALICE, the hole in the center is filled with the beam pipe); 2) the top half-barrel positioned close to the beam pipe before it is joined to the second one; 3) a detail of the previous picture where the beam-pipe, the SPD outer and inner layer are indicated.

connected to the LV power supply to switch them off in case the half-stave temperature exceeds a pre-set temperature threshold (the typical set is 40 °C). Additional signals to the hardware interlock come from the cooling plant and the cooling line status. A slower software interlock, integrated in the Detector Control System (DCS), runs in parallel with the previous ones. It is segmented at the half-stave level while the hardware interlock acts on the half-sector to account of the low-voltage power supply segmentation.

The SPD front-end electronics read-out runs at 10 MHz clock frequency. One chip is read in 256 clock cycles. The 10 chips of each half-stave are processed sequentially in 256 μsec. The same time is required for the full SPD because all the half-staves are accessed in parallel. Each SPD chip provides a prompt signal based on the on-chip fast-OR circuitry; a signal is generated whenever one or more cells detect a signal above threshold. The 1200 fast-OR signals are sent to a pixel trigger system designed for fast implementation and processing of predefined algorithms to contribute to the L0 trigger decisions [8]. A challenging requirement on the SPD prompt fast-OR trigger is that it must reach the L0 trigger logic input at the ALICE Central Trigger Processor (CTP) within 800 nsec [7]. Taking into account the various transmission times on the optical fibers, the processing time allowed in the pixel trigger board is limited to 25 nsec. The pixel trigger system, integrated in the ALICE Experiment Control System (ECS), satisfies these requirements [9]. So far 9 physic algorithms and some cosmic dedicated ones have been implemented and can be software selected. The algorithms are programmable in an on-board FPGA allowing for maximum flexibility. The full system has been installed and thoroughly exercised during the commissioning phase described in the following.

Details on the SPD system: components, assembling and read-out can be found in a recent technical paper [2].

3 Assembly and integration

The component testing, assembly and integration have been carried out in dedicated facilities at the collaborating Institutes. Several steps of the assembly and integration procedures have been inter-

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spersed with check procedures to assure constant quality all across the production and to achieve the design performance.

Semi-automatic procedures were developed to characterize on-wafer and classify pixel ASICs and bump bonded ladders. This allowed us to achieve a very good overall yield throughout wafer processing and bump bonding [11]. The half-staves were assembled, wire bonded and characterized in a Class 100000 clean room, equipped with a Micrometric Measurement Machine (Apex-Crysta 9166, Mitutoyo) and a Delvotek ultrasonic wire-bonder machine. The first, used for the half-stave assembly, was equipped with custom made tools for the components alignments while the latter was used for the wire-bonding connections between the MCM, the FEE chip and the multilayer pixel bus. The half-staves were individually tested and characterized to select those of 'class I' which have been used to build the SPD. The percentage of half-staves tagged as class I during the production is greater than the 90%. The procedure, which takes into account the main detector functionalities, is described in the following.

The pixel chip includes many operation parameters, remotely adjustable through 8-bit DACs, to tune current and voltage bias references, L1 trigger delay, global threshold voltage and leakage current compensation. All these functionalities were tested tuning few dedicated DACs. The uniformity response of the chip matrix and the minimal threshold settable to avoid the presence of noisy pixel (typical values found are 200 DAC unit $\approx 2800e^{-}$) were verified. These measurements were performed using the on-chip programmable amplitude pulser. The half-staves were also tested using a radioactive source (Sr^{90}) in order to assess possible bump bonding defects. This test was performed in self-trigger mode, using the internal fast-OR, to reduce the time needed to collect a statistically significant data sample. Finally, it was required a number of noisy and dead pixels in each half-stave less than 1%, and a maximum value of leakage current of 15 μA at the nominal bias voltage of 50V.

The so qualified class I half-stave were then transferred to the assembly facility for precision mounting onto the carbon-fiber support sectors. The half-staves were electrically tested for signal integrity before and after being mounted. The cooling circuit and the electrical/optical connections were also verified before continuing the integration process.

The final integration and pre-commissioning of the assembled sectors and half-barrels were carried out in a surface facility at CERN. The system was equipped with cooling plant, LV and HV power supplies, optical fibers and electrical cables of the same type and length as in the experimental area. A prototype temperature interlock system was also provided to guarantee safe operations. The temperature sensor readings were cross-checked and calibrated using IR thermal video cameras. A first release of Detector Control System (DCS) was operational [10]. Test data were collected using the available ALICE Data Acquisition (DAQ) system. A mechanical integration test with the half-barrels was also carried out in the same facility with handling and installation gear which was later used for the installation in the experiment (see figure 2).

4 Commissioning

The SPD installation in the ALICE experimental hall took place at the end of June 2007; the remaining part of the ITS and the TPC were then moved to their final positions. After that, the service support, which houses power/optical cables and cooling pipes for all the central detectors,

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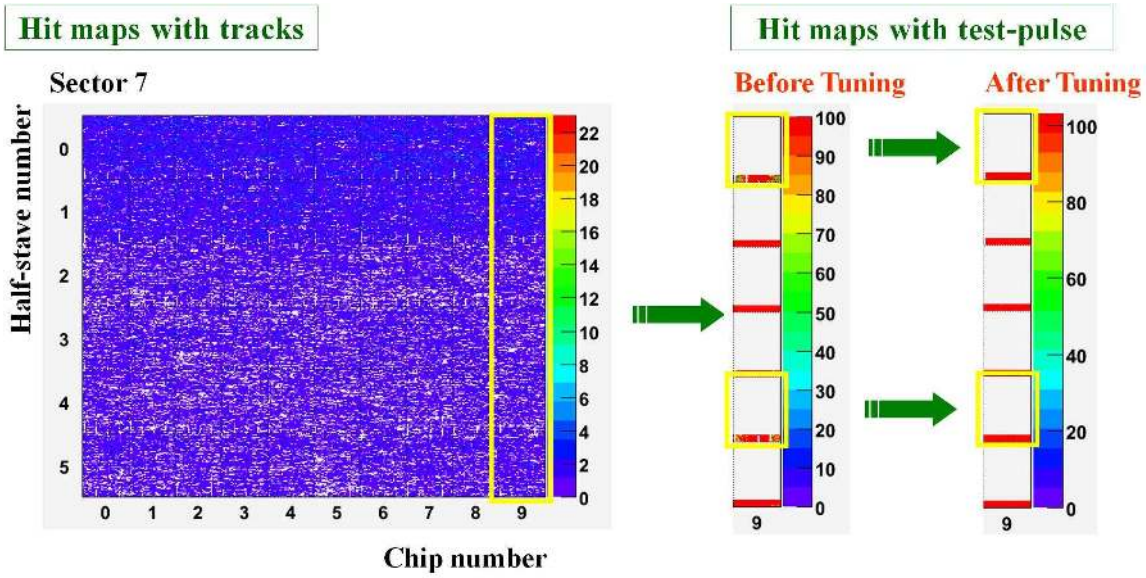

Figure 3. Example of calibration plots. On the left a sector hit map is shown with cosmic tracks collected during the commissioning. On the right the same kind of plot showing the last chip response to the internal pulser. The result of the tuning procedure on the chip 9 is shown.

was installed and finally all the services needed to power and readout the SPD were connected. At the same time the Detector Control System (DCS) was deployed and integrated in the Experimental Control System (ECS) and Data Acquisition (DAQ) and the off-detector electronics was installed and commissioned.

In December 2007 the SPD commissioning in the ALICE framework started. The SPD was initially set up with the configuration files produced during the half-stave characterization. The optimized configuration files were then stored in the SPD Configuration DataBase (CDB) developed in ORACLE. In this phase the uniformity matrix response was checked with the internal pulser to spot the noisy and not responding pixels, the operating temperature of each half-stave was also measured. A fine tuning of the programmable DAC settings was done to obtain the best compromise between performance and current dissipation. The calibration data were analyzed with on-line and off-line tools running in the ALICE framework. In figure 3 some examples of plots from these studies are shown. A typical sector hit map with all the tracks collected during the commissioning phase is shown on the left. The chip position in the half-stave and the half-stave position in the sector are reported on the x and y axis respectively. The half-stave 0 and 1 belong to the inner layer and the others to the outer one. The sparse holes in the uniformity pixel response are due to insufficient statistics. On the right the response to the internal pulser before and after the DACs tuning for the chips 9 in the same sector is shown. The matrix detects all the signals when the good setting is found. As an example only part of the matrix was pulsed but the improvement on the matrix response for 2 chips can be noticed.

During this commissioning it was not possible to power the full detector. Stable data taking with the expected performance was achieved with 106 half-staves out of 120 total (88.3%). The

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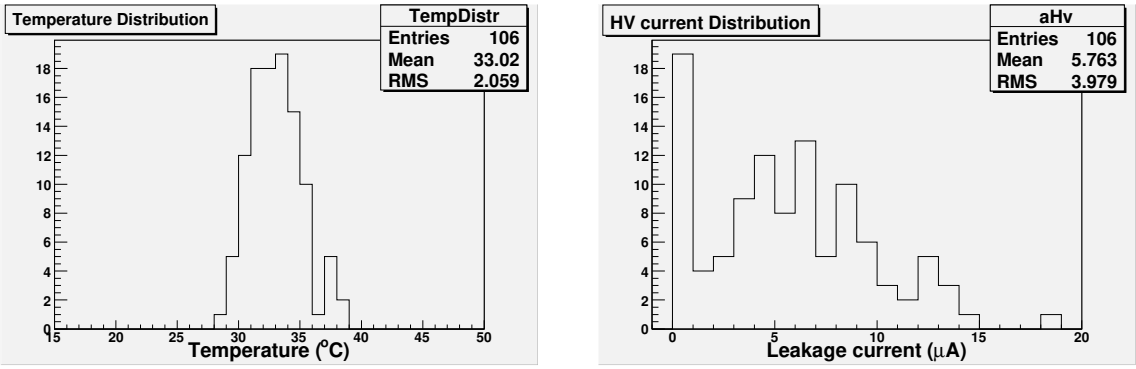

Figure 4. Left: temperature distribution for all the powered half-stave. Right: Current leakage distribution measured for the same half-staves.

remaining 14 half-staves could not be effectively operated due to localized lower efficiency of the cooling system, which will be investigated during the winter shut down. It was found that few half-staves had faulty connections which have now been repaired. The optimization of the cooling circuit operating parameters is well advanced. The overall percentage of not usable pixel cells of the included half-staves ($\approx 0.05\ ^{o}/_{oo}$) is well within the specifics. This percentage takes into account the dead pixels found during the half-staves characterization and the pixels electrically masked because they were noisy. The overall number of unusable pixels is actually a lower limit because the count of dead pixels could not be verified due to the lack of statistics of cosmic tracks, visible also in figure 3. In figure 4 the temperature and leakage current[2] distributions during the SPD operation with the first circulating beam are shown.

The SPD readout has been tested with a random generated trigger up to 40 MHz. The measured readout time per event, which very slightly depends on the occupancy, is $\approx 300\ \mu$s. The dead time has been shown to be negligible up to a trigger rate of ≈ 3 kHz thanks to the multi-event buffer system. At higher rate, the dead time depends on the probability to fill the multi-event buffer. The maximum event readout rate has been verified to be ≈ 3.3 KHz. The readout performance are in agreement with the design specification.

5 Calibration and alignment

In February 2008 the first ALICE global cosmic run took place and the SPD participated in the data taking with the others detectors. In May 2008 the pixel trigger system was installed and commissioned, requiring dedicated DACs tuning for the SPD fast-OR circuitry. At present 923 out of 1200 chips are included in the Fast-OR logic ($\approx 88\%$ of available half-staves). A manual procedure to tune the four fast-OR DACs per chip has been used to build the basis of a full automatic procedure, which is actually under development and which will be integrated in the configuration strategy.

The pixel trigger importance was immediately clear for the SPD commissioning and for the alignment of the central tracking detectors: the ITS and the TPC. As already mentioned, some pre-

[2] The bias voltage is set to the nominal value (50V) except for those half-staves with a leakage current close to 20μA. In this case lower bias voltages are used for the moment. Anyway the detector is fully depleted at 12V as shown in previous studies [12].

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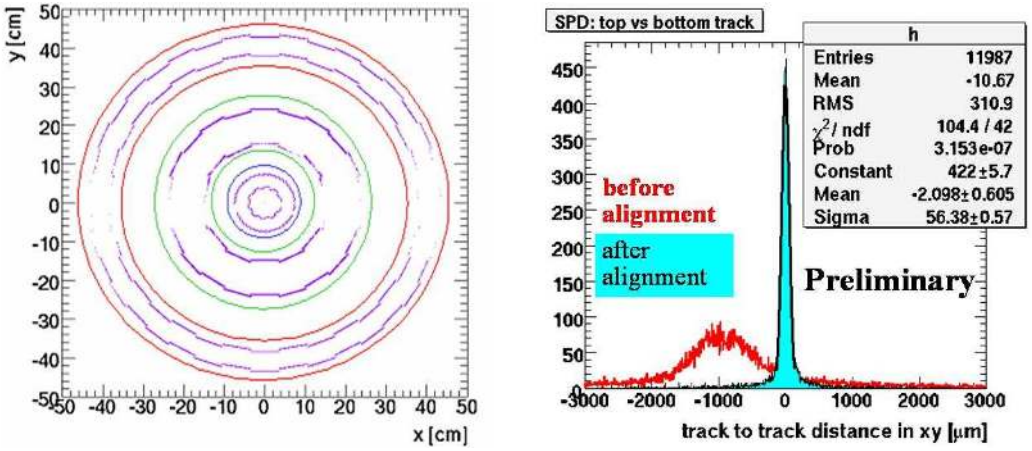

Figure 5. Left: display of all the ITS reconstructed clusters from the events taken during the cosmic run and used for the alignment. It can be easily observed a reduced number of cluster on the sides because of the lower probability of horizontal cosmic ray. Right: residuals for the SPD alignment using the Millepede Monte Carlo code. The filled curve shows the residuals after the alignment of the two half-barrels.

defined algorithms, such as multiplicity and cosmic trigger, have been already implemented in the pixel trigger system. The algorithm usually used to collect cosmic events with tracks in the SPD is named top-bottom-outer-layer (a trigger is generated if at least two hits are detected in the outer layer; one located in the top half-barrel and one in the bottom). Since May 2008 more than 100000 reconstructed cosmic tracks were collected by the ITS with the trigger provided by the SPD. The trigger rate varied from 0.08Hz to 0.18Hz, depending on the number of half-stave participating in the trigger logic. The values are in agreement with the expected rate from the L3 measurements at LEP. The tracks with at least 3 points in the SPD (≈ 45000 with 4 points and ≈ 55000 with 3 points) are used to align the detector: the goal is to determine the spatial corrections to be applied to the ideal geometry implemented in the ALICE software in order to match the real geometry of the installed SPD. The number of alignment parameters to be determined is six per sensor (ladder), i.e. 1440 for the whole detector, and the required precision is below 10μm (better than the intrinsic position resolution) in the transverse plane. Two independent methods, based on tracks-to-measured-points residuals minimization, are considered. The first method uses the Millepede approach [13], where a global fit to all residuals is performed, extracting all the misalignment and tracks parameters simultaneously. The second method performs a (local) minimization for each single module and accounts for correlations between modules by iterating the procedure until convergence is reached. The main figure of merit of the realignment quality is, for cosmics, the spread of the transverse distance between the two independently-fitted tracks in the upper and in the lower half barrels. At the moment, preliminary results from the Millepede realignment give a spread of $\approx 56\mu$m in the cosmic data (figure 5, right), to be compared to the $\approx 40\mu$m obtained from a simulation with perfectly aligned detector geometry. This result, confirmed by other independent checks, indicates a residual misalignment lower than 10μm at the sensor level.

In June 2008 LHC started to exercise beam 1 (the anticlockwise beam which is injected in LHC before ALICE) and it was dumped before reaching ALICE. In June the 12$^{\text{th}}$, the SPD was the first detector in the LHC experiments which observed the first particles created in LHC. From June on other tests were carried out and the SPD recorded data giving a fast feedback to the LHC

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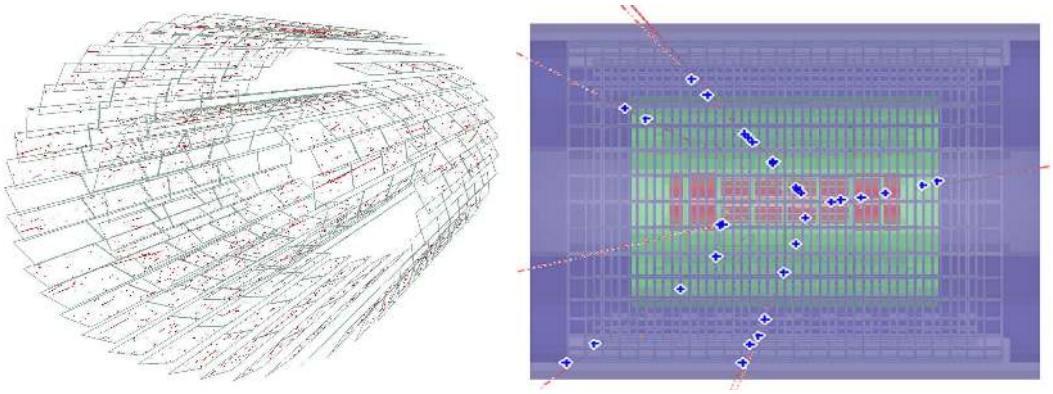

Figure 6. On the left the first event with particles generated in LHC ever seen by a LHC experiment. The muons generated far away from the interaction point by the beam dump traveled parallel to the beam axis making long tracks in the SPD (more than 10 cm). On the right the first event reconstructed in the ITS and triggered by the SPD showing the LHC beam which interacts with the detector materials. The event has been reconstructed with the final vertexing algorithm.

people about the multiplicity observed in each beam condition (*beam dumped and beam circulating with/without screens in*). On September 12th, when there were the first circulating beams in the LHC, the ITS, triggered by the SPD, caught the first interaction between proton beam and one SPD module. In figure 5 the two most remarkable pictures representing the SPD readiness for physics and its great contribution in the ALICE experiment since the beginning are shown. More details on the detector commissioning can be found in [14]

6 Conclusion

The SPD was installed in June 2007 and the commissioning in ALICE was started in December 2007 after the cabling and cooling connections. All the read out electronics and power supplies are in place and commissioned. The safety interlocks are all connected and fully operational. The pixel trigger electronics is also installed and commissioned with the required trigger algorithms. The DCS is available in agreement with the ALICE rules and it is well integrated in the ECS. The read-out time and dead time for the SPD have been measured and are in agreement with the design specifications.

A series of calibration runs were performed to tune the SPD configuration and to reduce the current consumption without loss in performance. The SPD took part in stable runs with the 88.3% of the detector and a low fraction of dead and noisy pixel (well below the expected 0.1% upper limit). The fast-OR prompt pixel trigger includes $\approx$ 88% of chips. An automatic procedure to speed-up the fine adjustment of the fast-OR response is being developed.

The SPD is ready for the first collisions; further optimizations are in progress to achieve full performance and 100% coverage.

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