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The ambipolar transport behavior of WSe_2 transistors and its analogue circuits

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Abstract

Tungsten diselenide (WSe_2) has many excellent properties and provides superb potential in applications of valley-based electronics, spin-electronics, and optoelectronics. To facilitate the digital and analog application of WSe_2 in CMOS, it is essential to understand the underlying ambipolar hole and electron transport behavior. Herein, the electric field screening of WSe_2 with a thickness range of 1–40 layers is systemically studied by electrostatic force microscopy in combination with non-linear Thomas–Fermi theory to interpret the experimental results. The ambipolar transport behavior of 1–40 layers of WSe_2 transistors is systematically investigated with varied temperature from 300 to 5 K. The thickness-dependent transport properties (carrier mobility and Schottky barrier) are discussed. Furthermore, the surface potential of WSe_2 as a function of gate voltage is performed under Kelvin probe force microscopy to directly investigate its ambipolar behavior. The results show that the Fermi level will upshift by 100 meV when WSe_2 transmits from an insulator to an n-type semiconductor and downshift by 340 meV when WSe_2 transmits from an insulator to a p-type semiconductor. Finally, the ambipolar WSe_2 transistor-based analog circuit exhibits phase-control by gate voltage in an analog inverter, which demonstrates practical application in 2D communication electronics.

Introduction

P-type and n-type transistors are the basic elements for constructing silicon-based complementary metal-oxide-semiconductor (CMOS) electronics to realize digital and analog applications[1]. Typically, unipolar p-type and n-type transistors with high density are fabricated by various doping techniques and are integrated to build logic circuits[2]. The requirement of spatial separation in circuits makes the fabrication more complicated, resulting in the increase of fabrication costs. Conversely, ambipolar transistors, which can be easily switched between p-type and n-type by applying an electric field, are promising candidates to minimize circuit size with effectively simplified designs.

There are a few promising materials with the ambipolar property, including organic/inorganic semiconductors. However, organic semiconductors are rarely applied in high-frequency logic electronics due to the relatively low carrier mobility[3]. Graphene's[4] absence of bandgap hinders its application in logic devices, even though the bandgap can be somehow tuned[5,6]. Although layered black phosphate has been shown to possess a unique ambipolar property[7], it hardly survives after several hours of exposure in the atmosphere due to the low reactive barrier between black phosphate and oxygen/water[8–10]. Recently, transition metal dichalcogenides (MX_2, where M = group IVB–VIIB metal and X = chalcogen) with a layered crystal structure were demonstrated to exhibit excellent semiconducting electrical properties with a large on/off ratio[11–14]. Among them, tungsten diselenide (WSe_2), which consists of one layer of W atoms sandwiched between two layers of Se atoms, has many excellent properties providing potential applications, including valley-based electronics[15,16], spin-electronics,

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and optoelectronics[17,18]. More significantly, different from the unipolar n-type semiconductor MoS_2 with the presence of sulfur vacancy and the strong Fermi level pinning near the conduction band[19–21], WSe_2 as an ambipolar semiconductor has been demonstrated as having Fermi level effectively shifting between the valence band and the conduction band under application of an external field[22–24].

Recently, the optical and hole dominant transport properties of exfoliated WSe_2 have been explored[24–27]. To facilitate the potential application of WSe_2 in CMOS, it is essential to understand the underlying ambipolar hole and electron transport mechanisms. In this study, we obtain deep insight into the thickness-dependent electric field screening effect, and the interlayer coupling interaction is analyzed according to Thomas–Fermi theory. The thickness from 1 to 40 L and temperature-dependent ambipolar transport behavior of WSe_2 transistors are studied systematically. Furthermore, the Fermi level shift of WSe_2 under gate voltage is investigated to understand its ambipolar behavior by Kelvin probe force microscopy. Finally, ambipolar WSe_2 transistors in analog circuits exhibiting gate-controlled phase change are demonstrated in practical application in two-dimensional (2D) electronics.

Materials and methods

Device fabrication

The WSe_2 flakes were mechanically exfoliated from a bulk crystal onto an SiO_2/Si wafer using adhesive tape. The FETs were fabricated on a single wafer using electron beam lithography, simultaneously exposing all of the devices with the same processing step to ensure uniformity. The source and drain electrodes (10 nm Ti/40 nm Au) were deposited by electron beam deposition with a deposit speed of 0.2 Å/s. Before electron beam evaporation, the samples were kept overnight under the high vacuum of the electron beam deposition system. All of the devices were deposited simultaneously to ensure the same conditions. Before measurement, devices were annealed under Ar (including 10% H_2) at 200 °C for 2 h.

Measurement

The Raman spectroscopy measurements were carried out with 514-nm, 1.0-mW laser excitation and ×100 objective (Renishaw inVia Raman Spectroscope, Sweden). High-resolution transmission electron microscopy (HRTEM) imaging was conducted using an FEI Talos F200X operated at 200 kV. EFM measurements were performed with a commercial atomic force microscopy (AFM) instrument (Dimension Icon, Bruker, USA) under ambient conditions. Commercial rectangular silicon cantilever coated with a Co/Cr layer with a resonant frequency of 75 kHz and a spring constant of 2.8 N/m (MESP, Bruker, USA) was used for electrostatic force microscopy (EFM) imaging. The tip radius of the magnetic tip is ~35 nm. The tip lift height is 10 nm. A Keithley 4200SCS was employed to measure the direct current transport properties of the devices using a probe station in a vacuum chamber. The performance of the analogs circuits was measured using an oscilloscope (Agilent Infiniti Vision 3000). V_{bias} and V_{DD} were applied by the Keithley 4200SCS, and V_{ac} was applied using a signal generator (Agilent 33120 A).

Results and discussion

WSe_2 flakes were prepared by mechanical exfoliation, and the optical properties, including the optical contrast and Raman spectra, were characterized (see Supplementary Figures S1 and S2). As seen, the relationship between the optical contrast or Raman optical properties and thickness trends weaker and towards disorder when the layer number is higher than 4L. Furthermore, HRTEM was employed to study the atom-stacking mode of WSe_2 with a thickness range from 1L to 12L (see Supplementary Figures S3 and S4). The similar properties, including the distance along ($\bar{1}010$) or ($0\bar{1}10$) and the similar intensity profiles along the (1210), (0110), ($\bar{1}010$), and ($2\bar{1}10$) directions in SAD patterns, indicate the same stack mode (2H mode) of WSe_2.

To gain a deeper insight into the dimensionality effect on the interlayer screening in WSe_2 flakes, EFM was employed to probe the electric field, which is caused by the charged impurities present at the WSe_2/SiO_2 substrate interface. In this study, the EFM measurements are conducted in a two-pass lift mode, in which a conductive AFM (c-AFM) cantilever first scanned over the WSe_2 flakes for topography and then was lifted a constant height to detect long-range electric interactions between the voltage applied tip and WSe_2 flakes. Because the EFM phase change directly relates to the unscreened charges, the observed differences in the EFM phase change indicate different field screening capabilities of WSe_2 flakes with different thicknesses. The typical AFM topographic image of 1L and 2L WSe_2 on SiO_2 is shown in Fig. 1a, and the corresponding EFM images under a negative tip voltage and a positive tip voltage are shown in Fig. 1b, c. The correlated line profiles from Fig. 1a–c are shown in Fig. 1d, where one can see that the phase shift ($\Delta\phi$) of WSe_2 is always negative compared to a bare SiO_2 substrate. Significantly, $\Delta\phi$ is dependent on both WSe_2 thickness and the tip bias. If the AFM tip and WSe_2 can be considered as an ideal capacitance, the EFM phase shift can be described as Eq. (1)[28,29], where Q and k are the Q-factor and spring constant of the cantilever, C is the local capacitance between the tip and WSe_2, V_{tip} is the applied

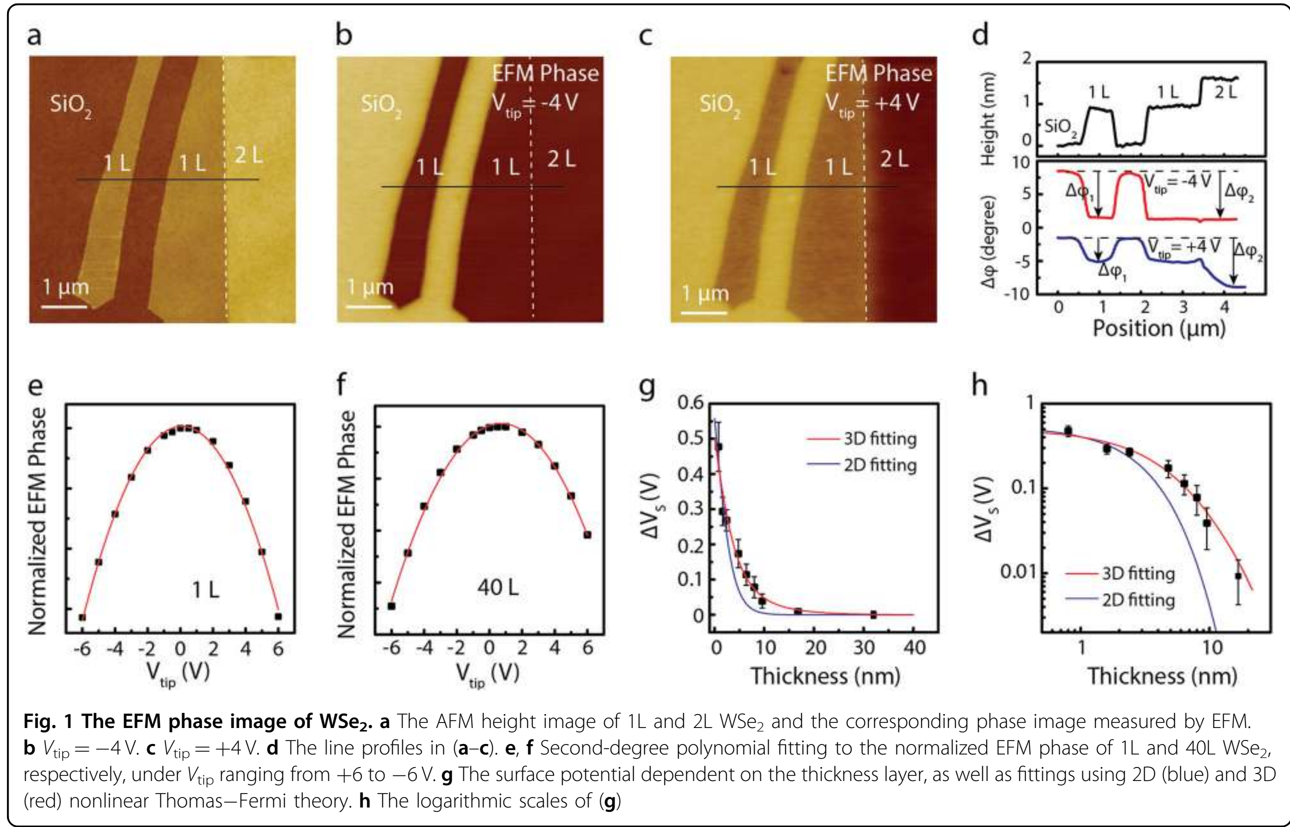

Fig. 1 The EFM phase image of WSe_2. **a** The AFM height image of 1L and 2L WSe_2 and the corresponding phase image measured by EFM. **b** $V_{tip} = -4$ V. **c** $V_{tip} = +4$ V. **d** The line profiles in (**a**–**c**). **e**, **f** Second-degree polynomial fitting to the normalized EFM phase of 1L and 40L WSe_2, respectively, under V_{tip} ranging from +6 to −6 V. **g** The surface potential dependent on the thickness layer, as well as fittings using 2D (blue) and 3D (red) nonlinear Thomas−Fermi theory. **h** The logarithmic scales of (**g**)

DC voltage, and V_s is the effective surface potential.

$$\Delta\phi = \frac{Q}{2k}\frac{\partial^2 C}{\partial^2 z}\left(V_{tip} - V_s\right)^2. \tag{1}$$

Typically, a fit between V_{tip} and phase can be achieved for both 1L and 40L WSe_2 by using a second-degree polynomial (Fig. 1e, f). The deviations of the V_s values for the 1–40L WSe_2 are summarized in Fig. 1g. As seen, the effective surface potential difference decreases as thickness increases, indicating the screening effect of WSe_2 enhanced with the number of layers. To gain insight into the screening effect, nonlinear Thomas–Fermi theory is employed to understand the interlayer couple interaction. First, if the interlayer coupling interaction is excluded, the screening effect is parallel, following the 2D model, and then the surface potential difference can be described as Eq. (2)[28,29].

$$\Delta V(D) = \frac{2\pi\hbar^2\sigma_0}{eN_sN_v m_{||}}\sqrt{2\beta_0 d}\,\frac{1 - r_D}{\sqrt{1 - r_D^2}}, \tag{2}$$

where $r_D = 1/cosh\left(D\sqrt{2\beta_0/d}\right)$; $\hbar$ is the reduced Plank constant; σ_0 is the charge density on the SiO_2 substrate; N_s and N_v are the spin and valley degeneracies ($H_s = N_v = 2$); $m_{||}$ is the in-plane effective mass; d is the interlayer spacing in WSe_2; $\beta_0 = e^2 N_s N_v m_{||}/4\pi\varepsilon_0\varepsilon\hbar^2$; and ε_0 and ε are the vacuum permittivity and the dielectric constant of WSe_2 ($\varepsilon = 7$)[30], respectively. The blue lines in Fig. 1g, h show the 2D fitting, where σ_0 is $1.2\times10^{13}\,cm^{-2}$, $m_{||}$ is $0.01m_e$ and m_e is the electron rest mass. According to the fitting, one can see that the screening effect follows the 2D model when the thickness is less than 2.4 nm (3L WSe_2), suggesting a weak interlayer coupling interaction at lower thickness. However, the 2D fitting is hardly acceptable when the thickness increases further, indicating that the interlayer coupling interaction becomes strong. The three-dimensional (3D) fitting, considering interlayer coupling interaction, can be described as Eq. (3)[28,29].

$$\Delta V(D) = \frac{1}{2}\left(\frac{6\pi^2\hbar^3}{N_sN_v d m_{||}\sqrt{m_\perp}}\right)^{\frac{2}{3}}\left(\frac{25\beta_\perp d\sigma_0^2}{8e^2}\right)^{2/5} \times \frac{1 - r_D}{\left(1 - r_D^{5/2}\right)^{2/5}}, \tag{3}$$

where $m_\perp = \hbar^2/2t_\perp d^2$, $t_\perp = 0.2eV$ ($t_\perp$: interlayer hopping parameter), $\beta_\perp = \left(4e^2/5\varepsilon_0\varepsilon\right)\left(N_sN_v d m_{||}\sqrt{m_\perp}/6\pi^2\hbar^3\right)^{2/3}$, and r_D can be numerically solved from Eq. (4):

$$\left[\frac{25\beta_\perp d\sigma_0^2}{8\left(1 - r_D^{5/2}\right)}\right]^{-1/10}\int_{r_D}^{1}\frac{du}{\left(u^{5/2} - r_D^{5/2}\right)^{1/2}} = \sqrt{\frac{2\beta_\perp}{d}}D. \tag{4}$$

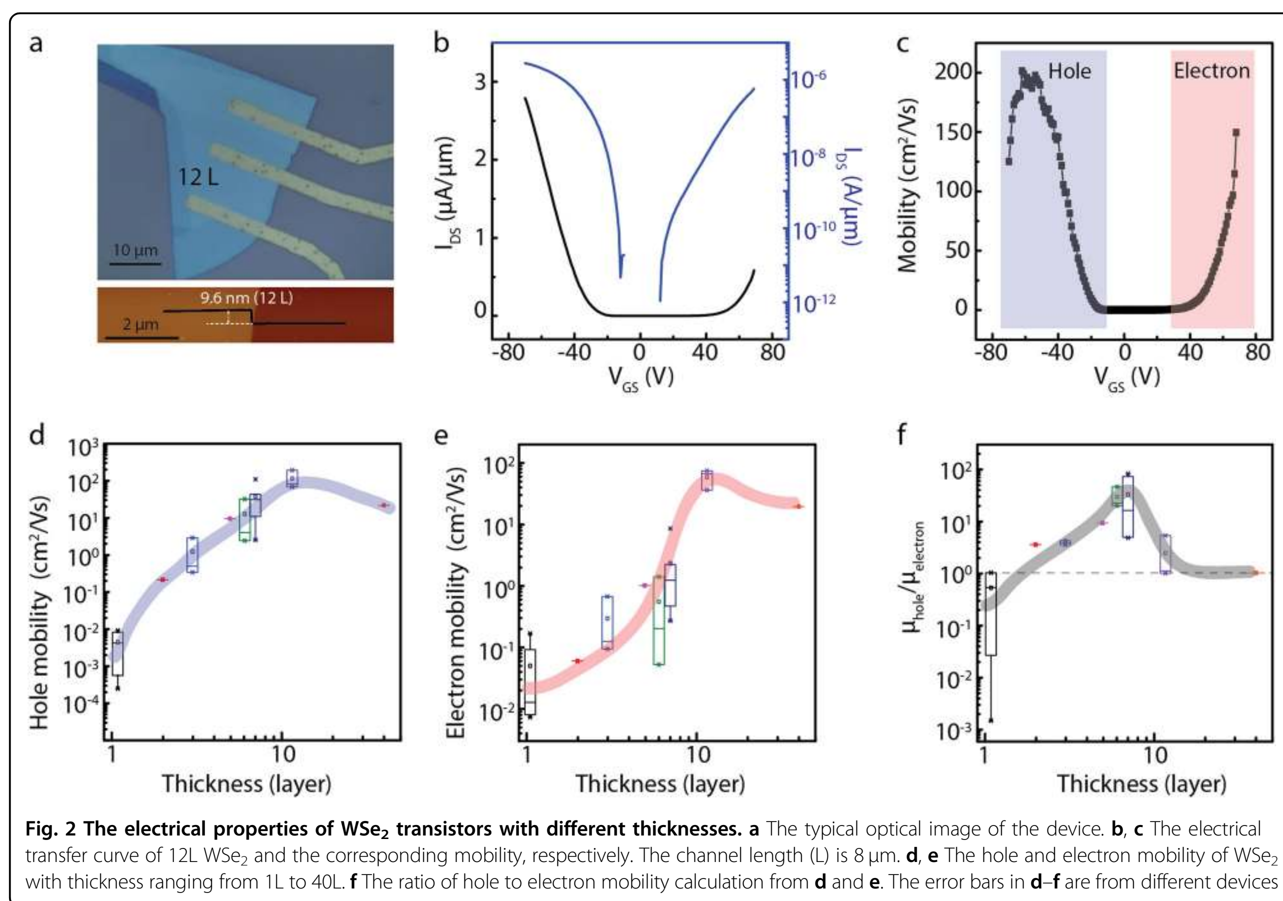

Fig. 2 The electrical properties of WSe_2 transistors with different thicknesses. a The typical optical image of the device. **b**, **c** The electrical transfer curve of 12L WSe_2 and the corresponding mobility, respectively. The channel length (L) is 8 μm. **d**, **e** The hole and electron mobility of WSe_2 with thickness ranging from 1L to 40L. **f** The ratio of hole to electron mobility calculation from **d** and **e**. The error bars in **d**–**f** are from different devices

The red line in Fig. 1g, h shows the 3D fitting, where $\sigma_0 = 0.8 \times 10^{13}\,\text{cm}^{-2}$ and $m_{||} = 0.01m_e$, respectively. One can see that the 3D fitting has much better consistency with the EFM results, particularly for the thicker region, indicating that WSe_2 is mostly in a strong coupling regime, which will apparently be reflected in the electrical transport mechanism.

In order to explore the thickness-dependent transport behavior of WSe_2, back-gated field effect WSe_2 transistors (FETs) were fabricated, where Ti/Au instead of traditional p-type Pd/Au or Pt/Au contacts were deposited to form ambipolar contact. Figure 2a shows the optical image of the 12L WSe_2 transistor. The transfer curve at room temperature (RT) is shown in Fig. 2b, indicating a typical ambipolar transport behavior, where the hole is the dominant carrier when $V_{GS} < -15$ V and the electron is the dominant carrier when $V_{GS} > +15$ V. The ambipolar behavior results from the shifting of the Fermi level under the electric field, which is attributed to the weak Fermi-level pinning at the metal/WSe_2 interface. Figure 2c shows the gate voltage-dependent field effect mobility, which is calculated by $\mu = (L/WC_0V_{DS})(dI_{DS}/dV_{GS})$, where C_0 is the capacity and L and W are the channel length and width, respectively. The maximum hole mobility and electron mobility are 196 and 150 cm^2/V s when the gate voltage is −56 and +70 V, respectively. The balanced electron and hole transport characteristic results from the similar n-type and p-type Schottky barrier because Fermi level is closer to the middle level between the conduction band and valence band. Figure 2d, e shows the thickness-dependent results for hole mobility and electron mobility, where the mobility is extracted in both positive/negative 50–60 V ranges of gate voltages for hole mobility (μ_h) and electron mobility (μ_e), respectively. With the dimensionality increase from 2D (monolayer) to 3D (12L), both hole mobility and electron mobility increase. The mobility increase should be related to both the increased density of state inducing a smaller Schottky barrier (discussed later in Fig. 3d) and the screened interfacial charged impurities inducing a weaker scattering[31]. Moreover, the bandgap of WSe_2 decreases as the thickness increases[32], which is also one of the key reasons for the enhancement of electrical performance.

When the thickness is 40L, both the hole mobility and electron mobility decrease to ~20 cm^2/V s, which should be caused by the increased series resistances associated with an increasing number of interlayers[33]. Fig. 2f shows the thickness-dependent μ_h/μ_e, which is the important

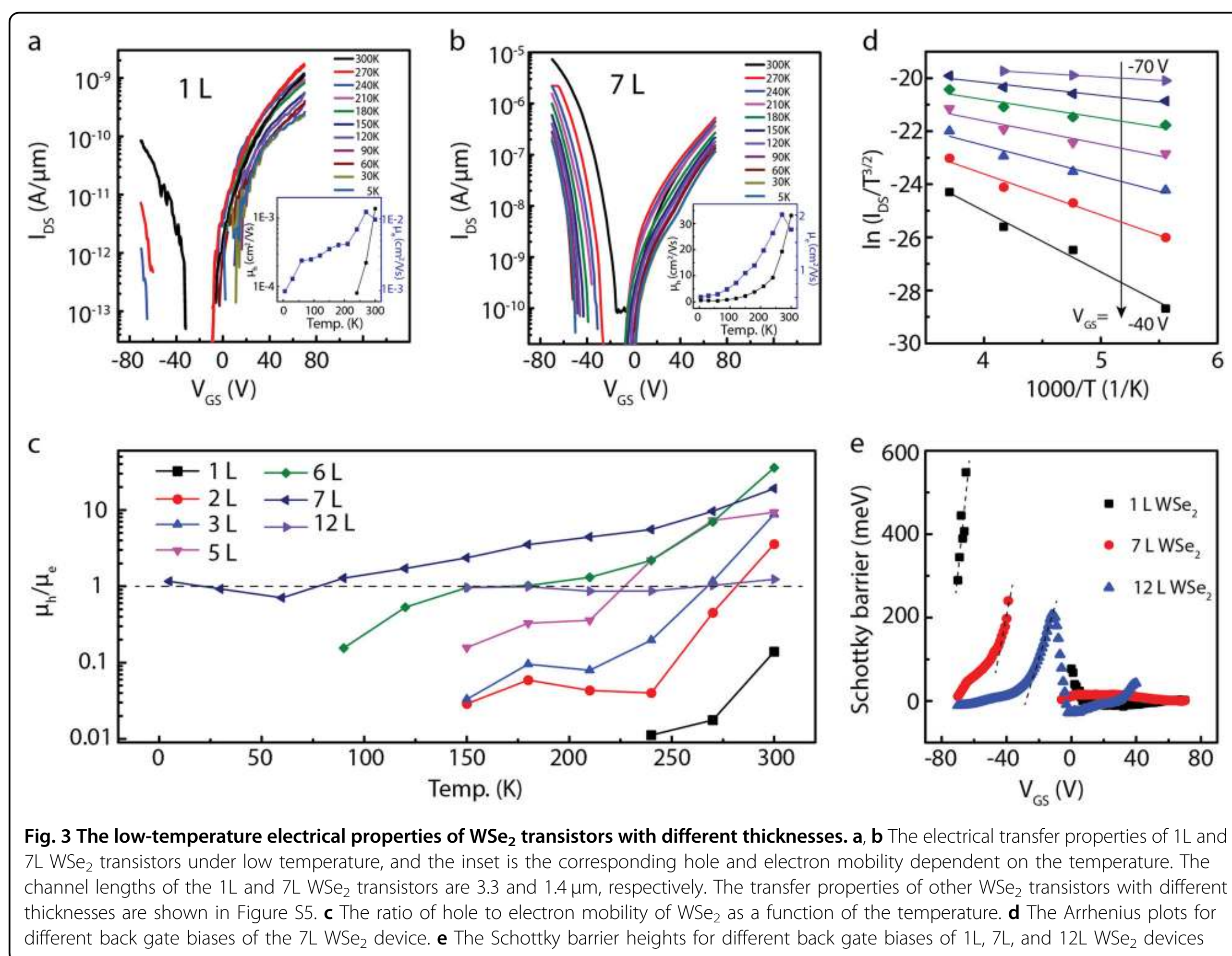

Fig. 3 The low-temperature electrical properties of WSe_2 transistors with different thicknesses. a, **b** The electrical transfer properties of 1L and 7L WSe_2 transistors under low temperature, and the inset is the corresponding hole and electron mobility dependent on the temperature. The channel lengths of the 1L and 7L WSe_2 transistors are 3.3 and 1.4 µm, respectively. The transfer properties of other WSe_2 transistors with different thicknesses are shown in Figure S5. **c** The ratio of hole to electron mobility of WSe_2 as a function of the temperature. **d** The Arrhenius plots for different back gate biases of the 7L WSe_2 device. **e** The Schottky barrier heights for different back gate biases of 1L, 7L, and 12L WSe_2 devices

factor for evaluating the symmetric transport characteristic. The ratio of μ_h/μ_e for 1L WSe_2 is approximately 0.1, indicating an electron dominant transport characteristic, which implies that the hole carrier is almost suppressed by the interfacial charged impurities and has a more sensitive response than that of the electron carrier. For 2L and 3L WSe_2, the ratio of μ_h/μ_e is approximately 3 and further increases to ~30 for 6L and 7L WSe_2, which should result from the fast increase of hole mobility attributed to the screened interfacial charged impurities (Fig. 1). From 7L to 12L, the ratio of μ_h/μ_e decreases to approximately 1, corresponding to the balanced ambipolar transport behavior, which should result from the faster increase of μ_e (Fig. 2e) caused by the lower Schottky barrier height for the electron injection. In a 40L WSe_2 transistor, the ratio of μ_h/μ_e is ~1, which suggests that the transport properties for the hole and electron carriers are same. The transport behavior (n-type or p-type) is not only dependent on the interfacial state but also dependent on the work function of metal contact. For the interfacial state, in combination with the EFM results (Fig. 1), we can propose that the channel region with thinner thickness has a higher effect from the interfacial charged impurities, and thus the hole carrier is suppressed, inducing n-type behavior. As the thickness increases, the interfacial charged impurities are screened, which makes the WSe_2 flakes display intrinsic property. Alternately, the metal contact is also another critical role in transport. Pudasaini et al.[34] reported that the carrier type can evolve from p-type to ambipolar to n-type in WSe_2 using Cr (the work function of Cr is 4.6 eV) contact with increasing channel thickness. In thinner WSe_2, the hole conduction appears dominant because the aligned Fermi level of thinner WSe_2/Cr contact is below the middle of the bandgap. In this study, the lower work function of Ti (~4.3 eV)[35] and the higher Schottky barrier height in the hole transport region can induce the preferential electron dominant conduction in thinner WSe_2. This phenomenon is in line with the previous reported preferential n-type in thinner WSe_2 with low-work-function metals, such as Ni, In, and Ag[24,35]. The requirement for real application of ambipolar semiconductor is not only the balanced hole and electron

carrier but also the higher carrier mobility. Although the ratio of μ_h/μ_e in 2L WSe_2 is close to 1, the electron mobility and hole mobility are relatively lower. Thus, the balanced hole and electron transport with higher mobility could be achieved in 12L WSe_2, which could satisfy the requirement for practical ambipolar application.

To gain insight into the ambipolar transport behavior, the electrical properties of WSe_2 transistors with different thicknesses are measured from RT to 5 K. The typical transfer curves of 1L and 7L WSe_2 are shown in Fig. 3b (others are shown in Supplementary Figure S5). As seen in the 1L WSe_2 transistor, the hole branch is almost completely gone, meaning that it is an insulator when the temperature decreases to 210 K, while the electron branch still exists. Interestingly, it is 60 K when the hole branch is fully suppressed in the 2 L WSe_2 transistor. Further, in the 7 L WSe_2 transistor, it is obviously seen that both the hole and electron branches exist until the temperature cools to 5 K. The corresponding temperature-dependent mobility is inserted, where one can see that the electron mobility slightly increases and then decreases, while the hole mobility rapidly decreases during cooling. The electron mobility shows a peak attributed to the dominant scattering switching from phonon scattering to charged impurities scattering during cooling. This phenomenon is also observed in electron-dominant back-gated MoS_2 transistors[36]. Alternately, the hole mobility is monotonously and rapidly decreasing during cooling, implying that both the phonon and charged impurities scattering strongly effect the hole carrier, which is in line with the hole-dominant graphene transistor[37].

Figure 3c shows the ratio of μ_h/μ_e as the function of temperature in WSe_2 transistors with thickness ranging from 1L to 12L. We would simply separate the dominant transport mechanism by $\mu_h/\mu_e = 1$ as shown by the dashed line in Fig. 3c, and thus, the dominant carrier is the hole when $\mu_h/\mu_e > 1$, while the dominant carrier is the electron when $\mu_h/\mu_e < 1$. In 1–7L WSe_2 transistors, the ratios of μ_h/μ_e almost decrease with temperature, which should be caused by the faster decrease of hole mobility originating from the relatively stronger scattering on the hole carrier compared to the relatively weaker scattering on the electron carrier. In detail, the ratios of μ_h/μ_e for WSe_2 transistors monotonously decrease across the dashed line for 2L, 3L, 5L, and 6L at 280, 267, 228, and 80 K, respectively, which means that the dominant carrier is switched from hole carrier to electron carrier during cooling. The different converted temperatures in WSe_2 transistors with different thicknesses are possibly attributed to their different scattering levels. Different from 1L–6L WSe_2 transistors, the ratio of μ_h/μ_e for the 7L WSe_2 transistor decreases from ~15 at 300 K to ~1 at 80 K and then saturates to 1. The hole and electron mobility as a function of temperature is shown in the inset of Fig. 3b, where the hole mobility decreases faster than the electron mobility. When the temperature is lower than 80 K, both the hole and electron mobility trend toward saturation, which is distinct from the evolution of hole and electron mobility in 1L–6L WSe_2, where hole conduction rapidly decreases or even disappears. Therefore, from 7L WSe_2, the electronic transport behavior trends toward an intrinsic property, whereby the dominant scattering is originated from the scattering center of the material rather than from interfacial charged impurity. Finally, the ratio of μ_h/μ_e in the 12L WSe_2 transistor is approximately 1, implying that the influence of scattering on the hole or electron carrier is similar. The 12L WSe_2 transistor with balanced ambipolar behavior originates from the bulk effect since the interfacial charged impurities are screened.

As known, the mobility behavior of a 2D material at low temperature is correlated with the contact metal but more significantly dependent on the scattering mechanism. Coulomb scattering originating from the interfacial charged impurity is one of the key scattering mechanisms. Although the interfacial charged impurity can be screened by introducing high-k dielectric, ion-gel, and BN[23,27,36,38], the complex fabrication and higher cost need to be taken into consideration. Interestingly, the hole branch in the 1L WSe_2 transistor disappears, suggesting that the effect of interfacial charged impurities on the hole carrier is much stronger than that on the electron carrier, while the interfacial charged impurity is screened in the 7L WSe_2 transistor and leads to a similar effect on hole mobility and electron mobility.

Even for the samples that have be held in high vacuum overnight before electron beam evaporation, the TiO_x buffer layer between Ti/Au contact and WSe_2 may also be formed[39,40], which will induce the formation of dipoles and further tune the Schottky barrier height. Thus, the transport property cannot be predicted by simple band offset, and, therefore, it is worth estimating the Schottky barrier to further reveal the thickness-dependent band profile. To evaluate the Schottky barrier height between metal and WSe_2, I_{DS} could be defined by 2D thermionic emission (Eq. (5)) due to its sufficiently thin channel[41].

$$I_{DS} = A^*_{2D} T^{3/2} exp\left(\frac{\phi_B}{k_B T}\right)\left[1 - exp\left(\frac{eV_{DS}}{k_B T}\right)\right], \quad (5)$$

where A^*_{2D} is the 2D equivalent Richardson constant, T is the absolute temperature, k_B is the Boltzmann constant, and ϕ_B is the effective Schottky barrier. The temperature dependence of the I_{DS}–V_{BG} curve could be re-plotted with Arrhenius formation $\left(ln\left(I_{DS}/T^{3/2}\right) \sim 1000/T\right)$ as shown in Fig. 3d (7L WSe_2). The effective Schottky barrier could be obtained from the slope of the Arrhenius plot. Figure 3e shows the effective Schottky barrier as a

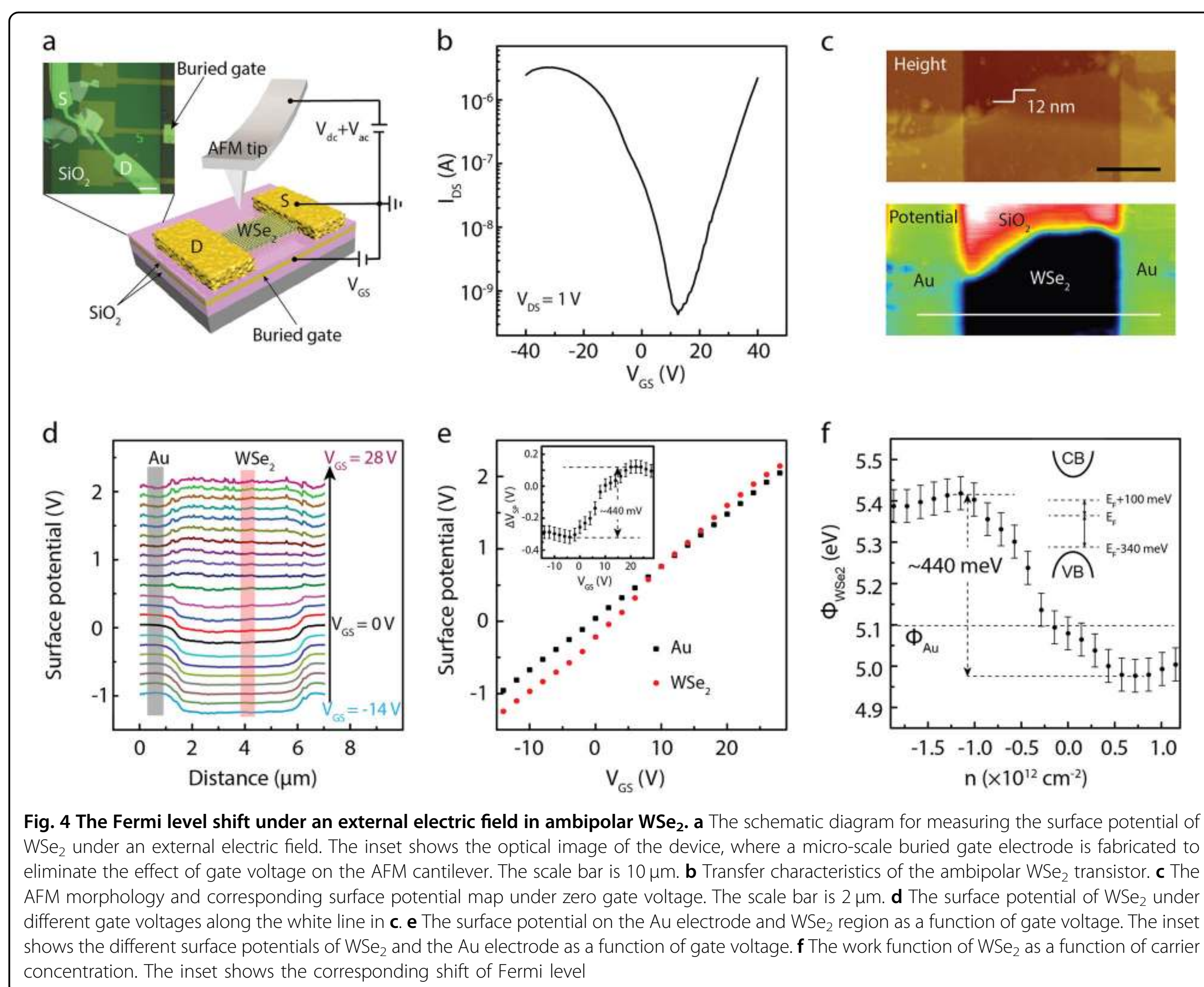

Fig. 4 The Fermi level shift under an external electric field in ambipolar WSe_2. a The schematic diagram for measuring the surface potential of WSe_2 under an external electric field. The inset shows the optical image of the device, where a micro-scale buried gate electrode is fabricated to eliminate the effect of gate voltage on the AFM cantilever. The scale bar is 10 μm. **b** Transfer characteristics of the ambipolar WSe_2 transistor. **c** The AFM morphology and corresponding surface potential map under zero gate voltage. The scale bar is 2 μm. **d** The surface potential of WSe_2 under different gate voltages along the white line in **c**. **e** The surface potential on the Au electrode and WSe_2 region as a function of gate voltage. The inset shows the different surface potentials of WSe_2 and the Au electrode as a function of gate voltage. **f** The work function of WSe_2 as a function of carrier concentration. The inset shows the corresponding shift of Fermi level

function of the gate voltage of 1L, 7L, and 12L WSe_2 devices. A peak between −10 and 0 V in the 7L WSe_2 device is attributed to the opposite polarities of Schottky contact, which could be tuned based upon the gate voltage[41]. As seen, the effective Schottky barrier for the hole carrier is strongly dependent on the gate voltage compared to that for the electron carrier. Knowingly, the effective Schottky barrier for the hole is obviously reduced as the WSe_2 thickness increases, while there is no noticeable change in the electron carrier. The above study demonstrates that 12L WSe_2 exhibits good ambipolar behavior with balanced carrier mobility in a broad temperature range from RT to low temperature.

The above study reveals that the carrier of WSe_2 can be effectively switched between electron and hole by a tunneling external electric field, corresponding to exhibit n-type and p-type behaviors, respectively. To reveal the ambipolar behavior of WSe_2, the work function change and Fermi level shift of WSe_2 are studied under different gate voltages. Here, in situ Kelvin probe force microscopy (KPFM) is employed to measure the contact potential difference between the tip and the sample, V_{CPD}, which is referred to as the surface potential (V_{SP})[42]. To reduce the unscreened effect of gate voltage on the AFM cantilever, the gate electrode with a size of 20 μm is buried under the SiO_2 layer. The WSe_2 flake is transferred on the surface, and then source/drain electrodes are fabricated by electron beam lithography, as shown in Supplementary Figure S6. Figure 4a shows the schematic diagram of the setup for surface potential measurement, where the electrostatic force between the cantilever and sample is nullified by applying a DC bias.

Figure 4b shows the transfer characteristic of the WSe_2 device exhibiting typical ambipolar behavior. The charge neutrality point is located at 12 V, which is due to the interfacial state between WSe_2 and sputtered SiO_2. The height and corresponding surface potential of the device are shown in Fig. 4c. The line profiles under

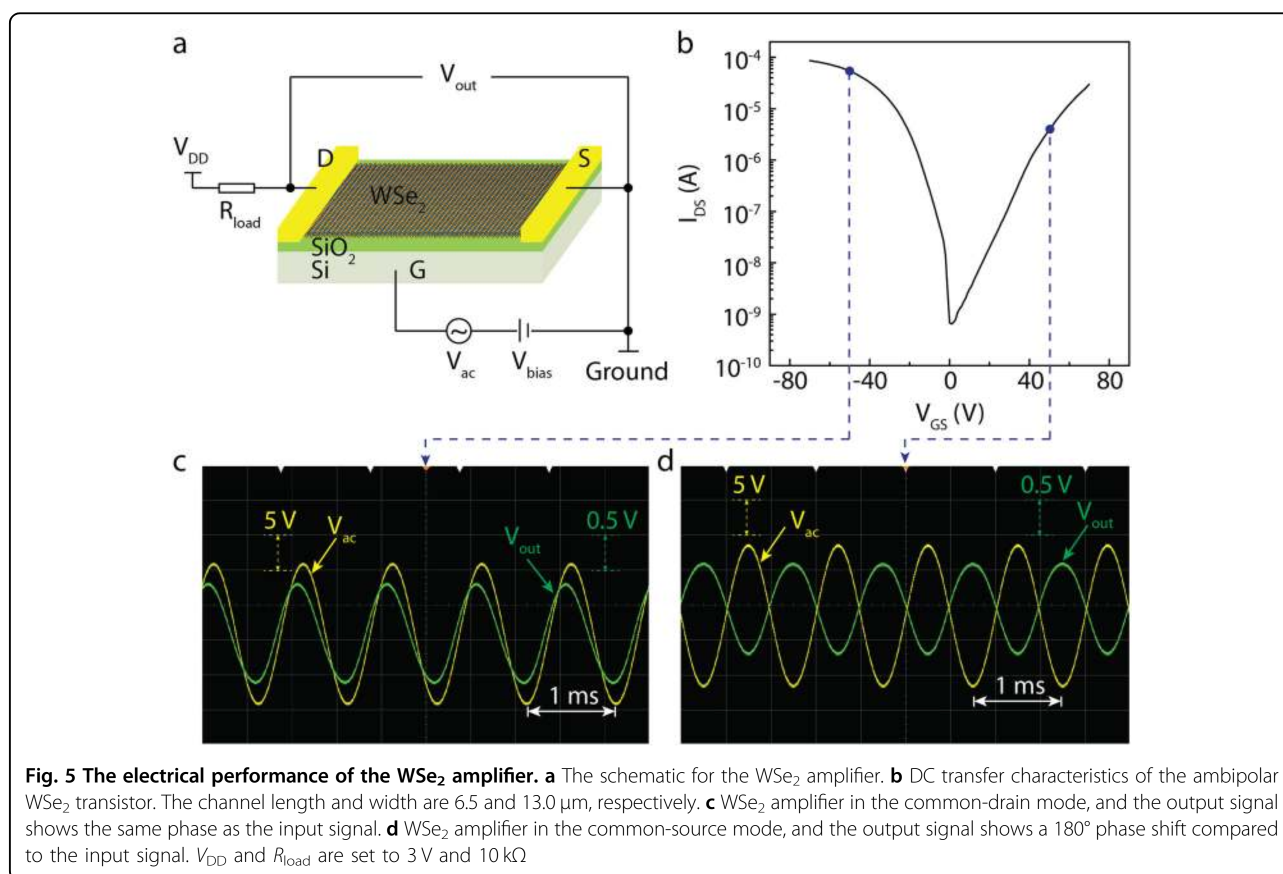

Fig. 5 The electrical performance of the WSe_2 amplifier. a The schematic for the WSe_2 amplifier. **b** DC transfer characteristics of the ambipolar WSe_2 transistor. The channel length and width are 6.5 and 13.0 µm, respectively. **c** WSe_2 amplifier in the common-drain mode, and the output signal shows the same phase as the input signal. **d** WSe_2 amplifier in the common-source mode, and the output signal shows a 180° phase shift compared to the input signal. V_{DD} and R_{load} are set to 3 V and 10 kΩ

different gate voltages along the white line in Fig. 4c are shown in Fig. 4d. As seen, the shift of the background is due to the unscreened electrostatic interaction between the AFM cantilever and the buried gate voltage[43]. It has been reported that the gate voltage will not influence the surface potential of a metallic electrode; therefore, the background signal could be subtracted to obtain the relative surface potential change of WSe_2, as shown in Fig. 4e. The surface potential difference ΔV_{SP} between WSe_2 and the Au electrode can be calculated by $\Delta V_{SP} = V_{SP_WSe_2} - V_{SP_Au}$, where $V_{SP_WSe_2}$ and V_{SP_Au} are the surface potentials of WSe_2 and Au, respectively. As seen in Fig. 4e, ΔV_{SP} changes from ~−0.330 to ~0.100 V when the gate voltage varies from −14 to 28 V. A sudden change of ΔV_{SP} (Fig. 4e) is observed at the charge neutrality point (V_D), where the gate voltage is 12 V. The rapid change of ΔV_{SP} is also reported in graphene, which may be related to the different electronic structures of the valance band and conductive band[43]. As known, the surface potential recorded by the KPFM could be formatted by $eV_{SP} = \emptyset_{tip} - \emptyset_{sample}$, where $\emptyset_{tip}$ and $\emptyset_{sample}$ are the work functions of the AFM tip and sample[42], respectively. Thus, the surface potential change is related to the work function: $e\Delta V_{SP} = \emptyset_{Au} - \emptyset_{WSe_2}$, where $\emptyset_{Au}$ and $\emptyset_{WSe_2}$ are the work functions of Au and WSe_2, respectively. Here, we assume that the work function of Au is 5.1 eV[44,45], and therefore, the work function of WSe_2 could be directly calculated by $\emptyset_{WSe_2} = \emptyset_{Au} - e\Delta V_{SP}$. Figure 4f shows the work function of WSe_2 ($\emptyset_{WSe_2}$) as a function of carrier concentration, where the carrier concentration is calculated by $n = C_0(V_{GS} - V_D)/e$. For this particular device, it is seen that $\emptyset_{WSe_2}$ could be tunneled by ~440 meV when WSe_2 switches between n-type and p-type transport behaviors. Namely, the Fermi level will upshift by 100 meV when the WSe_2 transmits from an insulator to an n-type semiconductor and downshift by 340 meV when the WSe_2 transmits from an insulator to a p-type semiconductor, as shown in the inset of Fig. 4f.

As studied above, the WSe_2 transistor displays typical ambipolar behavior with reasonable electron mobility and hole mobility, which has the potential for practicable use in communication[7]. As proof of the concept, the 12L WSe_2 transistor is employed to demonstrate two basic functions of analog circuits. The schematic of the WSe_2 amplifier is illustrated in Fig. 5a, where the supply voltage V_{DD} is set to 3 V, and the off-chip resistor R_{load} is 10 kΩ. As seen, the gate voltage (V_{GS}) is hence equal to the sum of a fixed DC bias voltage (V_{bias}) and a small sinusoidal AC signal (V_{ac}, $V_{PP} = 10$ V, $f = 1$ kHz). The DC transfer

curve of the WSe_2 transistor at RT is shown in Fig. 5b, which displays balanced electron and hole transport. The output signal (V_{out}) of the WSe_2 amplifier is monitored on an oscilloscope as shown in Fig. 5c, d, corresponding to negative and positive V_{bias}, respectively. When a negative V_{bias} is applied to the WSe_2 amplifier (Fig. 5c), in the positive phase of V_{ac}, I_{ds} increases/decreases as V_{GS} decreases/increases, so the voltage drop across the off-chip resistor will increase/decrease, respectively[46,47]. As a consequence, the corresponding V_{out} will decrease/increase, which exhibits the same phase as the input signal. This situation is called the common-drain mode. Similarly, when V_{bias} is positive in the n-type branch, the corresponding V_{out} will increase/decrease as V_{GS} decreases/increases, respectively, which exhibits a phase difference of 180° compared to V_{ac} (Fig. 5d). This situation is called the common-source mode. Therefore, it is clear that the working mode of the WSe_2 amplifier could be easily controlled by DC bias voltage. Two fundamental modes in a single WSe_2 transistor demonstrate that one can develop other WSe_2-based complicated analog circuits for signal processing performance with simplified circuit designs.

Conclusion

In summary, EFM is employed to investigate the electric-field screening effect of WSe_2 with a thickness range of 1–40 layers. The effective surface potential as a function of thickness is investigated in combination with non-linear Thomas–Fermi theory. The results show that the dielectric screening behavior follows a 2D model when the thickness is less than 3L, while it follows a 3D model when the thickness is greater than 3L. Significantly, the electrical transport properties of WSe_2 transistors demonstrate that the WSe_2 transistor exhibits ambipolar behavior and the asymmetric transport characteristic with different layer thicknesses. By studying the thickness- and temperature-dependent transport behavior, we successfully demonstrate that 12L WSe_2 exhibits balanced ambipolar behavior with higher electron and electron mobility from RT to low temperature. Furthermore, the ambipolar behavior of WSe_2 is studied by in situ KPFM to reveal its work function change/Fermi level shift as a function of gate voltage. The results show that the work function/Fermi level will be tunneled by 440 meV when WSe_2 switches between n-type and p-type WSe_2. Finally, the analog circuit composed of ambipolar 12L WSe_2 transistors exhibits good controlled-phase performance, demonstrating its practical communication application in 2D electronics.

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