The Analysis and Improvement of a Current-Steering DACs Dynamic SFDR—I: The Cell-Dependent Delay Differences

Tao Chen, *Student Member, IEEE,* and Georges G. E. Gielen, *Fellow, IEEE*

***Abstract*—For a high-accuracy current-steering digital-to-analog converters (DACs), the delay differences between the current sources is one of the major reasons that cause bad dynamic performance. In this paper, a mathematical model describing the impact of the delay differences on the DACs SFDR property is presented. The results are verified by comparison to behavioral-level simulations and to actual measurement data from published papers. Based on this analysis, the *delay differences cancellation* (DDC) technique to reduce the impact of the delay differences on the SFDR property is proposed and verified by simulation results.**

***Index Terms*—Current-steering digital-to-analog converters (DACs), delay differences cancellation (DDC), delay difference, delay distribution, spurious-free dynamic range (SFDR), switch-and-latch cell, switching sequence.**

I. Introduction

FOR TODAY'S digital-to-analog converters (DACs), higher and higher accuracy and speed are required. Such DACs are typically implemented as current-steering DACs. For a DAC with an accuracy higher than 12 bits, its spurious-free dynamic range (SFDR) property has become one of the major limiting factors for its performance [1]–[5]. There are quite a lot of non-ideal factors which will impact the DACs SFDR property. Some work has been done to explore the physical reasons of the deterioration of the SFDR. In [6] and [7], the impact of the current sources' limited output impedance for current-steering DACs is analyzed. As a conclusion, this limited output impedance will deteriorate the SFDR for high-accuracy high-speed DACs, especially when the single-ended output is used [7]. This conclusion can be verified by the model provided in [8].

The delay-related nonlinearities are another kind of main contributors to the bad dynamic property. Our previous paper [9] proposes a method for analyzing this kind of nonlinearities. The results of the analysis show that the delay-related nonlinearities can indeed limit the dynamic performance of a high-accuracy high-speed DAC if one does not apply any special techniques to solve this problem.

Based on their different causes, two kinds of delay differences in a high-accuracy current-steering DAC can be distinguished. One is the *cell-dependent* delay differences, and the other is the *output-dependent* delay differences.

Manuscript received December 14, 2004; revised April 18, 2005. This paper was recommended by Associate Editor J. Silva-Martinez.

The authors are with ESAT-MICAS, Katholieke Universiteit Leuven, Heverlee 3001, Belgium (e-mail: tao.chen@esat.kuleuven.be)

Digital Object Identifier 10.1109/TCSI.2005.854409

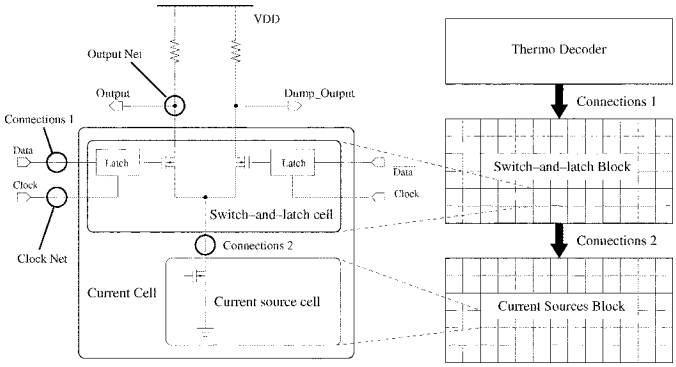

Fig. 1. Schematic of a current cell and the floorplan of the layout.

When the accuracy of a current-steering DAC increases, the number of current cells[1] increases, and it will be more and more difficult to let all these current sources have the same delay from the clock pad or to the output pad under the condition of keeping a reasonable layout aspect ratio. Fig. 1 shows the floorplan of the DAC and the schematic of a current cell. All the switch-and-latch cells are connected to the same output pad and the same clock pad. The delays from the clock pad to the switch-and-latch cells, or the delays from the switch-and-latch cells to the output pad, are determined by the length of the connection wire, as shown in the two circles in Fig. 1, and has nothing to do with the output value. We call this kind of delays the *cell-dependent delays*. Due to the different positions of the switch-and-latch cells (not the current-source cells) on the layout, the delays are different from cell to cell. For a DAC with a number of bits higher than 14, the delay differences may be as high as dozens of picoseconds in today's mainstream CMOS technologies. This is the physical reason for the cell-dependent delay differences.

Besides the cell-dependent delays, another kind of the delay differences is the *output-dependent* delay differences, whose delay values will depend on the output value, instead of the physical position of the current cells. The basic schematic of a current source used in the current-steering DACs is shown in Fig. 2(a). (Note that the current source or the switch transistor could also be cascoded.) Normally the switch transistors work in saturation region (when on) or cutoff region (when off). The voltage of the internal node X will change when changing the drain voltage of the *on* transistor because of the limited output

[1]From now on, the phrase "current cell" means the whole unit cell of the DAC, i.e., the current source together with the switches and latches. The phrase "current-source cell" only means the current source transistor, and "switch-and-latch cell" means the switches and latches. See Fig. 1.

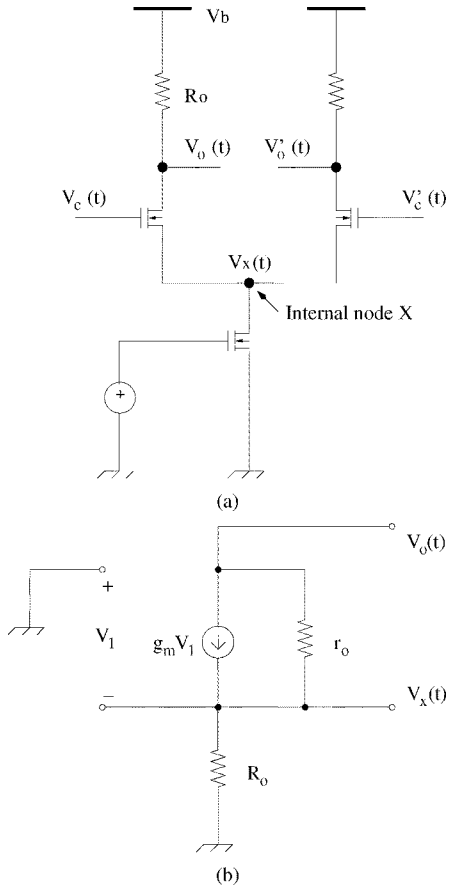

Fig. 2. Voltage variation of the internal node. (a) Schematics. (b) Small-signal equivalent circuit.

impedance of the switch transistor. Thus, the variation of the output voltage will cause a small variation of V_x, which will result in a change of the next switching time. Fig. 2(b) shows the small-signal equivalent circuit. The transistor which is off is omitted. When the output impedance of the (cascoded) current source R_o is very large, with *KCL* the equation below can be obtained

$$\frac{V_o - V_x}{r_o} = g_m V_x \Longrightarrow V_x = \frac{V_o}{1 + g_m r_o} \tag{1}$$

where g_m and r_o are the transconductance and the output impedance of the switch transistor respectively. This is the physical reason of the output-dependent delay differences.

As the first part (part I) of our study, this paper will only focus on the analysis and improvement of the cell-dependent delay differences. However, our calculations show that the same method can also be applied to the analysis of the output-dependent delay differences to get meaningful results. The analysis and improvement of the output-dependent delay differences will be proposed in the part II of this paper.

This paper is organized as follows. In Section II, the method used in [9] is explained in full detail to analyze the impact of the delay differences in the clock net on the SFDR of the DAC. Formulas with clear physical meaning are derived, and are compared to the measurement results from a published paper [1]. Next, this method is extended in Section III to analyze the delay differences in the output net. The impact of the return-to-zero (RZ) output stage on the cell-dependent delay differences will then be analyzed in Section IV. The intrinsic advantage of the RZ stage in reducing the impact of the delay differences on the SFDR can be observed from the results of the analysis. In Section V behavioral-level simulations are presented and the results are compared to the results of the mathematical model. Section VI proposes the delay-difference-cancellation (DDC) technique to overcome the cell-dependent delay differences. Our simulations show that the cell-dependent delay differences will not impact the SFDR any more with this technique. The DDC technique paves the way to the design of current-steering DACs with high dynamic accuracy (> 14 bits). Finally, Section VII summarizes the paper and draws conclusions.

II. Delay Differences on the Clock Net and its Mathematical Analysis

For the cell-dependent delays, the delay values are determined by the position of the current cell on the layout, while the delays in both the two differential output ends are the same. This means that taking the differential output will not reduce the nonlinearity caused by this kind of delay differences, and the second-order harmonic distortion is the dominant distortion which will determine the SFDR deterioration. In this section, the second-order distortion of a DACs single-ended output will first be calculated. Then we will calculate the amplitude of the signal frequency. From these results, the expression of the SFDR can be obtained.

A. Second-Order Distortion Caused by the Delay Differences on the Clock Net

For a current-steering DAC without RZ output stage,[2] the output of the current sources are added directly to the output current of the DAC; the delay differences among these current sources will reflect on the output current directly.

Consider one of the current sources i with clock delay d_i. Assume it is switched on in the nth sampling cycle. Then its output current is

$$I_{i,n}(t - d_i) = 1 - \exp\left(-\frac{t - nT_s - d_i}{\tau}\right),\ nT_s \le t \le (n+1)T_s \tag{2}$$

where T_s is the sampling period, τ is the time constant decided by the DACs load. The amplitude is set to be one. This is a simplified expression, the internal poles of the current cell have been omitted. But this is sufficient to get meaningful results.

The distortion of this current source is thus

$$\delta_{i,n}(t) = I_{i,n}(t) - I_{i,n}(t - d_i) \simeq \frac{d_i}{\tau}\exp\left(-\frac{t - nT_s}{\tau}\right),\quad nT_s \le t \le (n+1)T_s. \tag{3}$$

Assume the DACs input is a sinusoidal signal

$$f_{\text{in}}(t) = 2^{N-1}[\sin(\omega_0 t) + 1] \tag{4}$$

where N is the DACs number of bits. The amplitude is set so that the amplitude of every unit current source is 1.

[2]Current-steering DACs with RZ output stage will be analyzed later in Section IV.

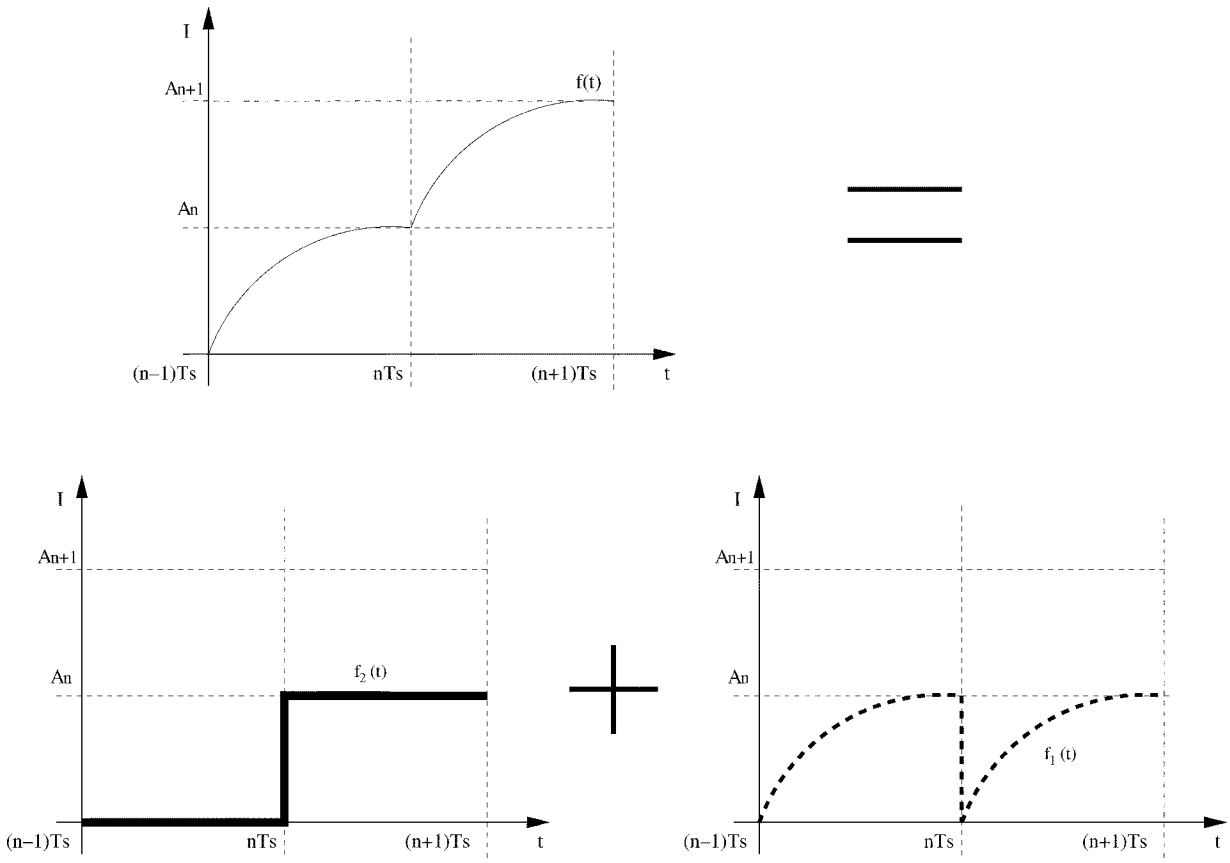

Fig. 3. DACs output signal without RZ output stage.

For a high-resolution DAC, ignoring the discrete nature of the output signal, the ideal output of the DAC in the period from $t = nT_s$ to $t = (n+1)T_s$ can be expressed as

$$A_n \simeq 2^{N-1}\left[\sin\left(\omega_0 n T_s\right) + 1\right] \tag{5}$$

$$A_{n+1} \simeq 2^{N-1}\left[\sin\left(\omega_0 (n+1) T_s\right) + 1\right]. \tag{6}$$

During this period the DACs total distortion is

$$\begin{aligned}\Delta_n(t) &= \sum_{i=A_n}^{A_{n+1}} \delta_{i,n}(t) \\ &\simeq \sum_{i=A_n}^{A_{n+1}} \frac{d_i}{\tau} \exp\left(-\frac{t - nT_s}{\tau}\right) G_{T_s}\left[t - \frac{2n+1}{2} T_s\right]\end{aligned} \tag{7}$$

where (3) has been used, and

$$G_{T_s}(t) = \begin{cases} 1, & \text{when } -\frac{T_s}{2} \le t \le \frac{T_s}{2} \\ 0, & \text{else} \end{cases} \tag{8}$$

is a square function.

In order to simplify the calculations, only linearly-distributed delays are considered for now. That is

$$d_i = ai \tag{9}$$

where a is a constant. Two assumptions are contained in this approximation. First, the delay values are integer times of a. (We will refer to this condition as linearly distributed delay values or simply LDDV assumption later.) Second, the current cells are switched on in the same order as their delay increases (referred to as linear switching sequence or LSS assumption). The LDDV assumption does not exist in a real DAC, but as will be seen in Section V, it has little impact on the result, so it is justifiable to adopt this assumption to simplify the derivation. What will impact the SFDR is actually the distribution of the delay values rather than the values themselves. The delay distribution is determined by the switching sequence of the switch-and-latch cells[3] when the input code step by step changes from the minimum value to the maximum value. Here, the LSS assumption is one of the possible cases in a real DAC and it leads to an interpretable analytic result. For the cell-dependent delays, when the positions of the switch-and-latch cells in the switch-and-latch block are decided, the delay values for the corresponding current cells are fixed, but the designer can still decide the delay distribution freely by arranging the actual switching sequence of the switch-and-latch cells. We will see later from the simulation results in Section VI that the LSS case is one of the worst delay distributions.[4] However, through the analysis of this worst case, we will obtain the optimized delay distribution and the corresponding optimized switching sequence of the switch-and-latch cells.

[3]Note that the switching sequence of the switch-and-latch cells can be different from the switching sequence of the current source cells.

[4]Actually, what we simulated and optimized in Sections V and VI is the distribution of the delays in the output net. But we will see later that the delay differences in both the clock net and the output net impact the SFDR in a similar way [see (23) and (46)].

Using (9) into (7), with a little calculation we can get the result for the DACs total distortion in the nth time window

$$\Delta_n(t) = \frac{a}{\tau}\exp\left(-\frac{t-nT_s}{\tau}\right)G_{T_s}\left[t-\left(n+\frac{1}{2}\right)T_s\right] \bullet \frac{A_{n+1}^2 - A_n^2 + A_{n+1} + A_n}{2}. \quad (10)$$

Define the function $M(t)$ as

$$M(t) = \frac{a}{\tau}\exp\left(-\frac{t}{\tau}\right)G_{T_s}\left[t-\frac{T_s}{2}\right]. \quad (11)$$

As will be seen later, $M(t)$ determines the amplitudes of the distortion components at different frequencies. Then (10) can be simplified to

$$\Delta_n(t) = M(t-nT_s)\frac{A_{n+1}^2 - A_n^2 + A_{n+1} + A_n}{2}. \quad (12)$$

With (5) and (6), we can get

$$\begin{aligned}\Delta_n(t) = \frac{M(t-nT_s)}{2}\{&2^{2N-2}\sin(2\omega_0 nT_s + \omega_0 T_s)\sin\omega_0 T_s \\ &+ \left(2^{2N-1}+2^{N-1}\right)\sin\omega_0(n+1)T_s \\ &+ \left(2^{N-1}-2^{2N-1}\right)\sin\omega_0 nT_s + 2^N\}. \end{aligned} \quad (13)$$

Thus the DACs overall distortion is

$$\begin{aligned}\Delta(t) &= \sum_{n=-\infty}^{\infty}\Delta_n(t) \\ &= \frac{M(t)}{2} \circledast \Bigg\{ \left[2^{2N-2}\sin(2\omega_0 t + \omega_0 T_s)\sin\omega_0 T_s \right. \\ &\quad + \left(2^{2N-1}+2^{N-1}\right)\sin(\omega_0 t + \omega_0 T_s) + 2^N \\ &\quad \left. + \left(2^{N-1}-2^{2N-1}\right)\sin\omega_0 t\right]\sum_{n=-\infty}^{\infty}\delta(t-nT_s)\Bigg\} \end{aligned} \quad (14)$$

where "$\circledast$" is the convolution operator.

Since the distortion is very small compared to the signal amplitude for high-resolution converters, the distortion at the signal frequency can be neglected. Thus, only the second-order distortion must be considered[5]:

$$\Delta_{II}(t) = \frac{M(t)}{2} \circledast \left[2^{2N-2}\sin(2\omega_0 t + \omega_0 T_s)\sin\omega_0 T_s \sum_{n=-\infty}^{\infty}\delta(t-nT_s)\right]. \quad (15)$$

Applying the Fourier transform

$$\mathcal{F}\left[\sum_{n=-\infty}^{\infty}\delta(t-nT_s)\right] = \frac{2\pi}{T_s}\sum_{n=-\infty}^{\infty}\delta(\omega - n\omega_s) \quad (16)$$

$$\begin{aligned}\mathcal{F}\left[\sin(2\omega_0 t + \omega_0 T_s)\right] = {}& \pi j\left[\exp(-j\omega_0 T_s)\delta(\omega+2\omega_0)\right. \\ &\left. - \exp(j\omega_0 T_s)\delta(\omega-2\omega_0)\right] \end{aligned} \quad (17)$$

$$\mathcal{F}[M(t)] \equiv \mathcal{M}(\omega) = \frac{a\left[1-\exp\left(-\frac{T_s}{\tau}\right)\exp(-j\omega T_s)\right]}{1+j\omega\tau}. \quad (18)$$

[5]Results later on confirm that the second-order distortion is the dominating contribution if the signal frequency is not too high.

For the high-accuracy DACs of nowadays, it normally holds that

$$\exp\left(-\frac{T_s}{\tau}\right) \ll 1. \quad (19)$$

It meas that, the output settles well at the end of each sampling cycle.

Thus, (18) can be simplified into

$$\mathcal{M}(\omega) \simeq \frac{a}{1+j\omega\tau}. \quad (20)$$

With (16), (17), and (20), the Fourier transform of $\Delta_{II}(t)$ can be obtained

$$\begin{aligned}\Delta_{II}(\omega) = {}& \frac{2^{2N-3}\pi j\sin(\omega_0 T_s)}{T_s}\mathcal{M}(\omega) \\ &\sum_{n=-\infty}^{\infty}\Big[\exp(-j\omega_0 T_s)\delta(\omega - n\omega_s + 2\omega_0) \\ &- \exp(j\omega_0 T_s)\delta(\omega - n\omega_s - 2\omega_0)\Big]. \end{aligned} \quad (21)$$

This is a sequence of *Dirac functions* at the frequencies $n\omega_s \pm 2\omega_0$. What we are interested in is the component at frequency $2\omega_0$, its amplitude is

$$|\Delta_{II}(2\omega_0)| = \frac{2^{2N-3}\pi\sin(\omega_0 T_s)}{T_s}|\mathcal{M}(2\omega_0)|. \quad (22)$$

Using (20), we get

$$|\Delta_{II}(2\omega_0)| = \frac{2^{N-4}d_{\max}\omega_s\sin\left(\frac{2\pi\omega_0}{\omega_s}\right)}{\sqrt{1+(2\omega_0\tau)^2}} \quad (23)$$

where $d_{\max} = 2^N a$ is the maximum delay difference of the current cells. We see from this result that the second-order distortion is proportional to both the maximum delay difference $d_{\max}$ and the sampling frequency ω_s, and that there is a peak when the signal frequency ω_0 is near $\omega_s/4$. τ is the time constant of the output node. We see from (23) that a bigger τ results in a smaller second-order distortion.

B. Signal Amplitude and the SFDR of a DAC Without RZ Output Stage

In order to get the SFDR, the signal amplitude at ω_0 has to be calculated. For a DAC without RZ output stage, its output signal is shown in Fig. 3, where T_s is the sampling cycle, A_n and A_{n+1} are the DACs output values at time nT_s and $(n+1)T_s$, respectively, as defined in (5) and (6). $f(t)$ is the DACs output signal. It can easily be decomposed into two parts: $f_1(t)$ (the right bottom curve) and $f_2(t)$ (the left bottom curve) , that is

$$f(t) = f_1(t) + f_2(t). \quad (24)$$

Then we can get $f(t)$ by calculating $f_1(t)$ and $f_2(t)$, respectively.

Define the function $s(t)$ as

$$s(t) = \left[1-\exp\left(-\frac{t}{\tau}\right)\right]G_{T_s}\left(t-\frac{T_s}{2}\right) \quad (25)$$

where the square function $G_{T_s}(t)$ is defined in (8). Then $f_1(t)$ can be expressed as (ignoring the discrete nature of the output signal)

$$f_1(t) = s(t) \circledast \left\{ 2^{N-1} \left[\sin \omega_0 (t + T_s) - \sin \omega t \right] \sum_{n=-\infty}^{\infty} \delta(t - nT_s) \right\}. \quad (26)$$

Under the condition of (19), we get the Fourier transform of $s(t)$ as

$$\mathcal{S}(\omega) \simeq \frac{\sin \omega T_s}{\omega} - \frac{\tau}{1+\omega^2\tau^2} - j \left[\frac{1 - \cos \omega T_s}{\omega} - \frac{\omega \tau^2}{1+\omega^2\tau^2} \right]. \quad (27)$$

With (16), and (27), $f_1(t)$ s Fourier transform is obtained

$$\mathcal{F}_1(\omega) = \frac{2^N \pi \sin\left(\frac{\omega_0 T_s}{2}\right)}{T_s} \times \sum_{n=-\infty}^{\infty} \mathcal{S}(\omega) \left[\exp\left(j \frac{\omega_0 T_s}{2} \right) \delta(\omega - n\omega_s - \omega_0) + \exp\left(-j \frac{\omega_0 T_s}{2} \right) \delta(\omega - n\omega_s + \omega_0) \right]. \quad (28)$$

Now we calculate the Fourier transform of $f_2(t)$. It can be expressed as

$$f_2(t) = \left[2^{N-1} (\sin \omega_0 t + 1) \sum_{n=-\infty}^{\infty} \delta(t - nT_s) \right] \circledast G_{T_s}\left(t - \frac{T_s}{2} \right). \quad (29)$$

Applying the Fourier transform

$$\mathcal{G}(\omega) \equiv \mathcal{F}\left[G_{T_s}\left(t - \frac{T_s}{2} \right) \right] = \frac{\sin \omega T_s}{\omega} - j \frac{1 - \cos \omega T_s}{\omega}. \quad (30)$$

With the above equations, together with (16), we get the Fourier transform of $f_2(t)$ as

$$\mathcal{F}_2(\omega) = 2^{N-2} \omega_s \sum_{n=-\infty}^{\infty} \Big[j\mathcal{G}(n\omega_s - \omega_0)\delta(\omega - n\omega_s + \omega_0) - j\mathcal{G}(n\omega_s + \omega_0)\delta(\omega - n\omega_s - \omega_0) + 2\mathcal{G}(n\omega_s)\delta(\omega - n\omega_s) \Big]. \quad (31)$$

From (24), (28), and (31), the Fourier transform of $f(t)$ can be obtained

$$\mathcal{F}(\omega) = \mathcal{F}_1(\omega) + \mathcal{F}_2(\omega). \quad (32)$$

The amplitude of the component at the signal frequency ω_0 is

$$|\mathcal{F}(\omega_0)| = \left| 2^{N-1} \omega_s \sin\left(\frac{\omega_0 T_s}{2} \right) \exp\left(\frac{j\omega_0 T_s}{2} \right) \mathcal{S}(\omega_0) - j 2^{N-2} \omega_s \mathcal{G}(\omega_0) \right|. \quad (33)$$

Observing (27) and (30), the relation holds

$$\mathcal{S}(\omega) \simeq \mathcal{G}(\omega) - \frac{\tau}{1+\omega^2\tau^2} + j \frac{\omega\tau^2}{1+\omega^2\tau^2}. \quad (34)$$

Using this equation into (33) gives

$$|\mathcal{F}(\omega_0)| = 2^{N-1} \omega_s \left| \left[\sin\left(\frac{\omega_0 T_s}{2} \right) \exp\left(\frac{j\omega_0 T_s}{2} \right) - \frac{j}{2} \right] \mathcal{G}(\omega_0) + \frac{-\tau + j\omega_0\tau^2}{1+\omega_0^2\tau^2} \sin\left(\frac{\omega_0 T_s}{2} \right) \exp\left(\frac{j\omega_0 T_s}{2} \right) \right|. \quad (35)$$

With some calculations, (35) can be simplified into

$$|\mathcal{F}(\omega_0)| = 2^{N-1} \frac{\omega_s}{\omega_0} \sin\left(\frac{\omega_0 T_s}{2} \right) \frac{1}{\sqrt{1+\omega_0^2\tau^2}}. \quad (36)$$

Thus, we have obtained the amplitude of the signal frequency.

Combining (23) and (36), the SFDR of a current-steering DAC without RZ output stage due to cell-dependent delay differences caused by the clock net of the latches can be obtained as (assuming that the second-order distortion is dominant)

$$\mathrm{SFDR} = \frac{|\mathcal{F}(\omega_0)|}{|\Delta_{II}(2\omega_0)|} = \frac{4\sqrt{\frac{1+4\omega_0^2\tau^2}{1+\omega_0^2\tau^2}}}{d_{\max}\omega_0 \cos\left(\frac{\pi\omega_0}{\omega_s} \right)} \quad (37)$$

where $d_{\max} = 2^N a$ is the maximum delay difference of the current cells. We see from this expression that the SFDR will increase with decreasing delay differences ($d_{\max}$) of the current cells. This is consistent with our intuition. The most interesting thing about this result is the dependency of the SFDR on the signal frequency and the sampling frequency. Fig. 4(a) shows the SFDR-f_0 curve, where the signal frequency $f_0 (= \omega_0/2\pi)$ has been normalized to the sampling frequency $f_s (= \omega_s/2\pi)$. When the signal frequency increases from zero up to $f_s/2$, the SFDR will first decrease and then increase. When $f_0/f_s \approx 0.25$, the SFDR reaches its lowest value. This result will be verified with more detailed simulation results later in Section V.

The SFDR-f_s curve is shown in Fig. 4(b), where the sampling frequency f_s has been normalized to the signal frequency f_0. We conclude from this figure that, when the signal frequency is a constant, we can improve the SFDR by decreasing the sampling frequency. This is reasonable because, when the sampling frequency increases, the distortion in every sampling cycle appears with a higher frequency, thus deteriorating the DACs SFDR property. When the sampling frequency becomes even higher, the amplitude of the distortion in every sampling cycle is reduced, the total distortion will not increase much, thus, the SFDR will approach a constant value, as shown in the figure.

When the signal frequency is so low that $\omega_0\tau \ll 1$, (37) can be simplified into

$$\mathrm{SFDR} \simeq \frac{4}{d_{\max}\omega_0}. \quad (38)$$

This result shows that the SFDR will decrease with increasing signal frequency at a rate of about $-20\ \mathrm{dB/dec}$ when the signal frequency is low. This is consistent with [1]'s measurement (see

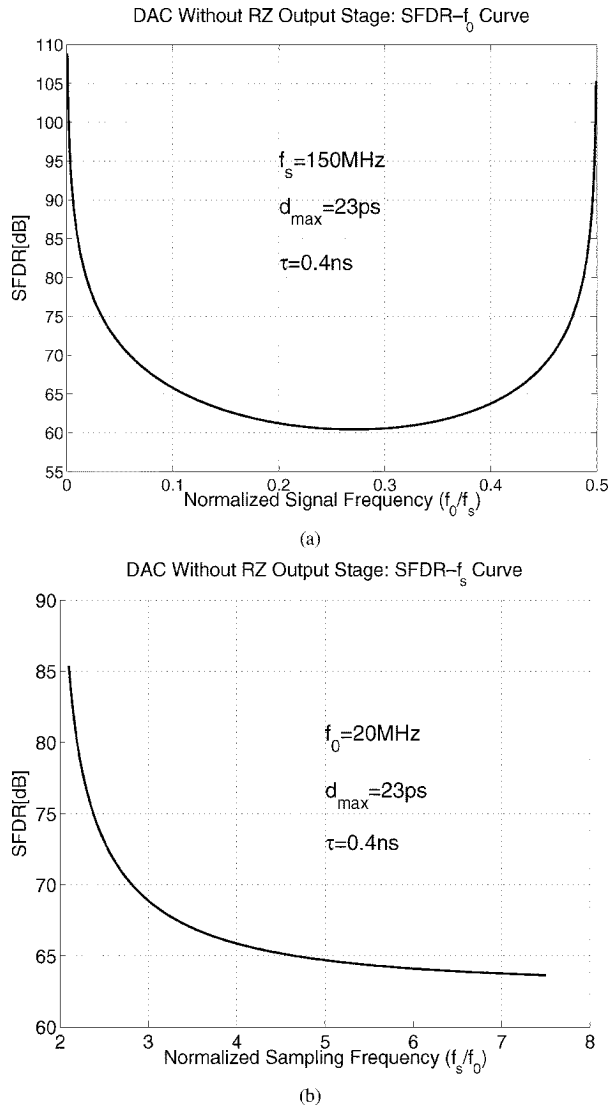

Fig. 4. Equation (37): the dependence of the SFDR on the signal frequency and the sampling frequency due to the delay differences on the clock net for a NRZ DAC. (a) SFDR-f_0 curve. (b) SFDR-f_s curve.

[1, Fig. 16]). Another conclusion which can be drawn from (38) is that, when the signal frequency is low enough, the DACs SFDR property will have nothing to do with the sampling frequency. In [1, Fig. 18], we can see that the DACs SFDR property is nearly constant provided that the sampling frequency is lower than 150 MHz. (If the sampling frequency becomes higher, the DAC will not be able to achieve 14 bits accuracy, thus the SFDR will decrease.) This result also verifies our analytic result.

With (38) we can estimate the maximum signal frequency a DAC can achieve under a given maximum delay difference. For an N-bit DAC, the SFDR it should achieve is at least $6.02N + 1.76$ dB [10]. So the relation below should be satisfied

$$\frac{4}{d_{\max}\omega_0} \geq 10^{(6.02N+1.76)/20} \Longrightarrow f_0 \leq \frac{2}{\pi d_{\max} 10^{(6.02N+1.76)/20}}. \tag{39}$$

For example, for a 14-bit DAC, when $d_{\max} = 23$ ps (extracted from the layout of a real DAC [1]), the maximum frequency it can achieve is only 1.39 MHz, even when all other nonlinearities are omitted. Of course, this result is based on the simplification of (9). However, our simulations in Section V with the actual delay values extracted from the layout obtain a result very close to this number. The reason will be analyzed in that section. Obviously, the cell-dependent delay difference may indeed deteriorate the DACs SFDR property seriously.

III. Delay Differences on the Output Net and its Mathematical Analysis

Now consider the second source of possible delay differences in a current-steering DAC, i.e., when the delays from the output of the switches to the DACs output pad are different (see Fig. 1). This difference can be described as a different time constant τ in (2). The distortion of the ith current source in the nth sampling cycle is

$$\begin{aligned}\delta_{i,n}(t) &= \left[1-\exp\left(-\frac{t-nT_s}{\tau}\right)\right] - \left[1-\exp\left(-\frac{t-nT_s}{\tau+\tau_i}\right)\right] \\ &= \exp\left[-\frac{t-nT_s}{\tau\left(1+\frac{\tau_i}{\tau}\right)}\right] - \exp\left(-\frac{t-nT_s}{\tau}\right), \\ &\quad nT_s \leq t \leq (n+1)T_s \end{aligned} \tag{40}$$

where τ_i is the variation of the time constant τ, and is much less than τ itself, say, $\tau_i \ll \tau$. With this condition, (40) can be simplified into

$$\begin{aligned}\delta_{i,n}(t) &\simeq \exp\left[-\frac{t-nT_s}{\tau}\left(1-\frac{\tau_i}{\tau}\right)\right] - \exp\left(-\frac{t-nT_s}{\tau}\right) \\ &= \exp\left(-\frac{t-nT_s}{\tau}\right)\left[\exp\frac{(t-nT_s)\tau_i}{\tau^2} - 1\right], \\ &\quad nT_s \leq t \leq (n+1)T_s. \end{aligned} \tag{41}$$

Since

$$0 \leq t - nT_s \leq T_s \qquad \tau_i \ll \tau$$

we have

$$\frac{(t-nT_s)\tau_i}{\tau^2} \leq \left(\frac{T_s}{\tau}\right)\left(\frac{\tau_i}{\tau}\right) \ll 1.$$

So, (41) can be further simplified into

$$\delta_{i,n}(t) \simeq \frac{(t-nT_s)\tau_i}{\tau^2}\exp\left(-\frac{t-nT_s}{\tau}\right), \quad nT_s \leq t \leq (n+1)T_s. \tag{42}$$

As in Section II-A, the total distortion in the nth sampling cycle is

$$\Delta_n(t) = \sum_{i=A_n}^{A_{n+1}} \delta_{i,n}(t) \simeq \sum_{i=A_n}^{A_{n+1}} \frac{(t-nT_s)\tau_i}{\tau^2}\exp\left(-\frac{t-nT_s}{\tau}\right) G_{T_s}\left[t-\left(n+\frac{1}{2}\right)T_s\right] \tag{43}$$

where A_n and A_{n+1} are defined in (5) and (6), and the function $G_{T_s}(t)$ is defined in (8).

Again, we assume the variation of the time constant, τ_i, to be linearly distributed

$$\tau_i = b\,i \tag{44}$$

where b is a constant. The LDDV and LSS assumptions are included in this equation just as in (9). Their impact on the results

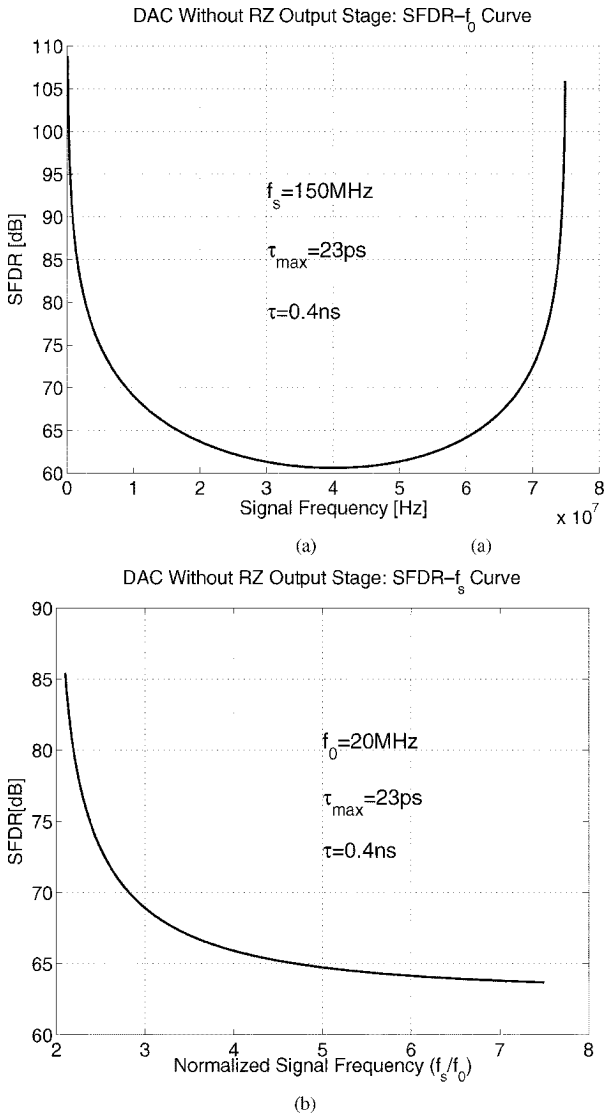

Fig. 5. Equation (46): the dependence of the SFDR on the signal frequency and the sampling frequency due to the delay differences on the output net for a NRZ DAC. (a) SFDR-f_0 curve. (b) SFDR-f_s curve.

is also similar to the case of the delay differences in the clock net, which has been discussed when we introduce (9).

With similar calculations as in Section II-A, we can get the amplitude of the second-order distortion as

$$|\Delta_{II}(2\omega_0)| = \frac{2^{2N-3}\pi b \sin(\omega_0 T_s)}{T_s[1+(2\omega_0\tau)^2]}. \tag{45}$$

Combining (36) and (45), the SFDR of a DAC without output stage due to output time constant differences is obtained as

$$\mathrm{SFDR} = \frac{|\mathcal{F}(\omega_0)|}{|\Delta_{II}(2\omega_0)|} = \frac{4\left[1+(2\omega_0\tau)^2\right]}{\tau_{\max}\omega_0 \cos\left(\frac{\pi\omega_0}{\omega_s}\right)\sqrt{1+\omega_0^2\tau^2}} \tag{46}$$

where $\tau_{\max}$ is the maximum time constant τ variation. This result is shown in Fig. 5. It is very similar to (37)'s result (see Fig. 4), i.e., the impact of the output time constant variation on the SFDR is similar to that of the clock delay difference. That means that the output time constant variation will impact the SFDR in the same way as the clock delay difference does. Thus,

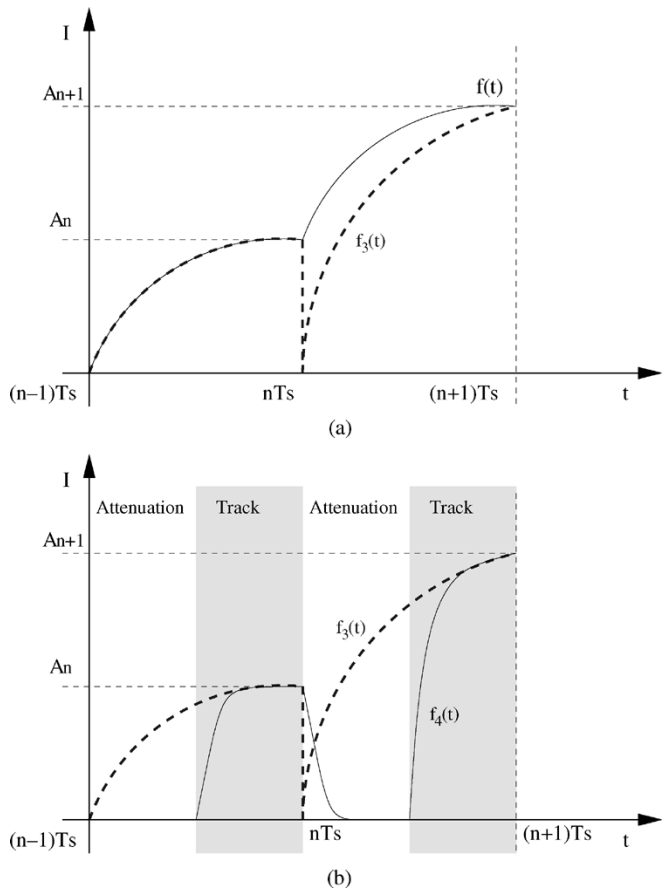

Fig. 6. RZ DACs output signal. (a) The simplified output signal $f_3(t)$. (b) The actual output signal $f_4(t)$.

when designing the layout of the switch-and-latch block, it is possible to let both delay differences cancel each other and thus reduce the whole delay variation.

IV. Impact of RZ Output Stage on Delay Differences

In [2] and [3], an RZ output stage was used to enhance the SFDR property by setting the output to a fixed value (ac ground) at the start of any transition. With this architecture, the output signal is divided into two phases in every clock cycle: the track phase and the attenuate phase. The output tracks the DAC output only during the track phase, and it is attenuated to a very low fixed value during the attenuate phase [2]. When the signal frequency increases, the SFDR property of such a DAC will decrease with a much slower rate compared to DACs without RZ output stage. In this section, a simplified ideal RZ output stage with attenuation time assumed to approach zero as shown in Fig. 6(a) will be analyzed as a worst-case situation to a real RZ DAC. The impact of the cell-dependent delay differences on the SFDR of such a DAC will be obtained. Since the delay differences on the clock net and the output net impact the SFDR in a similar way, only the delay differences on the clock net are analyzed in this section.

Fig. 6(a) shows the simplified output signal of an RZ DAC. In this figure, the curve $f_3(t)$ is the output of the RZ DAC. For comparison, a normal (without RZ output stage) DACs output signal $f(t)$ is also shown. Both the signal amplitude at frequency ω_0

and the amplitude of the second-order distortion have to be recalculated in order to get the SFDR. The curve $f_4(t)$ in Fig. 6(b) shows the output of an actual RZ DAC with nonzero attenuation time. We will discuss the impact of the attenuation time on the SFDR later.

Using the function $s(t)$ defined in (25), we can express $f_3(t)$ as

$$f_3(t)=s(t)\circledast\left\{2^{N-1}[\sin\omega_0(t+T_s)+1]\sum_{n=-\infty}^{\infty}\delta(t-nT_s)\right\}. \tag{47}$$

With calculations similar to Section II-B, the amplitude of the component at frequency ω_0 can be obtained as

$$|\mathcal{F}_3(\omega_0)|\simeq 2^{N-2}\frac{\omega_s}{\omega_0(1+\omega_0^2\tau^2)}\sqrt{\mathcal{T}(\omega_0)} \tag{48}$$

where

$$\begin{aligned}\mathcal{T}(\omega_0)=\omega_0^4\tau^4-2\sin\omega_0T_s\cdot\omega_0^3\tau^3+(3-2\cos\omega_0T_s)\omega_0^2\tau^2\\ -2\sin\omega_0T_s\cdot\omega_0\tau+(2-2\cos\omega_0T_s).\end{aligned} \tag{49}$$

The second-order distortion of such a DAC has to be recalculated too. Instead of (7), the total distortion of the nth cycle is now

$$\begin{aligned}\Delta_n'(t)&=\sum_{i=1}^{A_{n+1}}\delta_{i,n}(t)\\ &\simeq\sum_{i=1}^{A_{n+1}}\frac{d_i}{\tau}\exp\left(-\frac{t-nT_s}{\tau}\right)G_{T_s}\left[t-\left(n+\frac{1}{2}\right)T_s\right]\\ &=M(t-nT_s)\frac{A_{n+1}^2+A_{n+1}}{2}\end{aligned} \tag{50}$$

where $M(t)$ is defined in (11).

With calculations similar to Section II-A, we can get the amplitude of the second-order distortion as

$$|\Delta_{II}'(2\omega_0)|=2^{2N-5}\omega_s|\mathcal{M}(2\omega_0)|=\frac{2^{2N-5}\omega_s a}{\sqrt{1+2(\omega_0\tau)^2}}. \tag{51}$$

As we now have the signal amplitude [(48)] and the amplitude of the second-order distortion [(51)], the DACs SFDR can be obtained as

$$\mathrm{SFDR}'=\frac{|\mathcal{F}_3(\omega_0)|}{|\Delta_{II}'(2\omega_0)|}=\frac{8\sqrt{[1+2(\omega_0\tau)^2]\mathcal{T}(\omega_0)}}{d_{\max}\omega_0(1+\omega_0^2\tau^2)} \tag{52}$$

where $d_{\max}=2^N a$ is the maximum delay difference. Again, the SFDR property of such a DAC will increase with decreasing delay differences $d_{\max}$ of the current cells. But the frequency dependence is different from that of a DAC without RZ output stage. The SFDR-f_0 curve is shown in Fig. 7(a). We see that the SFDR will decrease with increasing signal frequency with a small slope. This is consistent with the measurement results in [2], [3], and [5]. Fig. 7(b) shows the SFDR-f_s curve resulting from (52). We see from this figure that the SFDR also decreases with increasing sampling frequency, but the reduction happens slower than in the case without the RZ output stage [see Fig. 4(b)].

For the RZ output stages with nonzero attenuation time [see the curve $f_4(t)$ in Fig. 6(b)], if ignoring the settling error at the end of the last track phase, the DACs output during the attenuation phase will not be impacted by the delay differences. The nonlinear distortion only exist in the track phase. According to (3), the nonlinear distortion decreases exponentially when reducing the time of the track phase. Meanwhile, the signal energy reduces linearly when reducing the time of the track phase. As a result, for an actual RZ output stage whose attenuation time is larger than zero, if the only nonlinearity that is taken into consideration is the cell-dependent delay differences, the SFDR should even be better than what we have obtained in (52).

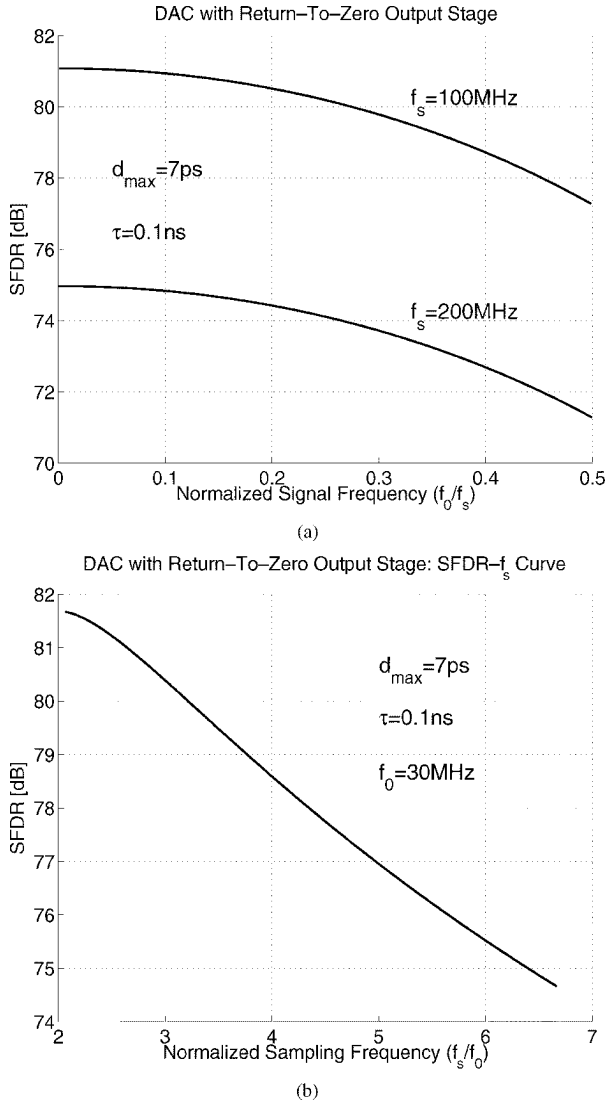

Fig. 7. Equation (52): the dependence of the SFDR on the signal frequency and the sampling frequency due to the delay differences on the clock net for a RZ DAC. (a) SFDR-f_0 curve. (b) SFDR-f_s curve.

When the signal frequency is so low that $\omega_0\tau\ll 1$, (52) can be further simplified into

$$\mathrm{SFDR}'=\frac{16\pi}{d_{\max}\omega_s}. \tag{53}$$

This result shows that when the signal frequency is low, the RZ DACs SFDR property will depend on the sampling frequency, instead of the signal frequency. This property is different from

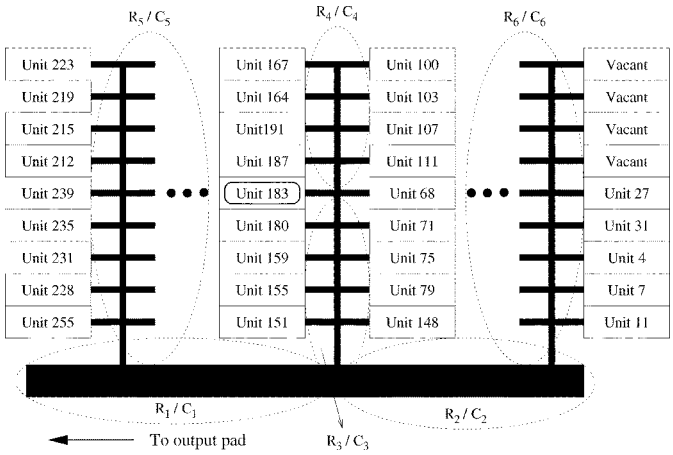

Fig. 8. Layout of the switch-and-latch block from [1].

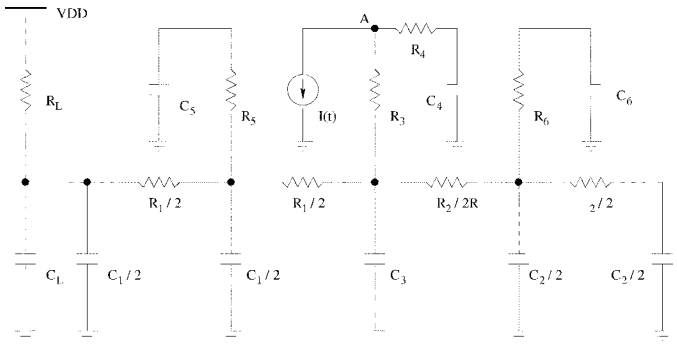

Fig. 9. Extracted circuit for calculating the delays.

Calculate the output current of each current source according to its position
For each transition, determine the current cells that will be switched on
Add up the output of the current cells that are switched on during this sampling cycle to get the current output
Do the same calculations to obtain the output in all the sampling cycles to get the output signal
Apply the FFT on the output signal to obtain the SFDR

Fig. 10. Flowchart of the SFDR simulation method.

that of a DAC without output stage [see (38)], the SFDR of which depends on the signal frequency instead of the sampling frequency.

V. Simulation Verification of Mathematical Model

According to the previous analysis, the delay differences on both the clock net and the output net will impact the SFDR in a similar way. Therefore, in our simulations we only consider the delay differences on the output net.

Fig. 8 shows the layout of the switch-and-latch block as extracted from a real DAC [1], which is used as illustrative example here. The clock net is not shown for simplification. We will simulate the behavior of every current cell, and then get the behavior of the whole DAC by adding up the current of all the current cells. In this figure, unit 183 is taken as an example. The resistances and the capacitors are the extracted parasitic resistances and capacitors of the actual wires on the layout. For the switch-and-latch cells in different positions, these parameters have different values, and will result in the delay differences on the output net.

The corresponding extracted circuits are shown in Fig. 9. As shown in Fig. 8, R_1, C_1 are the parasitic parameters of the main wire on the left side of unit 183. R_2 and C_2 are on the right side. R_5, C_5 are the parasitic parameters of all the branch wires on the left side of the branch wire where unit 183 is located, and R_6, C_6 are those on the right side. The parasitic parameters on the branch wire where unit 183 is located are divided into two parts. R_3, C_3 are on the bottom side, and R_4, C_4 are on the top side. Replacing unit 183 with a current source, we obtain the equivalent circuit of Fig. 9. In order to simplify the simulation, the R_5, C_5 subcircuit and the R_6, C_6 subcircuit are placed in the middle of the R_1, C_1 subcircuit and the R_2, C_2 subcircuit respectively. R_L and C_L are the load of the DAC. The point A is where the switch-and-latch cell is connected to the output net. The current source $It)$ describes the switching behavior of the current source. Ignoring the internal poles, $It)$ can be thought as an ideal step function when the current cell is switched on. The values of the resistances and the capacitances can be extracted from the layout. With this circuit model, we can calculate the output current caused by every current cell. When the clock transition happens, the output current of the DAC can be obtained by adding up the output currents of all the current cells which are turned on. Applying the same calculations to each sampling cycle, the total output signal can be obtained. Then the FFT analysis is applied to obtain the SFDR. The flowchart of the simulation method is shown in Fig. 10.

Fig. 11 shows the results of the simulations. For comparison, the calculation results of (46) are also shown as the thick curve without markers. The curve with the circle markers shows the simulation results. We see that both curves agree with each other well when the signal frequency is not so high. But when the signal frequency is higher than 72 MHz in the example of Fig. 11, the results of the calculation and simulation are becoming different: the simulated SFDR curve even flattens off. This is because at those frequencies the higher-order distortion dominates and makes the SFDR lower than the case when only the second-order distortion is considered, while in our mathematical model only the second-order distortion is taken into consideration. If we only consider the second-order distortion in the simulation, we will get the curve with triangle markers. It fits the calculation results much better at higher frequencies, and it also matches the total SFDR curve at lower frequencies, indicating that at lower frequencies indeed the second-order component dominates.

Our mathematical model is based on the very simplified assumptions [see (9) and (44)] and these assumptions do not exist

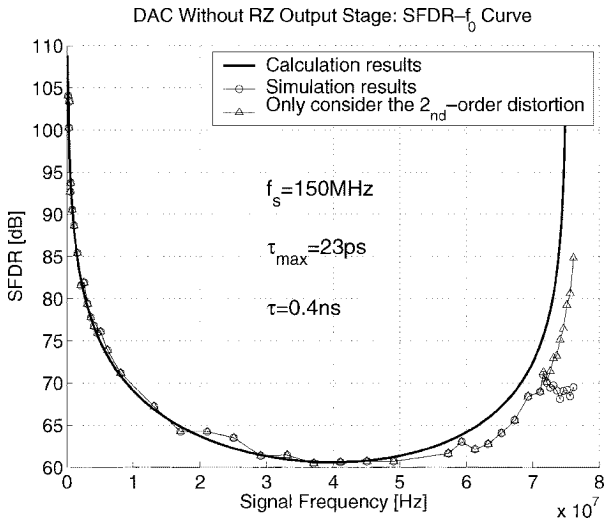

Fig. 11. Comparison of SFDR calculation and simulation results for a DAC without output stage [1].

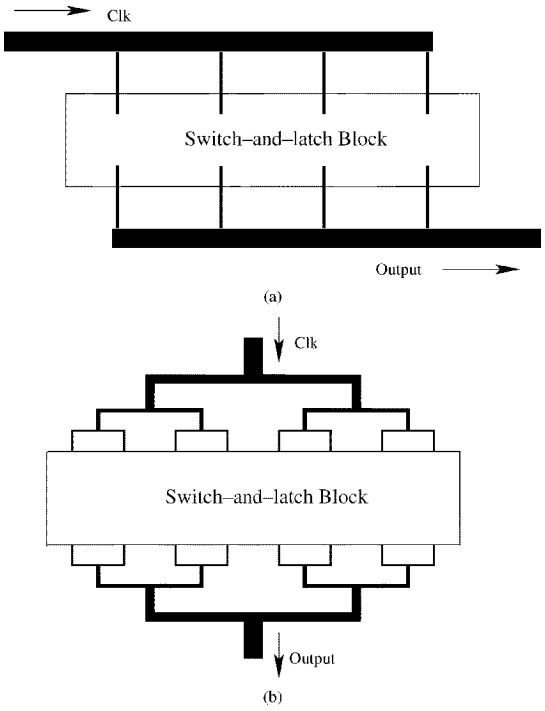

Fig. 12. Reduction of the cell-dependent delay differences. (a) Delay cancellation between the clock net and the output net. (b) Tree-like clock net and output net.

in real DACs. The reason why the simulation results fit the calculation result is that, in the chip [1] we used, the current cells are switched on nearly in the same order as their delays decrease [Fig. 13(a)], i.e., it approximately fits the LSS assumption defined in Section II-A. In such a case, the peak of the nonlinear distortion caused by the different delays appears twice in one sinusoidal cycle, and results in big second-order distortion, thus deteriorating the SFDR.

We will show in Section VI by simulations that the delay distribution (physically the switching sequence of the switch-and-latch cells) greatly affects the DACs SFDR property assuming that the delay difference values are fixed. Since it is hard for a high-accuracy DAC to reduce the delay differences of all the current cells through proper design and layout, finding a best delay distribution becomes a promising way to solve the SFDR problem.

VI. DDC Technique

As aforementioned, we can reduce the delay differences by making the delay differences on the clock net and those on the output net cancel with each other, as shown in Fig. 12(a). But the length differences in the clock net and in the output net will not result in exactly the same delay differences, therefore this method cannot solve the problem completely. Another possible solution is to use a tree-like connection for both the clock net and the output net as shown in Fig. 12(b). This method will inevitably increase the area and slow down the sampling frequency, and for high-accuracy DACs, the tree-like buses will make it difficult to get a reasonable aspect ratio.

The methods mentioned above work by reducing the values of the delay differences. In this section, we will present another method which will not change the delay difference values of the current cells. Instead, we will reduce the impact of the cell-dependent delay differences on the SFDR directly by properly choosing the switching sequence of the switch-and-latch cells. In this way, what is changed is the delay distribution instead of the values of the delay differences. It is to some degree similar to what has been done to the current source cells in order to achieve good INL static property in [1] and [11]. Fig. 1 shows the floorplan of a typical high-accuracy current-steering DAC. The connections between the thermodecoder block and the switch-and-latch block (connections 1 in the figure), together with the connections between the switch-and-latch block and the current source block (connections 2), provide enough freedom to the designers for realizing in the same chip both the optimum switching sequence in the current-source block for good static INL performance and the optimum switching sequence in the switch-and-latch block for good dynamic SFDR performance.

If we only take the distortion caused by the delay differences into consideration, two conclusions are justifiable based on the above analysis and simulations. First, to first-order approximation, the total distortion is the sum of all the distortions in every sampling cycle; in each cycle, the distortion is the sum of the distortions of every current cell that is switched on; and the distortion of a current cell in a sampling cycle is linearly proportional to the delay difference value of the current cell [see (3) and (42)]. Second, the second-order distortion dominates when the signal frequency is not too high. Correspondingly, there are two solutions to improve the SFDR property: to reduce the amplitude of the distortion in each sampling cycle, or to reduce the energy of the second-order distortion. Thus, we get two rules (we call them "the DDC rules") for arranging the switching sequence of the switch-and-latch cells

1) The amplitude of the distortion in every sampling cycle should be reduced to as low as possible. That means that the current cells with big delay values should neighbor the current cells with small delay values in the switching sequence.

TABLE I
POSITIONS OF SWITCH-AND-LATCH CELLS IN BLOCK

255	228	231	235	239	212	215	219	223
251	247	244	207	203	199	196	205	201
227	233	237	242	243	249	253	194	195
226	221	217	211	210	224	216	214	209
208	241	246	248	0	225	230	232	240
200	198	193	206	204	202	197	254	252
218	220	222	229	234	236	238	245	250
213	0	0	0	0	0	0	0	0
174	181	186	188	190	149	154	156	158
172	170	165	142	140	138	133	144	136
182	184	192	161	166	168	176	129	134
177	160	152	150	145	157	153	147	146
141	162	163	169	173	178	179	185	189
137	131	130	143	139	135	132	175	171
151	155	159	180	183	187	191	164	167
148	79	75	71	68	111	107	103	100
93	84	87	91	95	116	119	123	127
89	83	82	125	121	115	114	109	105
70	72	80	66	67	73	77	98	99
65	112	104	102	97	128	120	118	113
126	85	90	92	94	81	86	88	96
124	122	117	110	108	106	101	78	76
39	43	47	20	23	0	0	69	74
36	46	44	42	37	30	28	26	21
64	53	58	60	62	5	10	12	14
56	54	49	16	8	6	1	32	24
35	41	45	33	38	40	48	17	22
34	29	25	19	18	13	9	3	2
15	52	55	59	63	50	51	57	61
11	7	4	31	27	0	0	0	0

2) The distortion should appear with high frequency. That means that the current cells with big delay variations should be distributed as uniformly as possible. Thus, the energy of the lower-order distortion can be reduced.

Below we will illustrate these rules by an example.

The layout of the switch-and-latch block extracted from a real DAC [1] is shown in Fig. 8. The clock network in this chip is a tree-like net, the delay differences are very small compared to those caused by the output net, so it is not shown for reasons of simplification. The positions of the switch-and-latch cells in the matrix decide the actual delay values and are shown in Table I, where the numbers designate the switching sequence of the cells as used in [1]. (We will refer to it as "cell number" in this paper.) When the DAC is working, the unary current cells will turn on according to the order of the "cell number." The position of a number in the table designates its position in the switch-and-latch block. The number "0" means that the position is vacant. The delay values of each current cell can be calculated by the model presented in Section V. The normalized delay distribution is shown in Fig. 13(a). Obviously, they don not satisfy the assumptions of (9) and (44).

We see from Fig. 13(a) that in this chip the current cells with smaller cell numbers have greater delays. As a result, for a full-scale sinusoidal input signal, the distortion will have two peaks in every signal cycle, i.e., , the DAC will have a very big second-order distortion, and such a second-order distortion will determine the DACs SFDR property when the signal frequency is not too high (see Fig. 11). This conclusion is consistent with the previous analysis.

We can change the switching sequence by rearranging the positions of the switch-and-latch cells. Table II shows one possible rearrangement. The cells with consecutive cell numbers are put

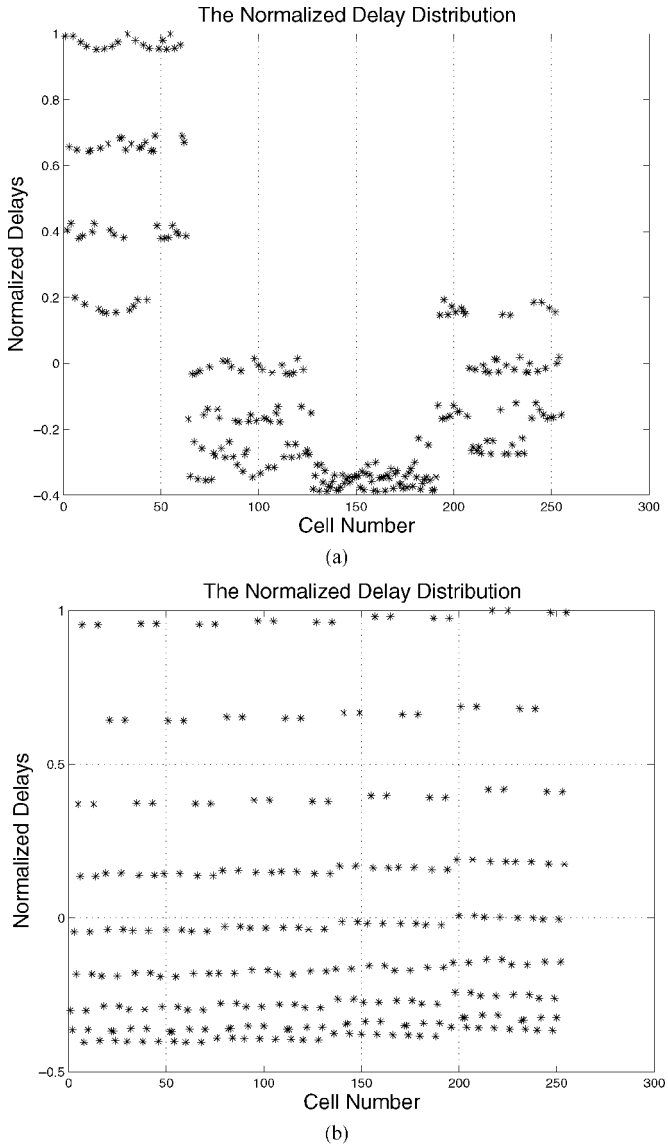

Fig. 13. Normalized delay distributions of the switch-and-latch cells from [1]. (a) Original distribution. (b) After the sequence rearrangement.

in the opposite place vertically to satisfy DDC rule 1. According to DDC rule 2, the cell numbers are uniformly distributed in the whole table. The corresponding delay distribution is shown in Fig. 13(b). The current cells with big delay deviation have been uniformly distributed among all the cell numbers, and every big delay cell is always neighbored by two cells with small delay values. So the DDC rules are satisfied by this arrangement.

Performing behavioral-level simulations as before on the "new" DAC, the SFDR results obtained are shown in Fig. 14, where the curve with circle markers is the case with the optimized switching sequence while still having the same delay values from the original layout [1]; the curve with right-pointing triangle markers shows the ideal case when there is no delay difference; the curve with upward-pointing triangle markers is the original case [1] before optimization; and the curves with asterisk markers are cases when uniformly distributed random switching sequences are applied. We see from these results that the rearrangement of the delay values can improve the DACs SFDR property significantly to a level that is very

TABLE II
OPTIMIZED POSITIONS OF SWITCH-AND-LATCH CELLS IN BLOCK

1	61	121	181	241	211	151	91	31
9	69	129	189	249	219	159	99	39
17	77	137	197	0	227	167	107	47
25	85	145	205	0	235	175	115	55
3	63	123	183	243	213	153	93	33
11	71	131	191	251	221	161	101	41
19	79	139	199	0	229	169	109	49
27	87	147	207	0	237	177	117	57
5	65	125	185	245	215	155	95	35
13	73	133	193	253	223	163	103	43
21	81	141	201	0	231	171	111	51
29	89	149	209	0	239	179	119	59
7	67	127	187	247	217	157	97	37
15	75	135	195	255	225	165	105	45
23	83	143	203	0	233	173	113	53
24	84	144	204	0	234	174	114	54
16	76	136	196	0	226	166	106	46
8	68	128	188	248	218	158	98	38
30	90	150	210	0	240	180	120	60
22	82	142	202	0	232	172	112	52
14	74	134	194	254	224	164	104	44
6	66	126	186	246	216	156	96	36
28	88	148	208	0	238	178	118	58
20	80	140	200	0	230	170	110	50
12	72	132	192	252	222	162	102	42
4	64	124	184	244	214	154	94	34
26	86	146	206	0	236	176	116	56
18	78	138	198	0	228	168	108	48
10	70	130	190	250	220	160	100	40
2	62	122	182	242	212	152	92	32

near to the ideal case without delay differences. Even the SFDR at high signal frequencies where the dominant harmonic distortion is higher than the second order is improved. This is because at these high signal frequencies the dominant harmonic distortion, though higher than the second order, is still a relatively low-order distortion (for example, the third-order), which is also reduced by the DDC technique together with the second-order distortion[6].

Under the condition of satisfying the DDC rules, i.e., a delay distribution similar to what is shown in Fig. 13(b), there may be lots of switching sequences of the switch-and-cell cells. Our simulations show that SFDR values very close to the ideal case with no delay differences can be obtained for all these switching sequences that satisfy the DDC rules. These results mean that with a DDC switching sequence the delay differences will have very little impact on the DACs SFDR property.

VII. CONCLUSION

Driven by signal processing and telecommunication applications, DACs with higher and higher accuracy and speed are required. As the accuracy and speed increase, some high-order distortions become important and impose additional constraints upon the designers. The impact of the current sources' limited output impedance on the SFDR has been well analyzed and can be solved for state-of-the-art DACs by using a differential output [6], [7]. Since most of the DACs nowadays are using differential output to achieve large output swing, no extra solution is needed to overcome the impact of the limited output impedance. However, even for DACs with differential output, our studies show that the delay-related nonlinearities still deteriorate the SFDR seriously.

[6]Actually the switching sequence (of the switch-and-latch cells) which can reduce the second-order distortion normally can also reduce the distortions that are slightly higher than the second-order. This can be observed from the results of the uniformly distributed random switching sequences in Fig. 14.

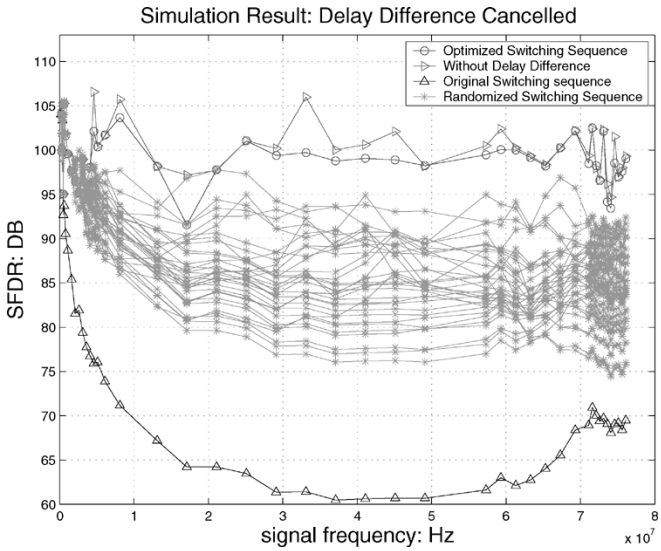

Fig. 14. Result of optimizing the switching sequence for a real design case ($f_s = 150$ MHz).

The impact of the cell-dependent delay differences on the SFDR of thermometercode-based current-steering DACs has been analyzed in this paper. Formulas with clear physical meaning have been derived and verified by both behavioral-level simulations and results described in published papers. The results are also justifiable for a segmented architecture, because in this architecture the thermometric part has a much more significant weight compared to the binary part and its delay differences will be the main contribution to the SFDR deterioration. According to our results, delay differences deteriorate the DACs SFDR property already at very low signal frequencies, and are thus one of the main reasons that may cause a bad SFDR property.

With the method proposed, the intrinsic advantage of the Return-to-Zero output stage in improving the SFDR property of a DAC has been analyzed and explained.

The DDC technique has been presented to reduce the impact of the cell-dependent delay differences on the SFDR. This technique makes use of the freedom in choosing the switching sequence of the switch-and-latch cells, and can improve the SFDR greatly with very low penalty on the layout area and complexity. The simulation results show that with the DDC technique, the DACs SFDR performance is very close to that of an ideal DAC which has no delay differences.

ACKNOWLEDGMENT

The authors would like to thank Dr. G. Van der Plas for his valuable discussions and suggestions.

REFERENCES

[1] G. Van der Plas, J. Vandenbussche, M. Steyaert, W. Sansen, and G. Gielen, "A 14-bit intrinsic accuracy Q^2 random walk CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1708–1718, Dec. 1999.

[2] A. R. Bugeja and B. Song, "A self-trimming 14-b 100-MS/s CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1841–1852, 2000.
[3] J. Hyde, T. Humes, C. Diorio, M. Thomas, and M. Figueroa, "A 300-ms/s 14-bit digital-to analog converter in logic CMOS," *IEEE J. Solid-State Circuits*, vol. 38, pp. 734–740, 2003.
[4] A. Van den Bosch, M. Borremans, M. Steyaert, and W. Sansen, "A 12 b 500 msample/s current-steering CMOS D/A converter," in *Proc. IEEE 2001 ISSCC*, vol. XLIV, Feb. 2001, pp. 366–367.
[5] Y. Cong and R. Geiger, "A 1.5 v 14 b 100 MS/s self-calibrated DAC," in *Proc. IEEE 2003 ISSCC*, vol. 1, Feb. 2003, pp. 128–482.
[6] A. Van den Bosch, M. Steyaert, and W. Sansen, "SFDR-bandwidth limitations for high speed high resolution current steering CMOS D/A converters," in *Proc. IEEE 1999 ISCAS*, 1999, pp. 1193–1196.
[7] S. Luschas and H. S. Lee, "Output impedance requirements for DAC's," in *Proc. IEEE 2003 ISCAS*, May 2003, pp. I–861–I–864.
[8] T. Chen and G. Gielen, "Modeling of the impact of the current source output impedance on the SFDR of current-steering CMOS DA converters," in *Proc. IEEE 2004 ISCAS*, May 2004.
[9] ——, "Analysis of the dynamic SFDR property of high-accuracy current-steering D/A converters," in *Proc. IEEE 2003 ISCAS*, May 2003, pp. I–973–I–976.
[10] S. Haykin, *An Introduction to Analog and Digital Communications*. New York: Wiley, 1989.
[11] Y. Cong and R. Geiger, "Switching sequence optimization for gradient error compensation in thermometer-decoded DAC arrays," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, no. 7, pp. 585–595, Jul. 2000.

Tao Chen (S'02) was born in Zhangping City, Fujian Province, P.R. China, in 1974. He received the B.S. degree in electronic engineering in 1996 from Zhejiang University, and in 1999, he received the M.S. degree, also in electronic engineering, from Tsinghua University, China.

From 1999 to 2000, he was an ASIC engineer at Huawei High-Tech Incoporation, Beijing, and then a chip design engineer with Capella Microsystem Incoporation, Beijing. Currently, he is a research assistant with the MICAS Laboratories, K.U. Leuven, Belgium. He is working toward the Ph.D. degree on the design of analog/mixed-signal integrated circuits.

Georges G. E. Gielen (S'87–M'92–SM'99–F'02) received the M.Sc. and Ph.D. degrees in electrical engineering from the Katholieke Universiteit Leuven, Leuven, Belgium, in 1986 and 1990, respectively.

From 1986 to 1990, he was appointed as a Research Assistant by the Belgian National Fund of Scientific Research. In 1990, he was appointed a Postdoctoral Research Assistant and Visiting Lecturer with the Department of Electrical Engineering and Computer Science, University of California, Berkeley. From 1991 to 1993, he was a Postdoctoral Research Assistant with the Belgian National Fund of Scientific Research, ESAT Laboratory, Katholieke Universiteit Leuven. In 1993, he was appointed as a tenure Research Associate of the Belgian National Fund of Scientific Research and also an Assistant Professor at the Katholieke Universiteit Leuven. In 1995, he was promoted to Associate Professor at the same university, where he is now a full-time Professor. His research interests are in the design of analog and mixed-signal integrated circuits, and especially in analog and mixed-signal CAD tools and design automation (modeling, simulation and symbolic analysis, analog synthesis, analog layout generation, analog and mixed-signal testing). He is coordinator or partner of several (industrial) research projects in this area. He has authored or coauthored one book and more than 250 papers in edited books, international journals, and conference proceedings.

Dr. Gielen was the 2004 President-Elect of the IEEE Circuits and Systems (CAS) Society. He has been an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: FUNDAMENTAL THEORY AND APPLICATIONS, and recently also of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING. He is also a member of the Program Committees of international conferences (ICCAD, DATE, ISCAS). He received the Best Paper Award of the Wiley *International Journal on Circuit Theory and Applications* in 1995. He was the 1997 Laureate of the Belgian National Academy of Sciences, Literature, and Arts, and is a member of the Editorial Board of the Kluwer *International Journal on Analog Integrated Circuits and Signal Processing*.