The BLIXER, a Wideband Balun-LNA-I/Q-Mixer Topology

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Abstract—This paper proposes to merge an I/Q current-commutating mixer with a noise-canceling balun-LNA. To realize a high bandwidth, the real part of the impedance of all RF nodes is kept low, and the voltage gain is not created at RF but in baseband where capacitive loading is no problem. Thus a high RF bandwidth is achieved without using inductors for bandwidth extension. By using an I/Q mixer with 25% duty-cycle LO waveform the output IF currents have also 25% duty-cycle, causing 2 times smaller DC-voltage drop after IF filtering. This allows for a 2 times increase in the impedance level of the IF filter, rendering more voltage gain for the same supply headroom. The implemented balun-LNA-I/Q-mixer topology achieves > 18 dB conversion gain, a flat noise figure < 5.5 dB from 500 MHz to 7 GHz, IIP2 $= +20$ dBm and IIP3 $= -3$ dBm. The core circuit consumes only 16 mW from a 1.2 V supply voltage and occupies less than 0.01 mm^2 in 65 nm CMOS.

Index Terms—CMOS integrated circuits, direct conversion, high-linearity mixer, linearity, low noise, low-noise amplifiers, low-power electronics, merged LNA and mixer, microwave integrated circuits, microwave receivers, multi-standard, noise canceling, noise cancellation, radio receivers, RF transceiver, software defined radio, software radio, UHF integrated circuits, wideband LNA, wideband matching, wideband receiver, wideband RF front-end, zero IF.

I. INTRODUCTION

WIDEBAND radio receivers have recently drawn significant research interest, e.g., for emerging software-defined radio (SDR) architectures and ultra-wideband (UWB) communication standards [1]–[3]. Such applications call for radio receivers covering the frequency range from a few hundred MHz up to about 6 GHz (SDR) or even 10 GHz (UWB). Co-operability with other communication devices (e.g., cellular, WLAN) operating in the same spectrum is mandatory, setting especially stringent demands on the wideband linearity of such a receiver. A single-ended RF input avoids the use of an external broadband balun and its accompanying losses. Compared to a differential input it also requires less switches

to connect the RF input to different RF filters and/or antenna networks [2].

Recently, some wideband balun-LNAs with high linearity have been proposed offering a wideband input match, gain and single-ended to differential conversion [4], [5]. Active mixers have a capacitive input impedance, i.e., the gate of a transistor. When a passive mixer is used, a voltage buffer or transconductance stage is often required between the LNA output and the input of the mixer(s). Also this intermediate stage between LNA and mixer loads the LNA capacitively. Due to this capacitance load, it is challenging to realize high LNA gain over a large bandwidth. Inductive peaking has been used to still achieve 6 GHz bandwidth [3], [6], however we would like to avoid the use of area consuming on-chip inductors in expensive nanometer scale CMOS processes. Moreover, the requirements on linearity in the input stage of a mixer will be higher than for the LNA, because of the voltage gain of the LNA. As the input signal of the mixer is still at a high frequency it is challenging to obtain high linearity there. For instance, negative feedback techniques are not very effective because loop gain is limited at GHz frequencies.

This paper proposes a solution to the above described problems via a so-called "BLIXER" topology. The topology actually comprises an active balun, LNA and mixer in a single circuit. Without bandwidth extension inductors, it still easily achieves more than 7 GHz bandwidth in 65 nm CMOS by merging a current commuting I/Q-mixer with a noise-canceling balun-LNA [7]. In this paper we explain the operation of the topology in detail and analyze its gain and noise behavior. Also we compare it to alternative topologies to illustrate its competitive performance.

The paper is structured as follows. Section II quickly reviews recently proposed balun-LNAs to show why it is challenging to simultaneously achieve high gain and high bandwidth. Then we introduce the BLIXER topology in Section III and show how it can simultaneously achieve high gain and high RF bandwidth. In Section IV, we analyze the gain and noise figure of the BLIXER in terms of component design parameters. Section V discusses the circuit implementation and measurement results, while Section VI draws conclusions.

II. BALUN-LNA GAIN AND BANDWIDTH LIMITATION

A. Balun-LNA Topology

Fig. 1 shows a balun-LNA consisting of a parallel operating common gate (CG) and common source (CS) stage. Both stages are cascoded to allow for realizing a high voltage gain via resistor R_{CG} and R_{CS}. The CG stage realizes wideband input
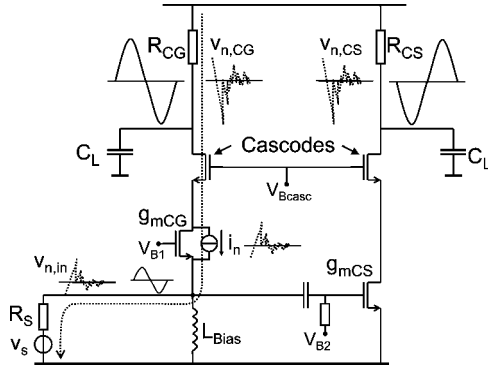
Fig. 1. Balun-LNA of [5] with cascodes added. Signal v_s is amplified and converted to a balanced RF output signal, while the noise i_n of the impedance-matching CG transistor is canceled.

Fig. 2. Practical balun-LNA design for $n = 4$ illustrating typical component dimensioning and biasing in a 65 nm CMOS technology.

impedance matching and gain, while the CS stage realizes an anti-phase output signal. The circuit can simultaneously achieve noise canceling, distortion canceling and output balancing as discussed in detail in [5]. In a CG stage only, the noise of the CG transistor would be dominant when the input impedance is matched to $R_S(g_{mCG} = 1/R_S)$. However, using a properly designed CS stage this noise (i_n in Fig. 1) can be canceled. The noise current (i_n) generates a noise voltage on the source resistor ($v_{n,in}$) and a larger voltage in anti-phase across $R_{CG}(v_{n,CG})$. The input noise voltage ($v_{n,in}$) is amplified by the CS stage to $v_{n,CS}$, which is in-phase and fully correlated with $v_{n,CG}$. For equal CG and CS stage gain, the *noise due to the CG transistor is fully canceled* at the differential output, while the *signal contributions* to the output signal *add up* to create a balanced output. This noise-canceling technique was proposed in [8], [9], while different circuit topologies were generated and compared in [10]. The parallel CS-CG topology (or balun-LNA) was found to be one of the best performing topologies (topology "e") in Figs. 4.22 and 4.23 of [10]). It cancels the noise of the CG transistor in order to obtain a noise figure (NF) close to or lower than 3 dB [3]–[6], [9], [11]–[13]. To achieve this low NF, the impedance of the CS stage needs to be scaled down n times with respect to the CG stage, where n is typically in the order of 4 (see Fig. 2).

The CG stage is biased using an external inductor (L_{bias}) to obtain low-noise operation and save valuable voltage headroom. Depending on the application this inductor can either be very large (RF-choke) for wideband operation, or smaller and well-defined to tune to a dedicated band and realize RF pre-filtering. Especially for software defined radio transceivers this is a realistic approach, as some RF pre-filtering is commonly needed to make the linearity requirements of a CMOS transceiver feasible [14]. Using an external inductor at the input of a CMOS chip allows for realizing external re-configurability and generally the quality factor of the off-chip inductors is higher than on-chip realizations.

B. Achievable Gain and Bandwidth

The voltage gain of transistors in modern CMOS processes is low. Cascoding is an effective method to increase the voltage gain. The output resistance of the transconductor (input transistor plus cascode) is increased, so that increasing R_{CG} and
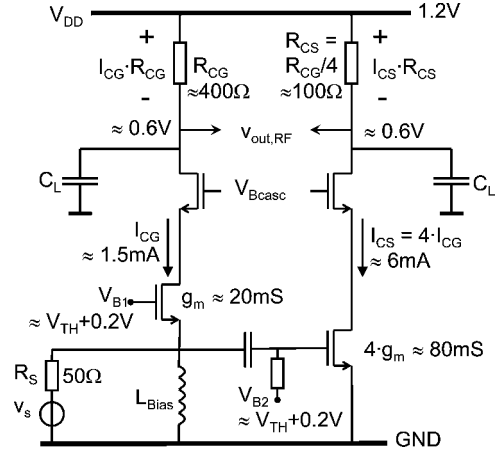
R_{CS} in Fig. 1 still improves the voltage gain. Next to this, the cascodes lower the effective input capacitance, as the Miller effect is reduced (most important for the CS transistor, as it is n-times wider than the CG transistor). This helps to improve the bandwidth over which good input impedance matching is achieved.

Let us now consider the gain and bandwidth of the balun-LNA, neglecting the effect of body effect for simplicity. In Fig. 2 a typical design in a 65 nm CMOS technology is shown. The transconductance of the CG transistor is 20 mS to realize impedance matching to a 50 Ω source. This requires about 1.5 mA of biasing current for a transistor with $W/L = 90\ \mu\text{m}/0.06\ \mu\text{m}$ at a moderate overdrive voltage of $V_{GT} \approx 0.2$ V. We design the voltage drop across the load resistor to be 0.6 V, half of the 1.2 V supply voltage. This leaves 0.6 V for the sum of V_{DS}'s of the input and cascode transistor, which is sufficient to keep each MOS transistor in saturation ($V_{DS} > V_{GT}$). With 1.5 mA bias current in the CG stage and 0.6 V headroom, the CG load resistor (R_{CG}) becomes 400 Ω. If we use the same components and biasing in the CS stage, and neglect the body effect, then DC-bias and modulus of the gain of the stages are equal. Since the CG noise is cancelled, the CS noise dominates in the LNA. To achieve acceptable noise, the impedance level in the CS stage is assumed to be scaled down by 4 times (80 mS and 100 Ω). This does not affect the DC-voltages and voltage gain. With $g_{m,CG} = 20$ mS and $R_{CG} = 400\ \Omega$, the voltage gain of the CG stage is

$$A_{v,CG} = g_{mCG} \cdot R_{CG} = 20 \cdot 10^{-3} \cdot 400 = 8. \tag{1}$$

As the gain of the CS stage is equal but with opposite sign, the total voltage gain of the CG-CS LNA from single-ended input to differential output is 2 times higher:

$$A_{v,CG-CS} = 2 \cdot A_{v,CG} = 16 \Leftrightarrow 24\ \text{dB}. \tag{2}$$

A high voltage gain can thus be obtained by using this parallel connection of a CG and a CS stage. However, the bandwidth associated with this high gain is limited due to the dominant pole at the output of the CG stage. For a 3 dB bandwidth of

10 GHz, the loading capacitance (C_L) is most critical at the CG side and should be smaller than

$$C_L < \frac{1}{2\pi \cdot R_{CG} \cdot f_{-3\text{dB}}} = \frac{1}{2\pi \cdot 400 \cdot 10 \cdot 10^9} = 40\,\text{fF}. \quad (3)$$

The load capacitance is the sum of the input capacitance of the next stage (input stage of the mixer) and the capacitance of the cascode transistor. For a cascode transistor with $W/L = 90/0.06$ (same size as the CG transistor), the capacitance of the only the cascode is already close to the maximal allowed capacitance:

$$C_{\text{Casc}} \approx C_{GDO} + C_{JDB} = 15f + 22f = 37\,\text{fF} \quad (4)$$

where the two dominant capacitances seen at the drain of the cascode are the gate-drain overlap capacitance (C_{GDO}) and the drain-bulk junction capacitance (C_{JDB}). This means that no (capacitive) load can be driven when a 3 dB bandwidth in the order of 10 GHz is required. This clearly shows that there is a bandwidth problem at the load of the CG side for high enough voltage gain. As one of the goals in this design was to avoid the use of on-chip inductors, no inductive peaking techniques [3], [6] will be used to broaden the bandwidth. The BLIXER topology we propose in the next section achieves high bandwidth without requiring on-chip inductors.

III. THE BLIXER TOPOLOGY

A. The Basic BLIXER Topology

In Fig. 3, the principle of the BLIXER topology is shown. Compared to the balun-LNA of Fig. 1, the same CG and CS transistors are used while the cascode transistors are now part of a current commutating mixer. Instead of one, both the CG and the CS side have now two cascode (or mixer) transistors, which are periodically switched on and off, with frequency f_{LO}. The current from the CG and CS transistor can always flow towards the loads (discussed in Section III-B), as at any moment in time one of its mixer (cascode) transistors is active, i.e., the LO signal has 50% duty-cycle. At the drains of the mixer the signal of interest is down converted to an intermediate frequency (IF) which is much lower than the RF frequency. In the BLIXER topology, the capacitance at the loads sets the *IF bandwidth*, instead of the *RF bandwidth* in case of the balun-LNA. As the IF bandwidth is much lower than the RF bandwidth, the capacitance at the loads can be much higher. Furthermore, the capacitive load of the next stage can be absorbed into the capacitance of the IF filter. The bandwidth problem at the load of the CG stage, described in the previous section, is thus solved without requiring inductors for bandwidth extension.

There are only three RF signal nodes in the BLIXER topology: the input node and the two drain nodes of the CG and CS transistor. This means that in the complete down-converter there are only three nodes that can limit the RF bandwidth. For impedance matching, the real part of the input impedance of the circuit equals R_S (50 Ω). When the real part of the impedances at the two drains nodes is low (indicated in Fig. 3), the bandwidth at these nodes can be high. For switch transistors equal to the cascode transistors in Fig. 2, the real parts at the drains of the CG and CS transistors are 50 Ω and 12.5 Ω, respectively, $(= 1/g_m$
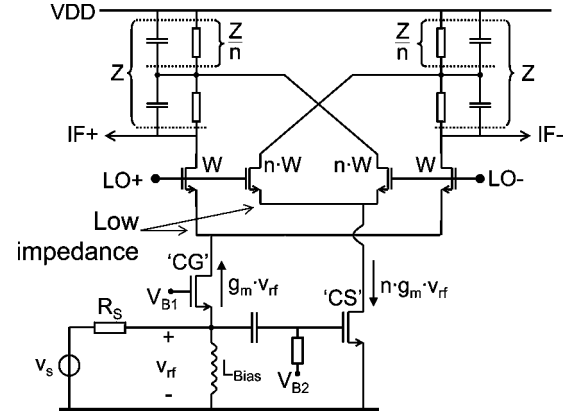

Fig. 3. Basic BLIXER topology consisting of the balun-LNA core of Fig. 1 with doubled cascode transistors driven by an LO implementing down-conversion mixing to IF.

of mixer transistors). Thus, all RF node impedances are in the order of 50 Ω or lower, allowing for high bandwidth.

The CG and CS transistors can be considered as a transconductor converting v_{rf} to currents $g_m \cdot v_{\text{rf}}$ and $n \cdot g_m \cdot v_{\text{rf}}$ (see Fig. 3). These currents are largely conveyed to the IF output via the switched cascode transistors, provided the real input impedance of these transistor is lower than the parasitic capacitance to ground. Only modeling gate-source capacitances, the RF bandwidth limitation due to the switched cascode transistors will be close to $f_T = g_{m,\text{switch}}/C_{gs,\text{switch}}$, which is typically an order of magnitude higher than for the balun-LNA with a voltage gain in the order of 20 dB.

B. Noise Canceling at IF Instead of at RF

Consider now the real part of the load impedance, which consists of four resistors instead of two in the balun-LNA. A bit more complex load is used in order to maintain the noise-canceling conditions in both LO switch positions. In Fig. 4, the active part of the circuit is shown when LO+ is high. As in Fig. 1, the CG side has Z as load, while the load in the n times scaled CS side is Z/n. The IF output voltage is sensed at the combined CG and CS load, where the lower capacitance of the current-less branch effectively works as level shifter. As the impedance of the CS side is n times lower than for the CG side, it has a low noise contribution and still the gain of the CG and the CS sides is equal. As the gain of both sides is equal, the noise of the CG transistor is canceled in the same way as in the balun-LNA of Fig. 1 Note that in the BLIXER topology the noise canceling takes place after the frequency (down) conversion i.e., at IF. The noise-canceling down-converter in [15] also has this property. However, it is much less power efficient as *cascaded* stages instead of cascoding (i.e., stacking of transistors with current re-use) was used, while also high overdrive voltages were used to push the bandwidth.

C. The I/Q-BLIXER Topology

Quadrature outputs are required in order to implement a low- or zero-IF receiver. It is possible to create quadrature outputs starting with signal currents i and $-i$ from a differential pair, by connecting two switching pairs to each current, and using a sine
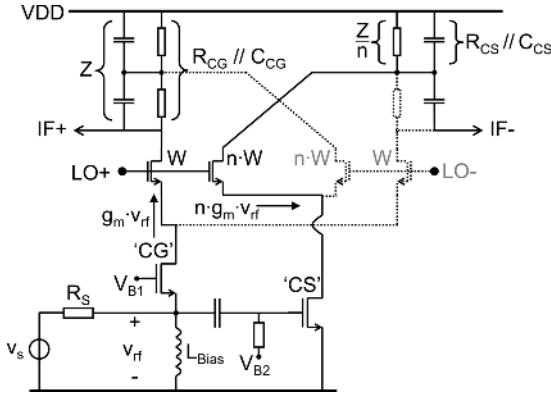
Fig. 4. Equivalent circuit of the BLIXER when LO+ side is active. As in Fig. 1, the current of the CG stage flows into its load impedance $R_{CG}(//C_{CG})$, and the CS current flows into $R_{CS}(//C_{CS})$, which impedance is n times smaller.
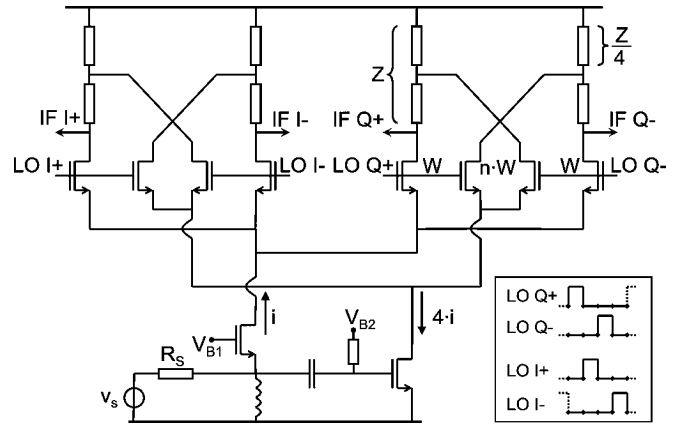

Fig. 5. I/Q-BLIXER driven by LO waveforms with 25% duty cycle, which allows for sharing currents i and $4 \cdot i$ by an I- and Q- mixer.

and cosine wave to drive the two pairs [16], [17]. In principle this is also possible with the asymmetrical balun-LNA currents i and $-4i$, provided that the switch transistors and load network are scaled as shown in Fig. 5. We will refer to this circuit as the I/Q-BLIXER. Simulations show that it is possible to use sine and cosine LO signals in I/Q-BLIXER, however this seems mainly attractive for narrowband receivers like in [16] and [17]. For narrowband receivers, the required sine and cosines can be generated via a quadrature VCO with relatively small tuning range. For multi-standard receivers or software defined radio we want much wider tuning range. Digital frequency synthesis methods exploiting Moore's law are then preferred [18]. However, using two square waves with 50% duty cycle with a relative delay of 1/4 period gives 25% overlap between LO I and LO Q pulses. Using a 25% duty-cycle, this overlap can be avoided and it is possible to "isolate" the I- and Q- current-path in time. Hence, the full g_m of the input devices is available to either the I- or Q-output of the circuit which is beneficial for the conversion gain. Furthermore, we will show in the next section that, without compromising the voltage headroom, it is possible to double the value of the IF load resistors to increase the gain.

D. Conversion Gain and Voltage Drop Load Resistors

The voltage conversion gain from single-ended input to differential output of the BLIXER topology (Fig. 3) can be calculated as

$$G_{\text{BLIXER}} = \frac{2}{\pi} \cdot (g_{mCG} \cdot R_{CG} + g_{mCS} \cdot R_{CS}) \cdot 2 \cdot \frac{1}{2}$$
$$= \frac{2}{\pi} \cdot (g_{mCG} \cdot R_{CG} + g_{mCS} \cdot R_{CS}) \quad (5)$$

where, after the first equal sign, the factor $2/\pi$ equals the fundamental Fourier component of a 50% duty-cycle (LO)-signal toggling between 0 and 1. The term between brackets is the combined voltage gain of the CG and CS side. The factor 2 is because a differential LO signal is used, and the final factor is because only the down converted half of the signal is used, as shown in (6) at the bottom of the page.

Similarly, the voltage gain of the I/Q-BLIXER (Fig. 5) with 25% duty-cycle LO equals

$$G_{\text{IQBLIXER}} = \frac{\sqrt{2}}{\pi} \cdot (g_{mCG} \cdot R_{CG} + g_{mCS} \cdot R_{CS}) \quad (7)$$

where the factor $\sqrt{2}/\pi$ equals the fundamental Fourier component of a 25% duty-cycle LO signal.

Compared to the BLIXER, the conversion gain of the I/Q-BLIXER is lower due to the lower duty-cycle, assuming the same g_m's and load resistors are used. However, in the I/Q-BLIXER larger load resistors can be used, as shown below.

The average (or DC) voltage drop across the load resistors in the BLIXER is

$$\overline{V_{\text{Load}}} = \frac{1}{2}(I_{CG} \cdot R_{CG} + I_{CS} \cdot R_{CS}). \quad (8)$$

This is because with 50% duty-cycle LO, half of the period the CG transistor bias current (I_{CG}) flows through R_{CG} and in the other half the CS bias current (I_{CS}) a current flows through R_{CS}.

In the I/Q-BLIXER, the DC-voltage drop across the load equals

$$\overline{V_{\text{Load}}} = \frac{1}{4}(I_{CG} \cdot R_{CG} + I_{CS} \cdot R_{CS}) \quad (9)$$

$$
\begin{aligned}
s(t) &= \cos(\omega_{\text{Signal}} t) \cdot \cos(\omega_{\text{LO}} t) \\
&= \frac{1}{2} \cdot \cos\left((\omega_{\text{Signal}} - \omega_{\text{LO}}) t\right) \quad \longrightarrow \text{down converted, used IF} - \text{signal} \\
&+ \frac{1}{2} \cdot \cos\left((\omega_{\text{Signal}} + \omega_{\text{LO}}) t\right) \quad \longrightarrow \text{up converted, removed by IF} - \text{filter.}
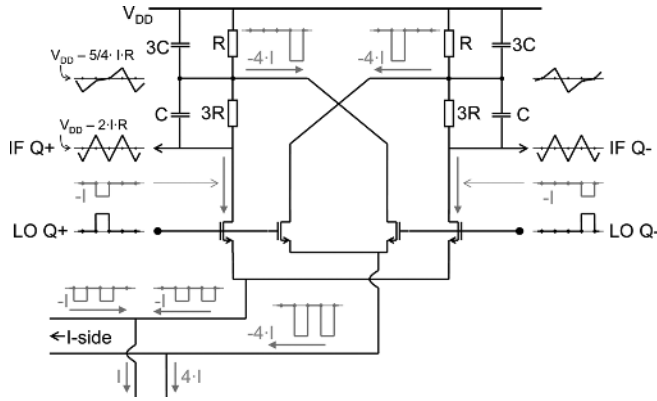\end{aligned}
\quad (6)
$$

Fig. 6.   Q-side of the I/Q-BLIXER showing the branch currents and node voltages.

as with 25% duty-cycle the CG and CS bias current flow only for 1/4 of the period through one of the loads (the waveforms are shown in Fig. 6). The capacitors in the load average these pulses of current and filter out the high-frequency components.

Comparing (8) with (9) we see that, assuming equal transconductor bias currents (I_{CG} and I_{CS}) and equal voltage drop across the load, we can double the load resistors (R_{CG} and R_{CS}) in the I/Q-BLIXER. This doubling of the load resistors ($+6$ dB) compensates the gain reduction caused by the lower duty-cycle (-3 dB) and results in 3 dB more conversion gain for the I/Q-BLIXER compared to a 50% duty cycle BLIXER.

A numerical example clarifies this further. Using exactly the same components and biasing as the balun-LNA of Fig. 2 for the BLIXER results in the same average voltage drop across the load resistors (0.6 V). Using (5) the conversion gain equals: $G_{\text{BLIXER}} = 20$ dB, which is about 4 dB lower ($2/\pi$) than the gain of the balun-LNA. In the I/Q-BLIXER we can double the load resistors, i.e., $R_{CG} = 800\ \Omega$ and $R_{CS} = 200\ \Omega$, for equal load voltage drop. This results in an I/Q-BLIXER with a gain of $G_{\text{IQBLIXER}} = 23$ dB, which is only 1 dB lower than the balun-LNA, and 3 dB higher than the BLIXER.

E. Similar Topologies in Literature

In [19], a MICROMIXER cell with single-ended input and differential output was proposed. It uses a bipolar equivalent of the CG-CS input stage. However the possibility of noise canceling was not recognized nor exploited. Two of these mixer-cells and an additional LNA would be needed for I/Q operation with acceptable NF.

A merged LNA and I/Q-mixer was published in [16]. However, this design is narrowband, uses 3 on-chip inductors and requires a differential RF input signal. In contrast, the I/Q-BLIXER topology does not require on-chip inductors, achieves wideband single-to-differential operation and I/Q-mixing in one circuit cell.

In [20], a "merged CMOS LNA and Mixer exploiting noise cancellation" is proposed, which seems related at first sight ("merged" and "noise cancellation"). However, a closer look shows this combination actually uses a folded mixer with separate bias currents for the LNA and mixer core (no current re-use). Also the used noise canceling is of another type rendering partial canceling. This circuit has no I/Q outputs,

requires a differential input (and external balun) and uses four on-chip inductors. Still, the circuit also uses down-conversion via current commutation directly on the output current of a CG input stage, and is in that sense related. We will compare its performance at the end of the paper (see Table I).

F. Attractive Properties of BLIXER Topologies

Apart from the bandwidth advantages, the BLIXER topology has some other advantageous properties with respect to linearity, balancing of the output and power consumption, as discussed below.

Similar as the noise, the distortion generated by the CG transistor is canceled [4], [5], [11] and the load resistors are linear. If the switch transistors are well switched, the mixer transistors convey the output current of the CG-CS stage to the output without much distortion (assuming $1/g_{\text{m}}$ is significantly lower than the somewhat nonlinear output impedance of the CG/CS transistors). This means that the only remaining source of nonlinearity in the BLIXER is the V-to-I conversion of the CS transistor. In a traditional cascade of voltage-gain LNA and active mixer, the mixer input transistors experience almost an order of magnitude more voltage swing that the RF input, and hence often limit the overall linearity. As the CS transistor of the BLIXER directly senses the RF input voltage *without pre-amplification*, relatively high linearity can easily be obtained.

Compared to the balun-LNA of Fig. 1, the BLIXER also improves on the quality of the balance of the output signal. This is because the output load network is completely symmetrical in the BLIXER, instead of the Z and Z/n in the balun-LNA. Moreover, *both the CG and the CS stage* contribute to *both* output signals (each half of the time). Even if the ratio of $g_{m,CG}$ and $g_{m,CS}$ is not exactly equal to the ratio of the *CS*- and *CG*-load impedances ($1:n$), still the gain balancing at the IF output is unaffected. Such a mismatch does make the noise canceling less perfect, but as shown in [8], [10] noise canceling is robust for such errors as $\pm 20\%$ mismatch still only gives 0.1 times the noise of the CG transistor (without canceling).

The power efficiency of the BLIXER is also attractive as the bias-current of the balun-LNA is re-used to realize the mixer functionality. Especially when the I/Q configuration is used, a complete I/Q receiver with high conversion gain is obtained re-using the power of balun-LNA. Of course, the LO drivers do require additional power, but this power will scale down in future technologies with Moore's law.

IV. IMPLEMENTATION AND SIMULATIONS

In the following sections we will discuss the actual chip implementation of the BLIXER in CMOS 65 nm technology and we will evaluate its performance via simulations, comparing to the balun-LNA and basic BLIXER.

A. Input Transconductor Implementation

The implementation of the input transconductor is shown in Fig. 7. As discussed in Section III-F the CS stage determines the linearity of the circuit. In order to obtain high (third-order) linearity the CS transistor should be biased with a high V_{GT}. However, at a high V_{GT}, the g_m/I_D of a transistor is low, which
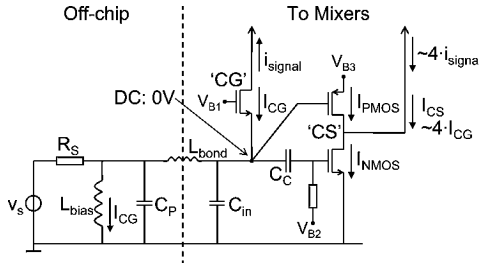
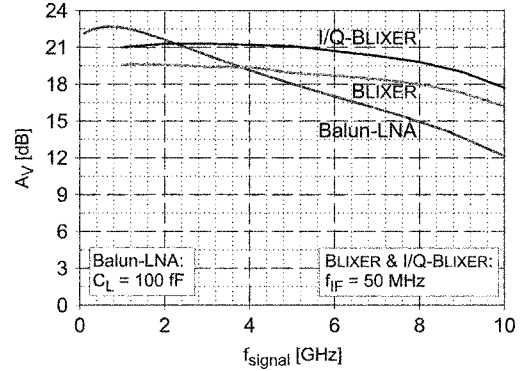Fig. 7. Implementation of the input stage. The CS transistor is split is a PMOS and an NMOS transistor.

Fig. 8. Gain of the balun-LNA, basic BLIXER (50% LO duty-cycle) and I/Q-BLIXER (25% LO duty-cycle). Note that the BLIXERs have much higher bandwidth (9.5 GHz).

means that a large bias current is required to reach a certain g_m. This reduces the voltage headroom as this bias current has to flow through the loads. Therefore, the CS stage is implemented using a PMOS and a NMOS transistor. Both the NMOS and PMOS can be biased at a high V_{GT} for high third-order linearity, whereas also the second-order distortion can be low in this inverter-type of circuit. The effective g_m of this inverter based CS stage is designed to be about 4 times higher than the effective g_m of the CG transistor. Also the DC-output current the CS stage inverter ($I_{CS} = I_{NMOS} - I_{PMOS}$) is designed to be approximately 4 times higher than the bias current of the CG transistor. Besides the high linearity, another advantage of the inverter-type CS is that the PMOS transistor can be DC-coupled to the input, which reduces the AC-coupling related signal-loss to the input of the CS stage.

The CG transistor is biased using an inductor which puts the source of the CG transistor at DC-ground, as indicated in Fig. 7. Because the biasing of the CG transistor does not require any DC-voltage drop, the voltage headroom of the CG and CS side is equal. A large bias inductor ($L_{bias} \sim 40$ nH) can be used as it is placed off-chip. This large inductor allows for good matching in the lower frequency range. In the higher frequency range, the parasitic capacitance of the inductor (C_{par}) dominates. Together with the total bondwire inductance and input capacitance (L_{bond} and C_{in}) a broadband-matching π-network is formed, which results in impedance matching up to high frequencies.

B. Switches and Load Implementation

The width of the switches switching the CG current was chosen at 40% of the width of the CG transistor. The reason for choosing a small(er) width is to reduce the input capacitance of the switches. The area of a transistor determines its 1/f-noise. In order to lower the 1/f-noise contribution of the switch transistors, their area was increased by setting the length to 100 nm, instead of using minimum length (65 nm) devices. As overlap and junction capacitances dominate the capacitance of transistors with small length, increasing the length increases the input capacitance of the switches only slightly. The CS switches are 4 times wider than the CG switches.

The impedance ratio of the CG and CS part of the load was designed equal to the ratio of effective CS and CG transconductance, which is nominally slightly lower than 4. The bandwidth of both parts of the loads was designed in the order of 300 MHz, enough to handle UWB signals in a zero-IF architecture.

C. Conversion Gain and Noise Figure Simulations

In this section we will evaluate the gain and noise figure of the BLIXER and the I/Q-BLIXER and compare it to the standalone balun-LNA. The aim of this comparison is to show that the BLIXERs can have more bandwidth, at practical values for the gain and noise figure. In order to make a fair comparison, all three circuits use the input stage described in Section IV-A, and the dimensions of the (switched or biased) cascode transistors are equal. Choosing this, the bias current of the three circuits cores is equal. However, the BLIXER and I/Q-BLIXER have more functionality than the balun-LNA, as these circuits also perform (I/Q) down-conversion.

As discussed in Section III-D, the load impedance of the BLIXER and the balun-LNA needs to be half the load impedance of the I/Q-BLIXER, in order to keep the average voltage drop across the loads equal in all three cases. The loads in the balun-LNA and BLIXER are halved by placing two I/Q-BLIXER loads in parallel. The switches of the BLIXER and I/Q- BLIXER are driven with ideal 50% and 25% duty-cycle LO signals respectively (rise and fall time 1% of the LO period).

Fig. 8 shows the voltage conversion gain of the BLIXERs as a function of the input signal frequency for an IF of 50 MHz. Also the voltage gain versus signal frequency of the balun-LNA, loaded with 100 fF on both outputs, is shown. Clearly, the bandwidth of the BLIXERs is much higher ($\sim$ 9.5 GHz) than the bandwidth of the balun-LNA ($\sim$ 3.5 GHz). As expected, the (low frequency) conversion gain of the I/Q-BLIXER is about 1dB lower than the gain of the balun-LNA.

Fig. 9 shows the Noise Figures of the three topologies. The *single* side band (SSB) noise figure of the BLIXER is $\sim$ 4 dB higher than the NF of the balun-LNA. This can be expected based on the conversion-loss of the mixing action (2π or -4 dB). In contrast to the BLIXER, the I/Q-BLIXER has I- and Q-outputs which can be combined to reject the noise of the image band. Therefore, the relevant measure of NF for the I/Q-BLIXER is the double side band (DSB) NF. Fig. 9 shows that compared to the standalone balun-LNA, the NF of the I/Q-BLIXER increases with only 1–2 dB.

D. Effects of Non-Ideal LO Signals

For higher LO frequencies, it becomes increasingly challenging to generate a 25% duty-cycle LO signal with sufficiently
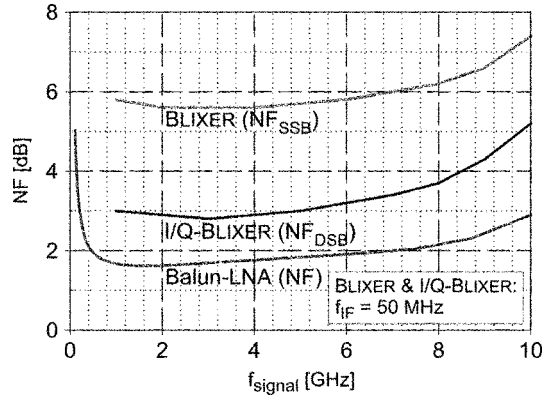
Fig. 9. Comparison of the noise figure of the balun-LNA, basic BLIXER and I/Q- BLIXER. NF_{DSB} is used for the I/Q-BLIXER as it has quadrature outputs.
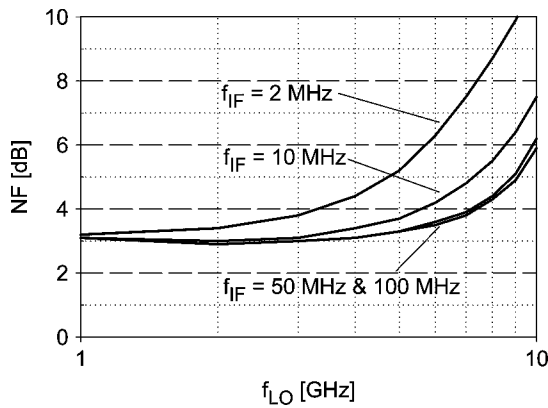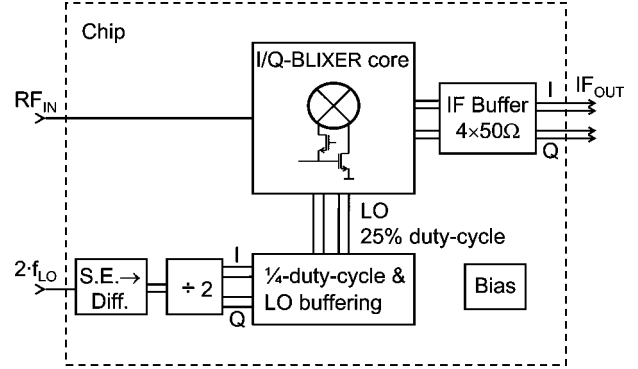

Fig. 11. Overview of the test chip. The LO is derived from an external clock via a single-to-different converter and divide-by-2 to generate quadrature phases.
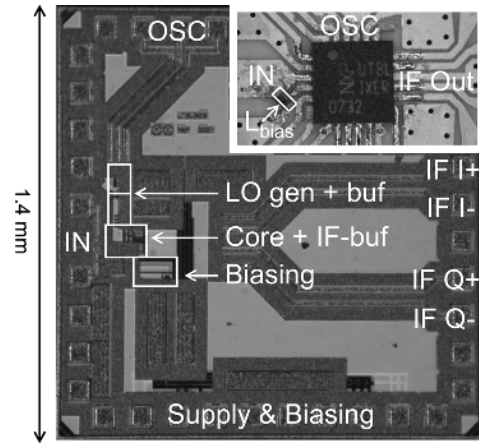

Fig. 10. Effect of LO pulse with finite rise and fall time in the I/Q-BLIXER on the NF versus the LO frequency for different IF frequencies.

Fig. 12. Chip micrograph and PCB detail showing packaged sample.

low rise and fall times. Simulations on the I/Q-BLIXER are performed to investigate the effects of finite rise and fall times. An ideal voltage source generating a 25% duty-cycle LO signal with 10% rise and fall time is supplied to a cascade of two inverters, for each of the four LO phases. The inverters used for this simulation are equal to the inverters used in the final stage of the LO driver in the complete I/Q-BLIXER realization. The size of second inverter is twice the size of the first inverter, and is designed to drive the LO switches. The inverters limit the rise and fall time to about 25–30 ps, which causes narrower pulses and lowers pulse-amplitude for higher LO frequencies.

Fig. 10 shows that for higher LO frequencies, mainly the NF at low IF frequencies (2 MHz) is affected. The increase in NF at low IF frequencies is due to an increased sensitivity to 1/f-noise of the LO switches and the LO driver (inverter) transistors. The reduction of conversion gain compared to the case with ideal LO drive is smaller than 1 dB (not shown as this is only a minor effect).

V. IC IMPLEMENTATION AND MEASUREMENTS

Fig. 11 shows an overview of the I/Q-BLIXER test chip. The RF input is single-ended while the IF I- and Q-outputs are differential. The single-ended external oscillator signal is converted into a differential signal on-chip and subsequently divided by 2 to generate in-phase (I) and quadrature (Q) LO signals. The output of the divide-by-2 is amplified to rail-to-rail

swing to obtain a 50% duty-cycle LO signal. The required 25% duty-cycle is generated using an AND operation on the I- and Q-signals. The I/Q-BLIXER core is implemented as described in Sections IV-A and Sections IV-B. The differential IF outputs of the I/Q-BLIXER are buffered to 50 Ω for measurement purposes using four source-followers.

The circuit was fabricated in a baseline 65 nm LP CMOS technology and a standard 1.2 V supply was used. The die photo and a detail of the PCB are shown in Fig. 12. The I/Q-BLIXER core measures less than 0.01 mm². The measurements were performed on packaged, PCB-mounted samples.

The measured voltage conversion gain is 19 dB with and the IF bandwidth is 400 MHz, as shown in Fig. 13. The DSB NF of the I/Q-BLIXER at a 3 GHz LO frequency is around 4.5 dB and flat over the IF bandwidth. The wideband RF performance is shown in Fig. 14. The gain remains flat within 1dB up to 7 GHz. From 1 to 6 GHz, the NF is below 5 dB, using a fixed IF of 50 MHz. Note that this NF includes the PCB losses. Above 7 GHz, the circuit generating the 25% duty-cycle LO signals fails and the gain and NF could not be determined. The S_{11} is below −10 dB up to 7 GHz.

The wideband linearity was measured using a two tone test. To assess IIP2 and IIP3 without filtering effects, the input tones and the intermodulation products should fall within the flat part of the conversion gain versus frequency curve (Fig. 14). In a wideband system a high spacing between the two test tones can
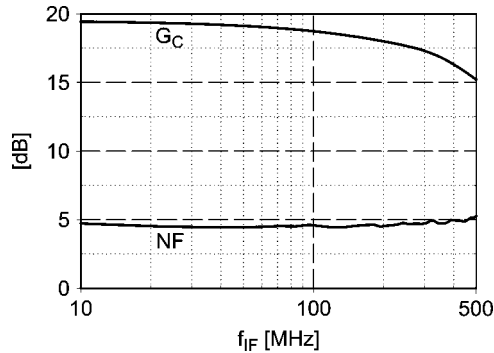
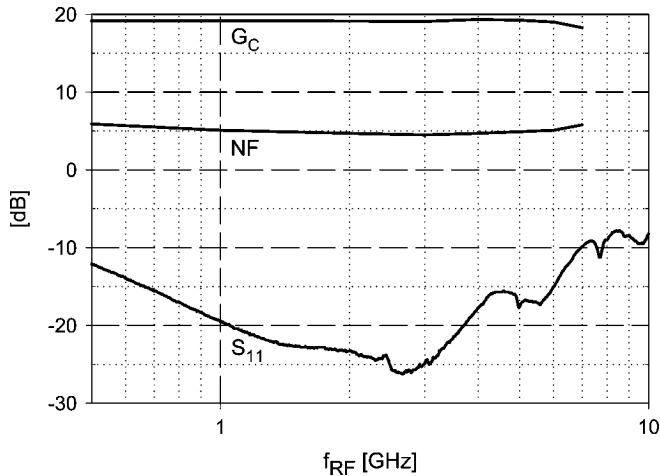Fig. 13. Conversion gain (G_C) and NF for $f_{LO} = 3$ GHz.

Fig. 14. Conversion Gain (G_C), NF and S_{11} versus RF input-frequency ($f_{IF} = 50$ MHz).

Fig. 15. I/Q-BLIXER power consumption breakdown for 500 MHz and 7 GHz.

be used. Two tones at 5.2 GHz and 5.7 GHz, which represents two IEEE 802.11a interferers, gives a 3rd order intermodulation product at 4.7 GHz . Using an LO frequency of 4.6 GHz the measured IIP3 = −3 dBm. The IIP2 equals +20 dBm, using 2.4 GHz (802.11 b/g) and 5.7 GHz (802.11 a) input tones and an LO of 3.2 GHz. The intermodulation for tones that leak through the mixer was determined using a 5.7 GHz and a 5.8 GHz signal (two 802.11a interferers). The intermodulation product at 100 MHz showed an IIP2 > +40 dBm, regardless of the LO frequency. The LO leakage to the RF input is below −60 dBm for LO frequencies up to 4 GHz and below −5 dBm up to 7 GHz.

Fig. 15 shows a breakdown of the power consumption of the different parts of the implemented circuit. The I/Q-BLIXER core consumes 16 mW and the biasing and IF buffering combined consumes 13 mW. Note that the IF buffers are added for measurements purposes and can often be omitted. At an LO frequency of 500 MHz, the 25% duty-cycle generation and LO buffering consume only 4 mW. At an LO frequency of 7 GHz this part consumes 28 mW, which is almost half of the total power consumption. The LO buffering is based on inverters, which explains the increase in (dynamic) power consumption at higher LO frequencies.

In Table I the measured performance is summarized and compared to other state-of-the-art wideband down-converters. The I/Q-BLIXER achieves the widest signal bandwidth. Note that we
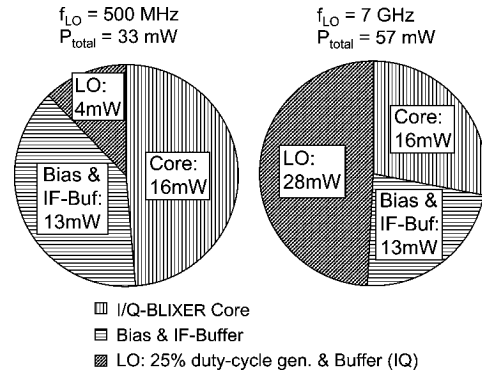
specify the −1 dB bandwidth, where others often specify the −3 dB bandwidth. The obtained linearity is the highest among the reference designs. The main reason for the high linearity is that the (RF) linearity is determined by only one transistor (combination), the CS inverter.

The noise figure is comparable to the other designs; furthermore, the NF is almost flat across the entire band. Note that this NF includes the PCB losses and that no external balun is needed.

Due to the absence of on-chip inductors, the area is very small. The combined area of the I/QBLIXER core and the I/Q-LO buffers is more than 4.5 times smaller than the smallest reference design.

For low LO frequencies, the power consumption of the LO buffering is much lower than the other designs, and for high LO frequencies, it is in the same order. The design of [20] has a lower core (LNA plus mixer) power consumption. However, in contrast to our design, this design has no quadrature outputs. Compared to the designs with quadrature outputs [1]–[3], the power consumption of our design is about 2 times lower.

VI. CONCLUSION

This paper proposes the BLIXER topology, which stacks a current-commutating mixer on top of a noise-canceling balun-LNA. The proposed topology has several attractive properties. It achieves a high and flat gain over a wide bandwidth without inductors for bandwidth extension. This is because the BLIXER directly converts the currents of the balun-LNA core to IF via current-commutating mixers, of which the (real part of) the input impedance is low. Creating voltage gain is shifted from RF to baseband where capacitive loading is not a problem. By using an I/Q mixer with 25% duty-cycle LO waveform, the output IF currents have also have a reduced duty-cycle, resulting in smaller DC-voltage drops after IF filtering. This allows for a 2 times increase of the impedance level of the IF load, rendering 2 times more voltage gain for the same supply headroom. The I/Q-BLIXER theoretically has only 1 dB less gain than a balun-LNA biased at the same current. Also, its double sided noise figure is only 1–2 dB higher than for the balun-LNA alone. The I/Q-BLIXER topology implements balun, LNA, and I/Q down-conversion functionality, all in one circuit core. A 65 nm implementation achieves >18 dB conversion gain, a flat NF < 5.5 dB from 500 MHz to 7 GHz, IIP2 = +20 dBm and IIP3 = −3 dBm. The core circuit consumes 16 mW which

TABLE I
COMPARISON OF STATE-OF-THE-ART WIDEBAND DOWN-CONVERTERS

Parameter		This Work	Lee ISSCC'07 [1]	Craninckx ISSCC'07 [2]	Bagheri JSSC'06 [3]	Amer JSSC'07 [20]
RX Frequency [GHz]		**0.5 – 7** [1)]	2 – 8	1.8 & 5 – 6	0.8 – 6	0.1 – 3.85
Gain [dB]		18 *excl.* IF-Amp	23 incl. IF-Amp	10 – 90 incl. IF-Amp	3 – 36 incl. IF-Amp	20 incl. IF-Amp
IIP3 [dB]		**-3**	-7	-9	-3.5	-3.2 [2)]
IIP2 @ RF [dB]		**+20**	+18	?	?	?
NF [dB]		4.5 – 5.5	4.5	4 – 8	5 – 5.5	8.4 – 11.5 (SSB)
S_{11} [dB]		< -10	< -8	< -9	< -10	< -10
Area [3)] [mm^2]	LNA + IQ-Mixers	**<0.01**	0.09	0.6	0.5	0.88 (only I-path)
	LO Buffers (I & Q)	**<0.01**		0.3	?	?
Power [mW]	LNA + IQ-Mixers	**16**	38	34 WLAN setting	29 (I & Q?)	9.8 (only I-path)
	LO Buffers (I & Q)	4 – 28	24	17 WLAN setting	?	?
CMOS Technology		65nm	65nm	0.13μm	90nm	90nm
VDD		1.2V	1.2V	1.2V	2.5V	1.2V

[1)] This is -1dB bandwidth; others use -3dB bandwidth

[2)] Estimated using $P_{IIP3} = P_{1dBCP} + 9.6$ dB [21]

[3)] Estimated from chip micrographs

is about 2 times lower than comparable wideband down-converters with I/Q-outputs. The area of the I/Q-BLIXER core occupies less than 0.01 mm^2 in 65 nm CMOS, which makes it the smallest wideband down-converter design published.

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