

## The bPOL12V DCDC converter for HL-LHC trackers: towards production readiness

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We present the electrical and radiation characterisation of the most recent prototype of the bPOL12V DCDC converter, a stacked assembly of two ASICs inside a QFN32 package. The use of a reference voltage generator chip in 130nm CMOS on top of the ASIC integrating the control system and power train enables improved radiation tolerance and the trimming of the output voltage during the production phase. Prototype samples have been exposed to X-rays, proton and neutron irradiations, as well as subject to long-term electrical stress to evaluate their reliability in the application. The results confirm that only a few minor modifications are required to achieve production readiness.

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## 1. Introduction

FEAST2 is a point-of-load (POL) DC-DC converter ASIC developed at CERN to enable a more efficient power distribution in upgraded LHC experiments, and has so far been largely adopted for this purpose [1]. Although it has been designed for application in the radiation and magnetic fields of the LHC experiments, its tolerance to displacement damage effects does not meet the requirements of HL-LHC tracker detectors. During neutron irradiation tests, samples fail after an integrated flux of about  $6 \cdot 10^{14}$  1MeV-equivalent n/cm<sup>2</sup>. Failure is due to excessive degradation in the electrical performance of the p-channel LDMOS (Lateral Diffusion MOS) transistors that, in the 0.35  $\mu$ m technology used for the ASIC manufacturing, are rated for a maximum  $V_{ds}$  of 80 V.

To overcome this limitation, the FEAST2 design has been migrated to a very similar 0.35  $\mu$ m technology that uses the same transistors for the low-voltage (3.3 V) part of the circuit but where the high-voltage module integrates LDMOS transistors rated to 25 V only. These lower-voltage transistors have a much better tolerance to displacement damage, as confirmed by measurements on dedicated test structures. The ASIC that resulted from this design migration is called bPOL12V, and 4 prototypes of this circuit have been produced and tested in the last years. This new DC-DC POL is the baseline converter for power distribution in the ATLAS and CMS HL-LHC outer trackers, where the radiation environment is estimated to about 50–60 Mrad for Total Ionizing Dose and  $1 \cdot 10^{15}$  n/cm<sup>2</sup> (expressed as 1MeV-equivalent) for displacement damage.

## 2. Overview of the bPOL12V ASIC

The design of bPOL12V is almost identical to the one used for its forebear FEAST2, although a large revision of the layout of the circuit was required by the considerable difference in the well implants in the two technologies.

bPOL12V uses a buck topology, which is the simplest architecture for step-down DC-DC converters. This choice is motivated by the simplicity as well as by the minimum number of passive components required for the integration of the ASIC in a full power module [2]. The maximum nominal input voltage is 12 V, but this is also the maximum drain-source DC voltage applicable to the NMOS transistors used for the power train in the chosen technology. It is industrial practice to de-rate the input voltage well below the maximum  $V_{ds}$ , but in our case the required radiation tolerance for displacement damage forbids the use of transistors rated at larger voltage for the power train. Experience has in fact shown how displacement damage tolerance decreases with the  $V_{ds}$  rating of the LDMOS [3].

The ASIC switches at a frequency that can be selected via an external resistor in the range of 1–2.5 MHz, enabling operation with air-core inductors of 220–500 nH compatible with the low volume and mass requirements of the trackers. The output voltage can be selected via an off-chip resistive bridge, and the maximum nominal output current is 4 A – but a lower limit is imposed at large output voltages by the thermal resistance of the assembly. Production samples will be mounted in QFN32 plastic packages identical to those already employed for the FEAST2 POL.

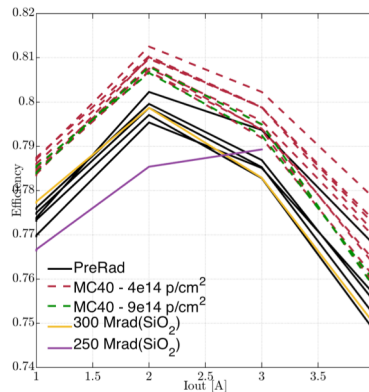
Protection features include Over-Current (OCP) and Over-Temperature (OTP) to avoid operation in conditions that might affect reliability. The thresholds for these protections are particularly difficult to set because they vary with radiation. Both the LDMOS and the core

transistors in the chosen CMOS 0.35  $\mu\text{m}$  technology experience in fact relatively large shifts in their electrical characteristics. The same applies also to the Under-Voltage Lock-Out (UVLO) thresholds, values of the input voltage under which the converter is forbidden to turn on: however in this case it is easier to take a larger margin because these thresholds only determine the minimum operational  $V_{\text{in}}$  for the converter. This limit has been set to 6 V.

The latest prototype of the bPOL12V ASIC, named “V4”, introduces for the first time a feature intended to largely improve the stability of the output voltage with radiation.  $V_{\text{out}}$  closely follows the reference voltage  $V_{\text{ref}}$ , which in all previous versions of the design was produced on-chip. Because of the drift in electrical parameters of the 0.35  $\mu\text{m}$  transistors, the reference voltage value considerably varied with irradiation and annealing in a way strongly influenced by the dose rate and temperature. This feature could not be improved by design. We decided hence to use a reference voltage generator circuit already developed in a 130 nm CMOS technology and qualified for radiation effects. This design was manufactured in the form of a small chip of about  $1.2 \times 1 \text{ mm}^2$  that can be stacked on top of the bPOL12V ASIC within the same QFN32 package. An additional advantage of this approach resides in the availability of e-fuses in the 130 nm process: using these devices it is possible to envisage a fine tuning of the  $V_{\text{ref}}$  of all production chips (trimming) to reduce the output voltage variation in production samples.

### 3. Measurement results

The V4 prototype has been fully characterized electrically, and then exposed to radiation using X-rays, neutrons and proton sources exceeding the radiation levels foreseen in the outer trackers of CMS and ATLAS. All electrical performances are compatible with the specifications, and the radiation tolerance matches the requirements as well. As an example, Figure 1 shows the efficiency of the converter before and after irradiations with X-rays and protons. Measurements after proton exposures were taken after a few weeks of annealing at room T. In Figure 2 the line and load regulation performance of the same samples is shown: only the line regulation is slightly affected by exposure (20 mV variation over the 6 V range of  $V_{\text{in}}$ ). For what concerns the protection features, only the OCP threshold significantly decreases in samples exposed to TID. Some samples irradiated up to 200 Mrad or more are forbidden by the OCP to supply currents in excess of 3.5–4 A, but a very relevant annealing is observed after irradiation. In case of need, a dedicated pad of the ASIC can be used to shift the OCP threshold up and bring the threshold above 4 A also in these samples.



**Figure 1.** Efficiency of bPOL12V converters before and after different radiation exposures.

$$V_{\text{in}}=10\text{V}, V_{\text{out}}=2.5\text{V}, L=460\text{nH}, f_{\text{sw}}=1.8\text{MHz}, T=25^\circ\text{C}.$$

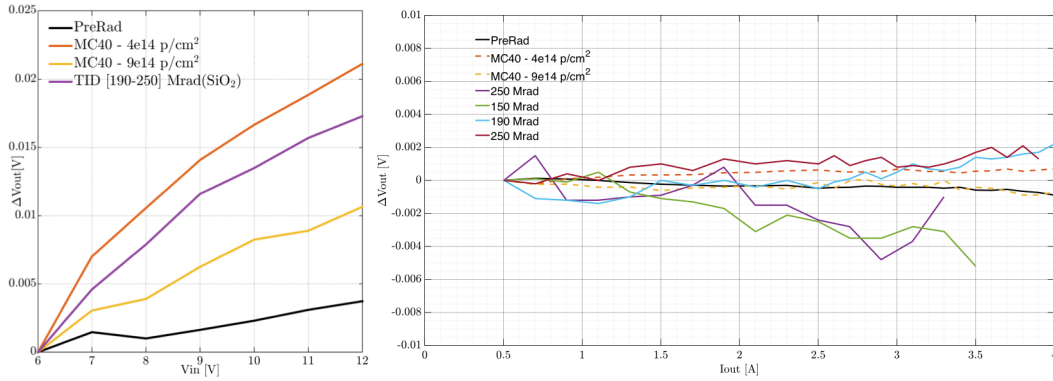


Figure 2. Line (left) and load (right) regulation of bPOL12V samples before and after irradiation.

### 3.1 Reliability evaluation

A large effort has been dedicated to the evaluation of possible threats to the long-term reliability of the converter, since it will represent a single point of failure for the tracker front-end modules. The desired input voltage specification of the converter of 12 V, is coincident with the maximum DC  $V_{ds}$  rating of the n-channel LDMOS used in the power train. During the different phases of the regular switching cycles, these transistors are thus possibly exposed to short over-voltage transients originated by large current discontinuities on the parasitic inductance of the paths where input and output currents flow. Every time the power transistors are turned on/off, the current path abruptly changes and, although this transition has been slowed down by design, the derivative of the current is so large that an instantaneous voltage variation occurs. The peak value is strongly influenced by parameters related to the integration of the ASIC in the final DCDC converter: the PCB layout and the choice of the input capacitors influence the parasitic inductance, while the value of the power inductor and switching frequency directly determine the peak current to be switched.

The testing approach, inspired by industry standards, was to keep a relatively large number of samples under voltage stress in extreme operational conditions for a long time (minimum 5 weeks, but months in some cases). The output voltage provided by the converters during the stress is monitored regularly every 10 minutes, while the device is providing power to a resistive load. This procedure has been executed on samples from the last two generations of prototypes of bPOL12V, V3 and V4. The board layout was in all cases identical, and very similar to the one used for the FEASTMP modules currently in production for LHC upgrades and built around the FEAST2 ASIC. Two values of the power inductor have been used: 460 and 220 nH from a commercial series of air-core solenoids. The switching frequency was the nominal 1.8 MHz for the 460 nH inductor, but was increased to 2.5 MHz for the 220 nH. So far about 200 samples have been stressed at input voltage ranging between 10 and 14 V while the chip temperature was between 60 and more than 100°C (strongly influenced by the load current during the stress and by the number of converters being stressed in the same confined space, since the system is air cooled). Systematic failures on a significant number of samples occur at  $V_{in}$  of 13V or larger, but a few debatable failures have been observed at 12V. In these few cases it was impossible to determine whether the failure was provoked by the stress or by a consequent manipulation of the samples. In conclusion, with the data available so far it appears that the input voltage is a

fundamental parameter in determining the reliability of bPOL12V, therefore we strongly recommend in the application the use of the minimum  $V_{in}$  compatible with the requirements of the power distribution system. At the same time, extreme care must be exercised in the layout of the converter module to minimize the parasitic inductances, while the power inductor should better be sized above 400 nH – or the switching frequency has to be increased to reduce the peak-switching current.

### 3.2 Displacement damage effects

bPOL12V samples have been exposed to neutron and proton beams to evaluate the impact of displacement damage effects. These tests have been done without bias, typically at room temperature, and samples could only be measured several weeks after the irradiation. Neutron irradiation took place at the Triga reactor of JSI in Ljubljana (Si), while the proton beams of the IRRAD facility at CERN (24 GeV/c) and of the MC40 cyclotron at the University of Birmingham (27 MeV) were used. Quite interestingly, even after normalization of the integrated fluxes using the NIEL equivalence, results induced by neutrons and protons differed: protons systematically induced more damage. This observation triggered additional measurements that are currently being performed; results will be detailed in a separate paper. Within the scope of this article it is sufficient to report that all consequences on the functionality of the converters induced by either protons or neutrons on the V3 and V4 prototypes have been understood and addressed, demonstrating that the next V5 version will be capable of surviving without significant performance degradation up to the integrated fluxes of the HL-LHC trackers – and with a safety margin larger than 2.

### 4. Conclusion

The latest prototype of the bPOL12V DCDC converter (V4) has been extensively tested to verify that its electrical and radiation tolerance performances meet the specifications for use in the ATLAS and CMS outer trackers. Although a few modifications are required to make the design production-ready, these are easy to implement and well understood. The next iteration of the design (V5) should thus be ready for mass production. Based on the results of long-term stresses, it is strongly recommended to avoid using the converters at the maximum input voltage of 12 V. During the radiation qualification of bPOL12V we observed a large difference in the degradation induced by neutrons and protons at different sources. Although the converter now passes the qualification for both types of particles, this difference needs to be studied in more detail because it might suggest the need for a re-definition of the radiation specifications in tracker systems.

### References

- [1] F. Faccio *et al.*, “FEAST2: a radiation and magnetic field tolerant Point-of-Load buck DC/DC converter”, 2014 IEEE Radiation Effects Data Workshop at the NSREC conference, Paris, July 2014.
- [2] F. Faccio, S. Michelis, *Custom DC-DC converters for distributing power in SLHC trackers*, in 2008 proceedings of TWEPP, Naxos, Greece.
- [3] F. Faccio *et al.*, “TID and Displacement Damage Effects in Vertical and Lateral Power MOSFETs for Integrated DC-DC Converters”, IEEE Trans. Nucl. Science, Vol.57, No.4, August 2010, pp.1790-1797.