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The Design of a Lumped Element Impedance-Matching Network with Reduced Parasitic Effects Obtained from Numerical Modeling

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Abstract— **This paper presents an impedance-matching network design with numerical modeling of the parasitic effects. A modeling tool CEMPIE (a Circuit Extraction approach based on a Mixed Potential Integral Equation formulation) is used to model the board-level parasitics of surface mount technology (SMT) resistors for impedance-matching networks. A 3-layer design of impedance-matching network with 0402 SMT resistors is implemented according to the modeling results. And its performance is demonstrated.**

Keywords-CEMPIE; PEEC; impedance-matching network; parasitics;

I. INTRODUCTION

On-board impedance-matching (pad-matching) networks can lose broadband frequency band behavior due to parasitic elements associated with surface mount technology (SMT) resistors, signal traces, mounting pads, and so on. Full-wave modeling of printed circuit board (PCB) layouts can provide insight in understanding the effects of these parasitics and aid the layout and the routing in achieving improved performance. In this paper, 75 – 50 Ohm impedance-matching networks designed with 0402 or 0201 package size SMT resistors were simulated using a full-wave modeling tool CEMPIE (a Circuit Extraction approach based on a Mixed Potential Integral Equation formulation) [1]. Through the analysis of the parasitics on the PCB, the impedance-matching network using 0201 parts provided better broadband characteristics than the networks that used 0402 parts. Using the insight from the study of the parasitics associated with 0201 SMT resistors, an improved design of the impedance-matching network with 0402 SMT resistors was achieved, which provided a broadband performance that is similar to that of the matching network with 0201 SMT resistors.

II. CEMPIE METHOD

CEMPIE is a circuit extraction and full-wave simulation tool [1-5], based on the mixed-potential integral equation (MPIE) in conjunction with a quasi-static approximation, which can be seen as an extension of the PEEC (Partial Element Equivalent Circuit) [6] method to general multilayer dielectric media. Through extensive applications [1-5], the tool has proved to be numerically robust.

Assuming the ground planes and dielectric layers to be infinite and enforcing the boundary conditions on the perfect electric surfaces S of the PCB, as shown in Fig. 1, the following Mixed Potential Electric Field Integral equation holds [3]:

$$\hat{n}\times\left[j\omega \int_S \overline{\overline{G}}^A(\vec{r},\vec{r}')\cdot \vec{J}(\vec{r})dS' + \nabla\phi(\vec{r}) \right]_{\vec{r}\in S} = 0, \qquad (1)$$

where $\overline{\overline{G}}^A$ is the dyadic Green's function for the magnetic vector potential in a stratified medium, which traditionally takes the form [7]

$$\overline{\overline{G}}^A = (\hat{x}\hat{x}+\hat{y}\hat{y})G^A_{xx} + G^A_{zx}\hat{z}\hat{x} + G^A_{zy}\hat{z}\hat{y} + G^A_{zz}\hat{z}\hat{z}, \qquad (2)$$

and ϕ is the electric scalar potential.

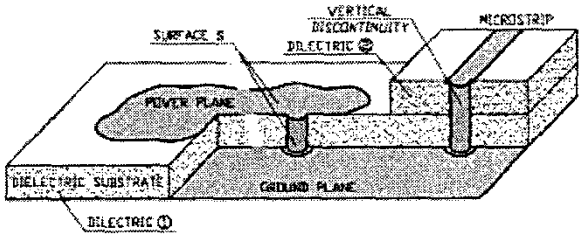

Figure 1. PCB configuration.

After representing the horizontal planes with triangular elements while the vertical surfaces of discontinuities with rectangular patches, initially the current density is approximated with a superposition of continuous normal/linear tangent (CN/LT) "rooftop" basis functions $B_n(u,v)$ [8], usually referred to a Rao-Wilton-Glisson (RWG) functions, then the Galerkin {It's controversial whether it shall be called Galerkin's approach because of the mixed basis

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functions.} weighted-residual method is applied [9], resulting in the matrix equation

$$j\omega[\mathbf{L}][\mathbf{i}]-[\Lambda][\varphi]=[\mathbf{0}], \tag{3}$$

where [i] and [φ] are the branch current and the node scalar-potential vector, respectively, [L] is the asymmetric inductance matrix, and [Λ] is the connectivity matrix between branches (edges) and nodes (cells). Relating the induced currents to the charges, which are approximated as piecewise constant over each patch, through the continuity equation, a second matrix equation is readily obtained as

$$-j\omega[\mathbf{C}]=[\Lambda]^{T}[\mathbf{i}]+[\mathbf{I}^{imp}], \tag{4}$$

where $[\mathbf{I}^{imp}]$ is the vector of the excitations which are treated as impressed currents sources and [C] is the asymmetric capacitance matrix obtained from the electric potential Green's functions G^{φ}. Combining (3) and (4) it is established the final system matrix [4]

$$\begin{bmatrix} j\omega\mathbf{C} & \Lambda \\ -\Lambda & j\omega\mathbf{L} \end{bmatrix}\begin{bmatrix} \phi \\ \mathbf{i} \end{bmatrix}=\begin{bmatrix} -\mathbf{I}^{imp} \\ \mathbf{0} \end{bmatrix}, \tag{5}$$

which describes the overall distributed electromagnetic behavior of the structure through branch currents and nodal voltages of a passive lumped network. The last step of the procedure consists in obtaining the equivalent representation, based on only node potentials,

$$[\mathbf{Y}]\,[\varphi]=-[\mathbf{I}^{imp}], \tag{6}$$

where $[\mathbf{Y}]=[\Lambda]^{T}[j\omega\mathbf{L}]^{-1}[\Lambda]+j\omega[\mathbf{C}]$ is the symmetric admittance matrix, computed from (5) by back-substituting for the unknown current vector. If originally [3,4] a {R,L,C} equivalent circuit was extracted from the [Y] matrix and exported directly into the commercial SPICE to simulate the PCB structure up to several gigahertz, subsequently [1,2,5] the admittance matrix has been transferred to an iterative equation solver after that external lumped circuit elements as well as sources had been inserted into it [5]. This method provides a more efficient computation of the few variables of interest, i.e. the scattering parameters and the input impedance.

III. Design of an Impedance-Matching Network

An impedance-matching network with two SMT resistors was used for matching 50 Ohm microstrip traces and 75 Ohm microstrip traces. The geometries with 0201 SMT resistors and 0402 SMT resistors are shown in Fig. 2(a) and 2(b), respectively. The substrate of the board is FR4, which has a relative permittivity of 4.0 and loss tangent of 0.02. The thickness of the board is 4.5 mils. The reflection loss (S_{11}) from both 50 Ohm and 75 Ohm ends of the impedance matching network, and the insertion loss (S_{21}), were simulated using CEMPIE. The results are plotted in Fig. 3 and Fig. 4. Due to the larger board-level parasitics, the reflection loss of the 0402 matching network is approximately 10 dB worse than that of the 0201 matching network in the frequency range from 500 MHz to 5 GHz. The insertion loss of the 0402 matching network is slightly larger as well. By studying the layouts of

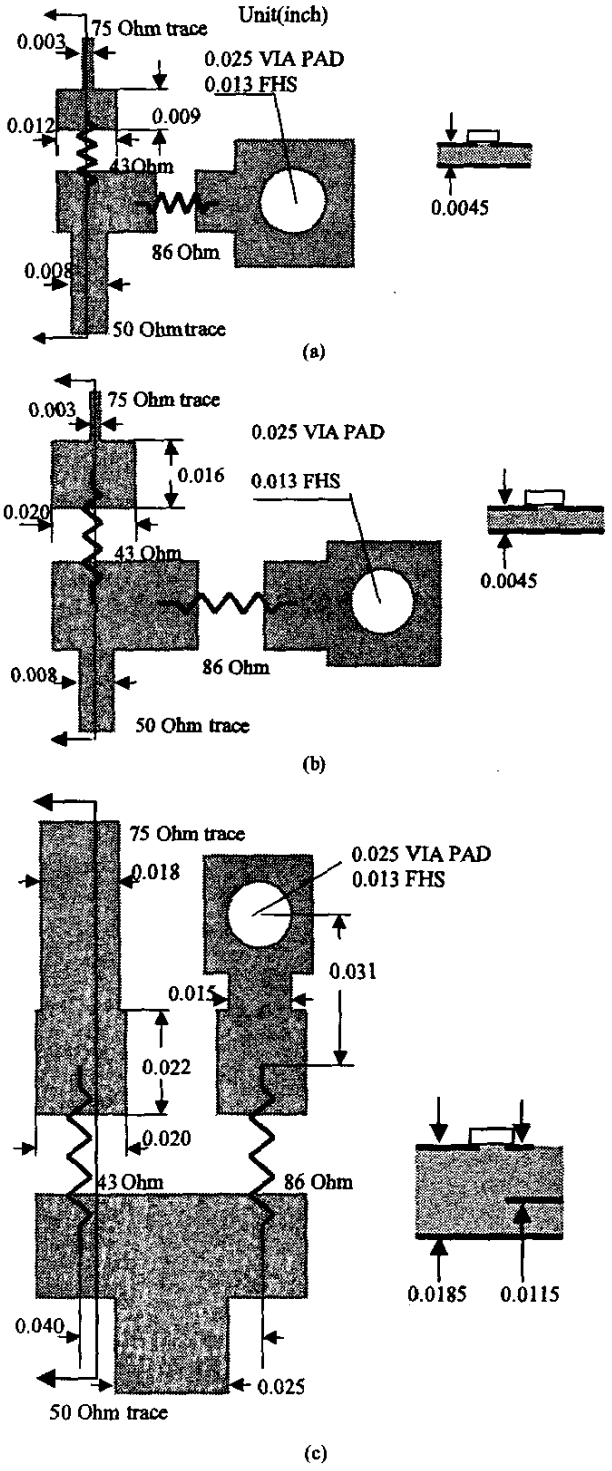

Figure 2. (a) 0201 impedance-matching network. (b) 0402 impedance-matching network. (c) 3-layer 0402 impedance-matching network

both impedance-matching networks, the differences in performance can be attributed to the discontinuities between the traces and the pads.

Since 0402 resistors were preferred because of board assembly considerations, a new improved 0402 design was proposed as shown in Fig. 2(c). A three-layer structure was used to decrease the discontinuities between the microstrip traces and the pads of the 0402 SMT resistors to mimic the geometry of 0201 matching network, with respect to the width discontinuity between trace and pad. The stackup was designed such that signal layer was on the top, and second layer was a reference plane for the 50 Ohm traces. The reference plane for the 75 Ohm traces was on layer 3, with the copper underneath the traces on layer 2 completely removed. The thickness between layers 1 and 3 was 18.5 mils, while the one between layers 1 and 2 was 11.5 mils. Under such design, the trace widths were widened. Fig. 3 and 4 show the simulation results modeled by CEMPIE. The return loss of the new 0402 matching network is improved and has comparable performance with 0201 matching network. The differences are less than 3dB in the frequency range from 100 MHz to 5 GHz.

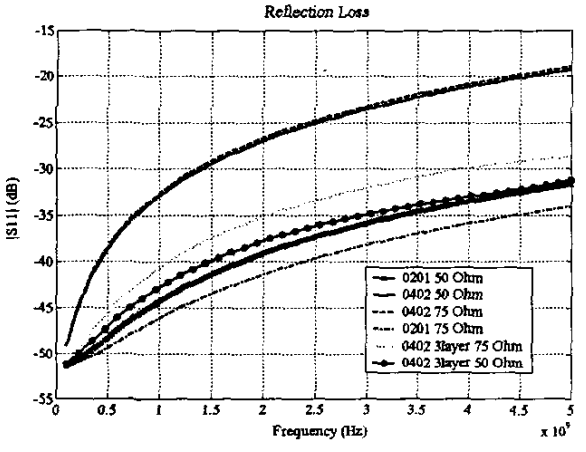

Figure 3. Modeled reflection loss.

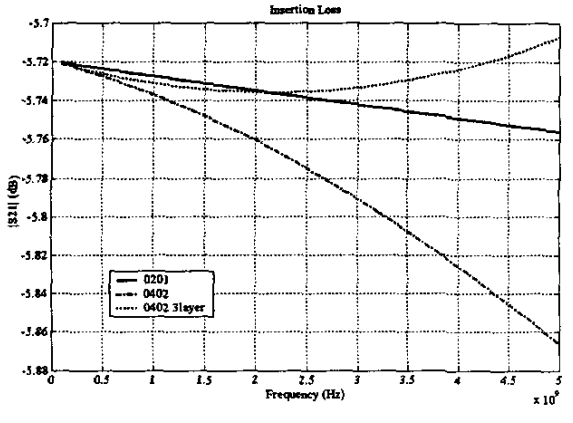

Figure 4. Modeled insertion loss.

A "through" structure comprised of the improved 0402 impedance-matching network (75-50 Ohm), a short 75 Ohm trace, and the same impedance-matching network but in reverse direction, was implemented and measured. Fig. 5 and 6 show the comparison of the measured reflection loss and insertion loss of the through structure comprised of the improved impedance-matching networks and coaxial matching networks.

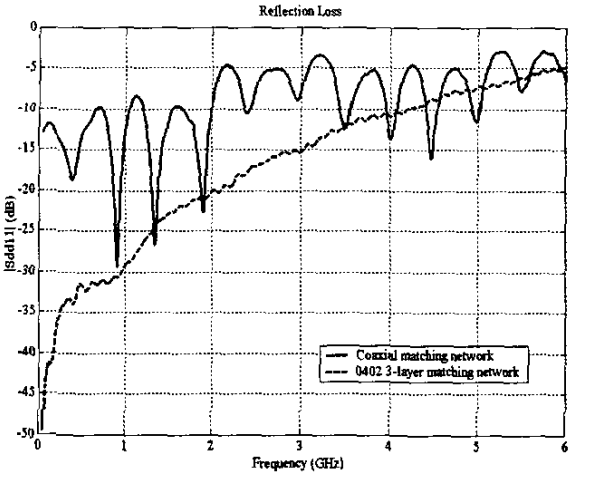

Figure 5. Measured reflection loss.

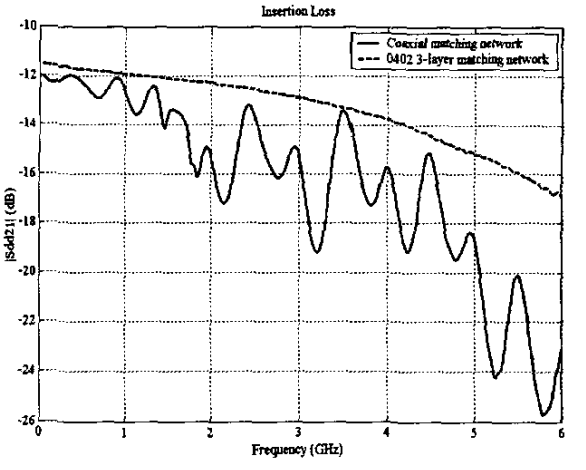

Figure 6. Measured insertion loss.

The coaxial impedance matching network was built around a Pasternak Enterprises Type N coaxial impedance matching pad cascaded on the 50 Ohm side with a short cable assembly comprising a short 50 Ohm coax terminated with a male type N 50Ohm connector on one end and an SMA connector on the pother end. On the 75 Ohm side, the cable assembly comprised a short 75 Ohm coax terminated with a mail 75 Ohm type N connector on one end and an SMA connector on the other end.,

The implemented impedance-matching network shows smaller reflection loss, better insertion loss and a far superior match over all. The reflection loss of the 0402 SMT network is as much as 10 dB lower than the coaxial structure at frequencies as high as 3 GHz and alternates between somewhat lower and in narrow band regions between 3 and 6 GHz. The insertion loss is superior across the spectrum by as much as 4 dB or more.

IV. CONCLUSIONS

An impedance matching network on a printed circuit board fabricated with 0402 SMT resistors was designed with the assistance of CEMPIE modeling in order to facilitate accounting for trace and package parasitics. By minimizing the discontinuities of microstrip traces and pads of resistors, the impedance-matching network using 0402 SMT resistors achieved a performance similar to that of the lower package parasitic 0201 SMT resistor-matching network. In this case, reflection losses for the 0402 SMT network were within 3 dB of the 0201 network over the frequency range of 100 MHz to 5 GHz. The insertion loss of the 0402 network was within a dB of the 0201 network, even at the highest frequency. This compared to a more conventional design with 0402 SMT resistors that produced reflection losses that were approximately 10 dB worse than the 0201 network. In short, SMT pad parasitics can be very important in impedance control, especially in the multi-gigaHertz regime. Discontinuities, such as between trace and pad, can be very important in impedance control, especially in the multi-gigaHertz regime. Modeling tools can be very helpful in understanding the effects of parasitics and mitigating those effects.

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