The development of flexible integrated circuits based on thin-film transistors

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Abstract

The use of thin-film transistors in liquid crystal display applications was commercialized about 30 years ago. The key advantages of thin-film transistor technologies compared with traditional silicon CMOS (complementary metal-oxide-semiconductor) transistors are their ability to be manufactured on large substrates at a low-cost per unit area and at low processing temperatures, which allows the transistors to be directly integrated onto a variety of flexible substrates. Here, I discuss the potential of thin-film transistor technologies in the development of low-cost, flexible integrated circuits for applications beyond flat-panel displays, including the Internet-of-Things and lightweight wearable electronics. Focusing on the relatively mature thin-film transistor technologies that are available in semiconductor fabrication plants today, the different technologies are evaluated in terms of their potential circuit applications and the implications they will have in the design of integrated circuits, from basic logic gates to more complex digital and analogue systems. I also discuss microprocessors and non-silicon, near-field communication (NFC) tags that can communicate to smartphones, and I propose the concept of a Moore's law for flexible electronics.

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Thin-film transistors (TFTs) are currently the dominant technology for in-pixel switches and drivers in flat-panel displays. Trends in consumer electronics demand ever higher display resolution and brightness, lower power consumption, and new features and form factors (such as curved and foldable displays). This drives TFT devices to deliver more complex functions than simply switching. For example, recent bezel-less displays delegate the selection of rows to be programmed to TFT circuits integrated next to the pixel array. Such driver circuits comprise thousands of switches operating together. This was previously a job for silicon chips mounted around the display.

Beyond displays, how far can thin-film circuits go in terms of replacing silicon CMOS chips? Fig. 1 illustrates the key advantages of thin-film circuits on flexible substrates. The circuits can be fabricated on large substrates, creating very thin, light-weight and ultra-flexible electronics[1,2]. Folding, rolling or crumpling the flexible circuits is possible without destroying the electronic functionality. Because of these properties, a flexible TFT-based microprocessor[3] (Fig. 1d) or a thin-film near field communication (NFC) tag (Fig. 1e) can, for example, be integrated imperceptibly into any object. Thin-film transistor technologies also have considerable potential for fabrication on ultrathin, stretchable substrates[4], which can be made porous creating breathable devices for contact to skin. With these features, thin-film integrated circuits (ICs) could be a gamechanger for wearable electronics. Ultra-thin, conformable ICs in the form of a tattoo, could be used to monitor vital body parameters, communicating these parameters directly to a patient's smartphone or to a medical doctor's database.

In this Perspective, I discuss the potential of thin-film circuits on plastic substrates for the development of Internet-of-Things (IoT) and wearable applications. I first look at the different TFT technologies that can be realized on flexible substrates, and then discuss the impact TFT technology will have on circuit design at the level of digital logic gates and VLSI (very-large-scale integration) digital circuits. For VLSI digital circuits, I consider the use of thin-film ICs in the creation of low-cost radio-frequency identification (RFID) tags for everyday items. Initially flexible chips may be used to simply identify each item. In a next step, when the RFID chip is potentially replaced with a thin-film near-field communication (NFC) chip, standard smartphones and tablets equipped with NFC readers could identify the objects and connect them to the cloud. Another advantage of thin-film IC technology is the possibility of being combined with sensor or signage technology, therefore integrating more functionality into the objects, and this is discussed in a section on analogue circuits. Finally, I will briefly examine the potential of silicon CMOS chip technology directly interfaced with TFT circuitry.

Thin-film transistor technology

The development and optimization of transistor technologies are driven by four important figures-of-merit: area, cost, power and performance. Power and performance are application-specific parameters, which tend to become more demanding as the application field evolves. As thin-film transistors are mainly developed for display-like applications, the drivers of technological evolution are the demand for higher resolution and brightness, which pushes transistors to increased density and semiconductor performance. This evolution is also beneficial for thin-film IC applications.

Thin-film transistor technologies have the potential to be low cost, due to the simple process flow (i.e. limited number of lithographical steps compared to Si CMOS) and material choices. Typical channel lengths for TFT technologies are in the μm range. Currently, thin-film integrated circuits are area-inefficient due to non-optimized design flows including the fact that transistor architectures have not been optimized for integrated circuits. As an example, a digital standard cell based CMOS IC comprises several metal layers dedicated to routing, which are on top of the Si CMOS transistor layers. Standard TFT transistor architectures on the other hand have a limited number of metal layers available (Fig. 1f), as it is not required for backplane applications. Interconnecting different standard cells for a TFT-based digital chip can only be realized by the metal layers already present in the TFT stack. Routing on top of such standard cells cannot be maximized resulting in a non-optimal area consumption of TFT-based digital chips.

At present, the mainstream thin-film transistor technologies, which are available in consumer electronics products, are amorphous silicon (a:Si), low-temperature polycrystalline silicon (LTPS) and amorphous metal-oxide semiconductors (mainly Indium-Gallium-Zinc-Oxide or IGZO) (Table 1). Metal-oxide TFT is a promising n-type only technology for flexible IC circuits, as it can be manufactured at process temperatures within thermal budget of flexible substrates[5], while still exhibiting a charge carrier mobility close to or above $10cm^2/Vs$, in contrast to $0.5-1cm^2/Vs$ for a-Si[6,7]. LTPS transistors require larger process temperatures and a more complex process flow, resulting in complementary p-type and n-type TFTs with larger mobilities ($50-100cm^2/Vs$)[7,8]. In addition, the amorphous nature of IGZO as a semiconductor[5] enables a TFT scaling roadmap, whereby shorter channel TFTs retain good performance characteristics, which is beneficial for both high resolution displays and flexible IC applications. In contrast, polycrystalline semiconductors have a negative impact on TFT behaviour

depending on crystal size and channel lengths. Short channel IGZO TFTs down to 30nm have been demonstrated already, for transistors fabricated in the back-end-of-line of a conventional silicon CMOS chip technology[9]. Moreover, organic transistors are widely studied as a potential candidate for flexible ICs to complement n-type metal-oxide TFTs[10], because p-type metal-oxides matching the performance of amorphous IGZO have not been discovered.

A recent review on the effects of mechanical stress on the intrinsic electrical performance of different semiconductors concluded that amorphous metal-oxide semiconductors are the most resilient under mechanical strain[11]. In addition, semiconductors are patterned mostly into small islands and the critical layers of the thin-film transistor stack can be located near the neutral plane of the full stack by matching the substrate and the topstrate or encapsulation. This is fully exemplified by the ultra-flexible organic TFT backplane, which measures a total thickness of only 2μm[1].

This article focuses on the mature technologies that are available in semiconductor fabrication plants (or fabs) today, Nevertheless, it is worth noting that recent developments with carbon nanotubes[12–15] and several two-dimensional semiconductors[16], such as graphene[15,17,18], black phosphorus[19] and chalcogenides[20–23], are encouraging and these materials could provide next-generation flexible TFT IC technologies, as a novel standalone transistor technology or by complementing existing TFTs. It also worth noting that a key benefit of some TFT technologies is the possibility to use additive manufacturing techniques like printing, which could reduce costs[24–29]. The main challenges of printed electronics at a circuit level are variability (device mismatch), large overlaps (source-drain to gate) due to layer-to-layer registration rules increasing the parasitics, and large device dimensions, which result in slower operating circuits.

Digital logic gates
Logic gates are the building blocks for complex digital circuits and require specific optimization depending on the process technology. The most optimal configuration is CMOS, profiting from the co-existence of complementary p-type and n-type transistors and all the circuit-techniques developed for conventional Si CMOS since the 1970s. In LTPS complementary logic is possible, but organic and metal-oxide TFTs do not have adequate complementary counterparts. The level of matching of both transistor-types will affect the properties of the complementary logic gate, including speed, power, robustness and area. In a complementary technology, both transistor types need to possess a near-zero threshold voltage and sufficiently low off-current. Furthermore, the charge carrier mobilities must differ by no more than a decade. The low threshold voltages are necessary and key to downscaling the supply voltage. Off-currents impact directly the static leakage current of the logic gate in the on- or off-state and therefore total power consumption. Fig. 2 shows an example whereby the off-current of the p-type transistor contributes mainly to the static power consumption for different integration levels of the targeted circuit. Low off-currents will become more important for higher circuit integration densities. In addition, differences in charge carrier mobilities between the n-type and p-type TFTs have an impact on area, speed and power. If the mobilities differ too much, the area consumption and speed of the complementary logic gate will be negatively affected in favour of unipolar logic gates.

A complementary technology flow is more complex compared to the fabrication of a unipolar transistor technology, and the additional steps for a complementary flow relate directly to an increased manufacturing cost. Therefore, from the cost perspective, unipolar technologies

can be beneficial for the realization of the flexible digital IC, especially when there is no area reduction as a result of the introduction of a non-matching complementary semiconductor.

Unipolar logic gates are the main option to realize flexible ICs for the TFT technologies that do not have a complementary counterpart. The main disadvantages of unipolar logic gates with respect to complementary logic gates are a reduced robustness[30], and an increased area and power consumption. Fig. 2 details different unipolar logic topologies. Resistive-load logic requires on-chip resistors, and will result in the lowest TFT-count. If the technology does not offer resistors in the right range, alternatively a TFT can be used as a load. Two options are shown in Fig. 2e-f: enhancement-load or diode-load logic and depletion-load or zero-V_{GS}-load logic. Selection of those depend on the available threshold voltage of the existing technology. Zero-V_{GS}-load logic only operates with normally-on devices, or devices which are already switched on at 0V gate bias. Diode-load logic is operating much faster compared to zero-V_{GS}-load logic, but suffers from a low gain and reduced noise margin and therefore robustness[31].

Several methods can be used to increase the robustness of these logic gates. One option is to increase the number of transistors per logic gate in order to improve the noise margin at the cost of area. Alternatively, transistors can be operated in two different operation modes – depletion and enhancement – or at least with two different threshold voltages per logic gate. A practical implementation of different threshold voltages can be rooted in the technology, by, for example, doping the channel, by varying the thickness of the semiconductor, or by varying the gate-dielectric thickness. A consideration in the choice of the implementation is that the process flow should stay sufficiently simple that yield and cost remain attractive.

By nature of having a thin film of semiconductor as the active layer, a thin-film transistor can naturally be equipped with two gates: the front-gate and back-gate. A back-gate operates in a similar way as the body bias of Si CMOS and can be used to regulate the threshold voltage of each TFT individually. Dual-gate unipolar inverters have proven already their benefits in terms of logic gate robustness[32] without an additional penalty on area. In this solution, a global, chip-level bias signal to shift the V_T of, for example, all drive TFT is required. The inverter scheme is shown in Fig. 2g.

The logic gate robustness can also be improved for back-gate-free TFT technologies by introducing more transistors per logic gate. Two examples are level shifters[33] and Pseudo-CMOS logic (Fig. 2h)[34]. Both options allow to shift the voltage transfer curve of the inverter towards the middle of the power rail, improving the robustness. Besides an increase in consumed area, an additional power rail to drive the additional TFTs may be required for optimal operation. Positive feedback level shifter logic employs 4 to 5 TFTs for an inverter function with only 2 power supplies[35]. This logic style results in the largest unipolar inverter gain and therefore noise margin per supply voltage published to date (76dB and 8.2V on 20V respectively), which is obtained by positive feedback on the backgate, including a global signal within power rails to tune individual threshold voltages. Finally, robustness of unipolar logic can be improved by using unipolar differential logic at the cost of larger area consumption[36]. Latter logic style uses only unipolar single gate TFTs and combines positive feedback to the concept of differential logic.

A fundamental problem for unipolar logic gates is the static power consumption. Dynamic logic is therefore an interesting direction as it has already been proven to lower the static leakage current and improve the area usage[37]. The leakage current of the technology has an

impact on the operating frequency. VLSI TFT circuits based on such clocked dynamic logic is still a challenge because of the more difficult design and strong requirements on clock synchronization.

Future trends may be to invent novel logic gates, based on unipolar technologies that actively compensate for shortcomings of regular unipolar logic gates, without the necessity to add its complementary counterpart and consequently a more complex process flow. Such logic gates may employ additional transistors with feedback function to reduce the leakage of the transistors after the switching action has occurred[38]. Feedback circuits on system level to disable large idle blocks are also unexplored for TFT circuits.

A third direction to lower the power consumption can be sought in technological improvements or even evolutions. Technology scaling similar to Moore's law for flexible thin-film ICs may also be crucial for the realization of complex VLSI circuits on foil, paving the way to a larger portfolio of applications. The intrinsic delay of scaled logic gates will improve with the scaling factor when full scaling (equal in voltage and geometry) is applied (Fig. 2c). The density per function improves with the square value of the scaling factor, so does the power per function. The power density remains therefore equal. The NFC chip described in the next section is comprised of 1712 metal-oxide n-TFTs, exhibiting 7.37ns gate delays and a 7.5mW power consumption. Fig. 2c recalculates this for 10,000 TFTs, assuming mainly static power losses. Applying Moore's law on flex towards a 200nm gate length results in 438µW power consumption for 10000 n-TFTs and 737ps gate delay. These numbers only consider the advancements of the device parameters. In reality, parasitics from the interconnects play a crucial role and need to be taken into account. Lowly-resistive and strongly decoupled metal wires for interconnects are also of high importance to realize this roadmap. Power density will be of huge importance in future, as circuits tend to evolve into more complex chips yielding more functionality and transistors at a similar area. Power consumption and Joule heating will require particular attention in thin-film technologies because plastic substrates and thin-film metals are poor heat conductors. If dynamic power consumption in those novel logic styles proves to be dominant, additional voltage scaling and clock frequency reductions (parallelism, pipelining) may contribute to lower the overall power consumption. Other well-known techniques as optimal device sizing, clock gating and utilization of different logic styles in one chip (fast logic gates versus low power logic gates) can be elaborated for VLSI flex ICs.

TFT technologies are expected to further improve parameters such as charge carrier mobilities, variability and bias instabilities. Larger mobilities will enable logic gate optimizations in terms of speed, area or a combination of both. With LTPS and amorphous oxide TFTs the state of the art transistor has a self-aligned architecture with minimum parasitic overlap between gate and source/drain[8,39–41], leading to fast logic gates with small power consumption. Fig. 2c shows such power and delay improvement for slower etch stopper layer (ESL) and faster self-aligned (SAL) metal-oxide TFT technologies. Fig. 1f details the cross-section of both TFT architectures. ESL transistors exhibit a large parasitic gate-source and gate-drain overlap capacitor, which is substantially minimized for the SAL architecture. In addition, the channel length of the SAL technology is equal to the definition of the gate layer which makes it easily scalable, while on the other hand the channel length of the ESL technology is approximately three times its critical dimension due to all necessary overlaps by including the channel protection layer. More evolutions in stack definition are envisioned to provide more metallization layers for interconnects and for downscaling the transistor footprint.

Towards VLSI (digital) circuits on foil

Radio-frequency identification tags have received a lot of attention in the field of thin-film electronics as they could act as low-cost IoT nodes or tag everyday objects. High-frequency RFID tags, operating at 13.56MHz base carrier frequency, operate at maximum distances of 10cm for proximity readers and up to distance of 1m for vicinity readers. TFT-based RFID tags can be grouped into two categories: tags that communicate to custom-built RFID readers with own defined protocols, like 8-bit, 12-bit or 16-bit tags[41–45]; and tags that communicate to commercial NFC readers, embedded in many smartphones and handheld devices. The chip design requirements are less stringent for the first category, as protocols can be defined with reduced complexity to account for the technology limitations of TFTs. Small-sized dedicated chips are targeted with limited number of transistors (<1000) embedding easy protocols, which is less interesting for Si CMOS technologies.

NFC tags need to comply with ISO standards (e.g. ISO 14443-A), set for Si CMOS technologies exhibiting approximately 100x larger charge carrier mobility values compared to metal-oxide TFTs. The selected ISO standard is the NFC Barcode protocol, a tag-talks-only protocol whereby the tag transmits its 128bit memory during 1.21ms and remains silent for 3.6ms. This fast NFC protocol can detect a tag within 5ms. The three main challenges to design a metal-oxide TFT-based NFC Barcode tag are the data rates of 106kbit/s (or carrier frequency divided by 128), a 128bit memory read out including 16 CRC bits and a limited incident power at the tag from the smartphone in the range of ~10mW. The technology for this work is a self-aligned metal-oxide TFT architecture, which was selected because of the strongly reduced parasitics and possibility to downscale the channel length to 2µm and 1.5µm (see Fig. 1f). Pseudo-CMOS logic gates have been chosen to serve as logic family maintaining the robustness of the chip without the presence of a backgate. Different implementations of the pseudo-CMOS logic gate have been used across the design serving different purposes, namely fast implementations for the clock division part and low power implementations for the core part.

Fig. 3 depicts the effect of channel length downscaling. The gate delay of a pseudo-CMOS inverter at 5V VDD and 10V VBIAS improves from 63.4ns to 5.2ns for 5µm to 2µm channel lengths. This is within the spec of 7.37ns, determined as maximum gate delay to directly divide the 13.56MHz incoming clock signal. A fast pseudo-CMOS implementation with 1.5µm channel length (L1.5F) results in a gate delay of 2.4ns at 5V VDD and 10V VBIAS.

These gate delays are sufficient to divide 13.56MHz carrier frequency, however, the power figure of these gates suggests a limited use of these gates in the design of the full chip. Therefore, four different ratios yielding low power pseudo-CMOS implementations have been evaluated, resulting indeed in a lower power operation with a small hit in gate delay (Fig. 3c-d), which is affordable for the core part of the chip. Another key advantage of the low power implementations, especially LP3 and LP4 is the more symmetric power distribution between VDD and VBIAS (Fig. 3g). This will ensure the correct generation of VDD and VBIAS by the rectifier circuit, as both power nodes observe a similar load.

Low power optimizations at system and architectural level have been performed by selectively choosing the proper pseudo-CMOS implementation where needed. The clock generator is a 7-stage toggle-flipflop chain, whereby the first stage is implemented with L1.5F logic (Fig. 4b). The power consumption has been decreased gradually along these 7 stages by selecting slower and power friendly pseudo-CMOS gates. The final stages are implemented with LP3 at channel length 4µm. Latter flavour has been also used for the digital core part (Fig. 4c). The data

formatting block requires slightly faster operating, therefore LP3 at channel length 2μm has been selected. The CRC code has been hardwired or preprogrammed in the memory since a regular CRC generator would add up to 1/3 of the total number of TFTs. This results in a substantial reduction of the static power consumption. The memory has been realized in two generations, the first generation is just synthesized ROM memory, the second generation is laser-programmed ROM (LPROM) memory. In latter design, 16 bits of the payload and 16 CRC bits are one-time programmable in the memory.

Fig. 4h shows the die picture of the combined clock generator, digital core generator and data formatting block. The size of the final chip is determined by the geometry of the standard cell library and the number of metals used for interconnects, in this work limited to 2, which also serve as gate and source/drain layer. An example standard cell is a 2-input NOR gate (Fig. 4d), employing 6 IGZO TFTs and measuring $163 \times 290 \mu m^2$. The die picture of the chip also reveals the location of the standard cells and the gaps in between the cells for the automatic place and route algorithm. The efficiency of the routing and therefore downsizing the chip can be envisioned by introducing more routing layers, as discussed previously. The standard cell library consists of 6 cells, including a buffer and a flipflop. As automatic place and routing algorithms introduce more parasitics, it was decided to manually route the most time critical blocks, like the clock generator and the data formatting block.

The final chip operates successfully at 3V supply and 6V VBIAS, consumes only 7.5mW power for 1712 n-TFTs and measures $50.55mm^2$ (Fig. 4e)[46]. Fig. 1e shows the photograph of the flexible NFC Barcode chip, including rectifier and load modulator, combined to an inductive antenna. The chip serves also as the bridge connecting the antenna. The preprogrammed 128-bit memory on the flexible NFC tag can be successfully tapped wirelessly into an NFC-enabled smartphone. Fig. 4e-g provides more measurement details and shows the power increase of the chip versus the supply voltage. In addition, the measured signals of the IGZO NFC Barcode tag when approached by an NFC reader device are plotted in Fig. 4f-g. At first the correct protocol behaviour is observed, with a silent period of 3.6ms alternating between 1.21ms code transmission. A more detailed zoom of the first bits in the sequence shows the correct bit representation and bit-timing according to the ISO 14443-A protocol.

Another interesting and complex digital circuit is a microprocessor. The first, and until date most complex, thin-film flexible microprocessor has been published in 2005[3]. It comprises 32k-transistors based on flexible complementary LTPS transistors, which has been released from carrier by means of the SUFLTA process flow[47]. The first unipolar organic microprocessor fabricated directly on flexible substrates exhibited a clock frequency of 40Hz to execute 8-bit operations[48]. In addition, 1-bit scalable microprocessor architectures have been demonstrated based on different emerging foil-compatible semiconductors, namely carbon nanotubes[12] and two-dimensional materials[49]. Solution-processed n-type metal-oxides have been combined to an evaporated p-type organic semiconductor resulting in the first hybrid organic/oxide 8-bit complementary thin-film microprocessor, operating at 2.1kHz[10]. Extrapolating the speed of the microprocessor by replacing the logic gates with aforementioned fast pseudo-CMOS logic gates may result in above 100k instructions per second calculation power enabling a broad application window. The power consumption of this chip may probably exceed the application specifications, demanding for many techniques to reduce the power consumption. At system level, disabling idle blocks in the architecture during operation by power gating, clock gating or active feedback via the backgates can reduce power consumption. It will also be a great asset if complex architectures can be designed specifically for the application. Gates which are not used should be eliminated[50], memory and

bus widths should be sized compliant to the application requirements and overheads of VLSI circuits should be limited. If sufficiently fast data processing can be brought to foil at low area and power consumption, a large application field can be envisioned whereby data can already be preprocessed at patch or IoT-node level.

Analogue circuits

Internet-of-Things sensor nodes collect data in the analogue domain, to be digitized with analogue-to-digital or time-to-digital converters prior to cloud storage. Data processing in digital domain is advantageous for TFT-based circuits as digital circuits are more mature than analogue TFT-circuits. Analogue to digital converters have already been demonstrated in thin-film transistor technologies, based on a:Si, organic, metal-oxide and LTPS transistors, yielding up to 8bit conversion at a maximum sampling rate of 300S/s for unipolar IGZO technologies[51]. Many advancements are still required prior to developing commercial products, which will be a gradual process from 1bit threshold sensing to multibit sensor conversion.

The analogue TFT world also benefits from the technological evolutions discussed in previous section. Introducing higher mobility semiconductors will lead to faster sampling rates and a larger transconductance, assuming other TFT and process parameters remain similar. The conversion speed can be increased by downscaling the TFT technology, however, the already limited gain of the operational amplifier or comparator is possibly reduced due to a lower output resistance for scaled TFTs. Improvements in variability and bias instabilities will lead to lower offset for differential amplifiers leading to an increased accuracy of the conversion. The introduction of a matching complementary TFT is likely to be the most significant development for analogue electronics, more than for digital flexible ICs, improving conversion rates, strongly enhancing the offset and gain of the amplifiers and downscaling of the consumed area. Analogue circuits based on unipolar technologies benefit already if stable passives are included in the process flow, like a high-resistive layer with low variation, improving the area and gain of the amplifiers.

Amplifiers are required for a multitude of applications, not limited by sensor-node IoT. Integrated sense amplifiers are beneficial to read out different memory topologies in a rapid fashion, from LPROM to SRAM[52] and in future non-volatile memory arrays embedded in thin-film transistor technologies. Large area imaging backplanes require in-pixel amplification and sense amplifiers to detect the incoming signals. Low noise amplification based on TFT-technologies can also find its way in wearable health patches to monitor vital signals whereby sensors or electrodes are attached to the body and interconnected to a Si CMOS IC. The analogue amplifiers can be mounted nearby the sensor/electrode to improve the signal-to-noise ratio of the sensor signal prior to transmission to the Si IC. Single stage high gain amplification in such patches is a strong asset, which has been demonstrated already by means of positive feedback mechanism and backgate technology in a unipolar IGZO technology, leading to 30dB gain[53]. The backgate can enable multi-threshold voltage logic as discussed in previous section, but can also improve the transconductance or the output resistance of the individual transistors. Improvement of those TFT parameters is a valuable property for analogue circuits, which consists of load TFTs and current sources that require a large output resistance, or improved transconductance for the input pairs, leading to 50dB gain of a 3-stage unipolar metal-oxide amplifier[54].

To understand the mismatch or the deviations of parameters between two transistors is of key importance for the design of analogue electronics. A mismatch law for conventional Si

CMOS has been reported[55], and it was concluded that device parameter mismatch is inversely proportional to the square root of the device area ($W \times L$). A properly operating differential input pair or a current mirror circuit relies on the matching properties of two transistors. It has been shown that the spread in organic transistor characteristics is too large, excluding the design of a current-steering DAC architecture[56]. Instead, for this organic technology, it was found that the capacitor mismatch follows Pelgrom's area-scaling rule, resulting in a 6-bit switched-capacitor architecture. An interesting post-fabrication select-and-connect method has also been reported to cope with large mismatch values for organic transistors[57]. This method led to an optimal area and power overhead reduction, compared to the introduction of many parallel transistors. Device mismatch is not solely a problem of manufacturing (dimensions, doping, interfaces, etc.), but can also occur during handling and operation. Mechanical handling of flexible electronics can introduce locally tensile or compressive stress on the device and therefore impact the characteristics. A proper floorplan of the design to accommodate for such effects in final product handling is required. During operation, two transistors in a differential pair may be biased with different conditions, resulting in different bias stress current degradation for both transistors. This will impact the proper functioning of the differential pair, as device characteristics start deviating. It will be important for future developments, as technologies mature, to obtain accurate models of the transistor behaviour under different circumstances, ensuring correct functioning of the analogue blocks without severe design overhead.

Health patches or sensor nodes combined with RFID or NFC tags is an intriguing direction for this field. From previous section, it is demonstrated that an accurate and stable time signal or clock can be derived from the incoming carrier frequency in an RFID tag. This time reference can be used to convert the sensor signal to a digital value via a time-to-digital converter. A full NFC solution based on the NFC Barcode protocol sets restrictions for the data conversion rate, as 128bit data is transmitted within 1.21ms. The minimum time for analogue conversion can take about 1ms, depending on the number of occurrences needed prior to smartphone detection. Afterwards, the converted digital bit sequence needs to be included, together with a newly calculated 16bit CRC number, albeit by means of a CRC generator, a look up table or a synthesized code scheme. The number of converter bits will decide which of the previously discussed solutions may be the most appropriate, given the area and power constrains of the tag.

Hybrid combination of silicon CMOS and TFT technologies

There are number of potential opportunities for Si CMOS chip technology to be directly interfaced with TFT circuitry. I focus here on solutions in which there is a clear gap in system requirements and solutions offered by specific IC technologies. Flexible TFTs are mainly limited in electrical performance, for example, Bluetooth or WiFi communication with TFTs is today not possible due to the limited cut-off frequency. However, Si CMOS ICs are limited in number of input/output pads and have area constraints. Therefore, it would be beneficial in some cases to combine at system level silicon CMOS ICs and TFT flexible chips. The choice for this solution will be strongly dependent on the system requirements and affect the cost and the complexity of the solution. An example of such integration can be the hybrid system in foil approach[58,59] in which a thinned silicon CMOS IC is embedded in a flexible substrate and combined to foil-compatible TFT technologies and sensors. Previous sections discussed some examples where at one side a Si NFC reader chip wirelessly connects to a flexible TFT-based NFC tag, and also a TFT low noise amplifier located near a sensor input to improve the signal to noise ratio prior to transmitting this analogue signal to a Si chip. More obvious

examples are in fact active matrix displays and imagers. A TFT backplane in a display uses the transistors solely as switches or to regulate the current through the OLED frontplane. More advanced pixel schemes also employing multiple TFTs per pixel compensating for non-idealities of TFT backplanes, like bias instabilities or uniformity issues. The Si CMOS chips, like a GPU, will translate the display image into the desired data and select signals. The trend towards bezel-free displays moves more complexity to the TFT backplanes, integrating TFT-based scan drivers for the select signals and multiplexers to reduce the number of data control signals.

A multiplexer/demultiplexer circuit based on TFTs could be of value in actively extending the limited number of input/output (IO) pins of a Si CMOS chip. Applications requiring a large number of sensors or actuators can be envisioned. A large area wearable patch can therefore consist of a large array of distributed electrodes whereby a TFT-based amplifier or analogue-to-digital converter is attached to each electrode. The pre-treated signals are subsequently transmitted to one Si CMOS IC by means of a TFT-based multiplexer, in which time-division multiplexing or frequency-division multiplexing of the IOs are two valid candidates. The bandwidth of the multiplexer will depend strongly on the used technology, the voltage range, the number of IOs and the power budget. Downscaling of TFT technologies will lead to lower supply voltages, and 5V, 3.3V, 1.5V and sub-1V VDD voltages can be envisioned, enabling direct communication of the flexible TFT IC to a Si CMOS IC[60]. On the other hand, Si CMOS ICs that need to drive high voltage actuators can make use of TFT-based level shifters to increase the CMOS compatible voltage range to the actuator requirements.

Conclusions

This article discussed the opportunities and shortcomings of thin-film transistor technologies for applications beyond displays, such as low-cost IoT and wearable electronics. In order to optimise cost, robustness, area and power, improvements in transistor technology need to be driven by the needs of flexible TFT-based ICs. A circuit-specific technology improvement includes the introduction of the concept of Moore's law for flexible electronics, in which flexible chips may become smaller, thinner and higher performing. Another key asset for TFT technologies is an individual backgate for each transistor, which can be employed in logic gates to enable multi-V_T and therefore more robust digital logic, or in analogue circuits where the transconductance or the output resistance need to be adapted. Flexible circuit technology developments may also need the introduction of extra metal layers in addition to the gate and source-drain layer, for routing complex digital circuits, which may improve the circuit power consumption, speed and area usage. Unipolar logic circuits have clear advantages over complementary logic gates in terms of a simpler process flow and therefore lower costs, which is an important aspect for these technologies.

Technology-aware design improvements are also necessary to bridge the shortcomings of TFT technologies. Several TFT technologies are limited to only unipolar semiconductors, therefore various implementations of unipolar logic gates have also led to improvements in terms of robustness, dynamic performance and power consumption. This has been realized by employing more transistors per logic gate, or by actively implementing the backgate. In the future, more dedicated improvements regarding this topic are required to enable applications that require more complex flexible ICs with a higher integration density, operating within power and speed budgets for the applications. A complementary process flow combining n-type and p-type TFTs may result in a more complex manufacturing, but has great circuit performance advantages. Potentially, different transistor technologies, like two-dimensional

materials or carbon nanotubes may be envisaged to be integrated with the unipolar TFT technologies, enabling favourable complementary logic. Complex digital and analogue TFT circuits have been demonstrated already, from RFID tags to analogue-to-digital converters to flexible microprocessors, indicating the readiness of TFT technologies for such applications. A TFT-based unipolar NFC tag has been discussed, in which power consumption and speed has been optimized at logic gate level and system level. This leads to a 7.5mW IGZO-based NFC tag that can tap its information directly into a NFC-enabled smartphone. Such an ultrathin tag can be invisibly embedded into everyday objects, enabling item-level IoT nodes.

Acknowledgements

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Table. 1. Comparison of different properties and applications for the four thin-film transistor technologies (a-Si, LTPS, Oxide and Organic).

Fig. 1. Examples of flexible electronics and their applications. **a.** Illustration of a thin large-area active-matrix sensor with 12 × 12 tactile pixels. **b.** Ultrathin plastic electronic foils are extremely lightweight ($3\,g\,m^{-2}$); they float to the ground more slowly than a feather and are therefore virtually unbreakable. Scale bar, 2 cm. **c.** At only 2 μm thickness, these devices are ultra-flexible and can be crumpled like a sheet of paper. Scale bar, 1 cm. **d.** Photograph of a flexible thin-film transistor based microprocessor. **e.** Photograph of a flexible thin-film transistor based NFC tag. **f.** Cross-section of an etch stopper layer (ESL) and self-aligned (SAL) amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) transistor configuration. The channel length (L_{ch}) is indicated. There are two metal layers available: metal 1 (M1) or gate, and metal 2 (M2) or source-drain (SD). Silicon dioxide (SiO_2) and silicon nitride (SiN_x) are typically used as dielectric and passivation layers. Panels **a, b, c** from ref. 1, **d** from ref. 3.

Fig. 2. Predicted impact of TFT technology parameters on power consumption and logic styles. **a.** TFT transfer characteristics of complementary transistors with equal mobility and threshold voltage, whereby the p-type off-current is varied. **b.** Impact of varying p-type off-currents on the static power consumption of complementary logic gates for increasing integration. **c.** Impact of technology improvements between IGZO etch-stopper layer (ESL, Fig. 1)[44], self-aligned (SAL, Fig. 1)[41] and scaled SAL[46] on power consumption and gate delay. The data points of this graph stem from a 12-bit IGZO RFID transponder chip realized in ESL[44] (black square) and SAL[41] (black circle) technologies. The IGZO NFC chip is represented by the red circle, realized in a scaled SAL technology[46]. The red dashed line shows the impact on power and gate delays for the scaled SAL NFC chip, if Moore's law on flex would be applied with full geometry and voltage scaling, ranging from 5μm to 200nm. The blue square is a stretched target, revealing the necessity of additional circuit and technology evolutions to reach ultralow power, fast operating circuits. **d.** n-type resistive-load logic. **e.** n-type diode-load logic. **f.** n-type zero-V_{GS}-load logic. **g.** dual-gate n-type diode-load logic. **h.** n-type diode-load pseudo-CMOS logic.

Fig. 3. Optimization of single-gate pseudo-CMOS logic gates for power and speed. **a,b,** Impact of channel length downscaling for regular and fast implementation of pseudo-CMOS logic on stage delay (**a**) and power (**b**) consumption. **c,d,** Impact of different low power implementations of pseudo-CMOS logic on power consumption (**c**) and stage delay (**d**). **e.** Overview table of different transistor sizes for all implementations; F stands for fast, LP implies low power. **f.** Schematic of a pseudo-CMOS logic gate. **g.** Relative power distribution between VBIAS and VDD for different pseudo-CMOS logic gate implementations. **a,b,c,d,e** From ref. 46.

Fig. 4. The design of the IGZO NFC Barcode foil. **a.** System overview and key blocks of the IGZO NFC Barcode Tag. **b.** Detailed block diagram of the clock generator, exhibiting 7 toggle flip flops. **c.** Detailed block diagram of the digital core part, designed in the LP3 library with channel length 4μm (L4_LP3). **d.** Standard cell layout of a NOR-2 input gate, measuring a width of 163μm and a height of 290μm of the L4_LP3 library. **e.** The measured power consumption of the barcode chip versus the supply voltage. **f.** Measurement details of the fully integrated IGZO NFC barcode with antenna displaying correct behaviour when approached with an NFC reader device. **g.** Zoom of the first bits displaying correct bit representation of the ISO 14443-A standard. **h.** Die photograph of the IGZO NFC foil, indicating the three main block diagrams. **b,c,e,f,g,h** From ref. 46.