## The Effect of Short Channel on Nanoscale SOI MOSFETs

D. Rechem and S. Latreche

Laboratoire Hyperfréquence et Semi-conducteur (L.H.S), Département d'Electronique, Faculté des Sciences de l'ingénieur, Université Mentouri de Constantine, Algérie

## 1. Introduction

Double gate silicon-on-insulator (DG SOI) devices have recently been of great interest, particularly for the investigation of sub-10nm field-effect transistor [1]-[3]. As the channel length is reduced from one transistor generation to the next, the susceptibility of the transistor to short-channel effects (SCE) is monitored in several ways such as threshold voltage ( $V_{TH}$ ) roll-off, sub-threshold voltage swing, and the drain induced barrier low, the channel length decreases and becomes crucial in deep-submicrometer technologies. As an indicator of these short channel effects, the threshold voltage and sub-threshold voltage swing has been extensively investigated [4]-[7].

In order to maintain a tolerable degree of short channel effect [8], it becomes necessary to reduce the SOI film thickness. Reducing the SOI film thickness causes a high electric field in the perpendicular direction to the Si/SiO2 interface, strongly confining charge carriers in the channel. Several interesting models have been proposed for the classical (i.e., without quantum effects) drain current [9]-[11]. Carrier quantization effects have been considered for the first time in [12]. Therefore, classical models that disregard these effects are no longer suitable for describing sub 10nm MOSFETs. Therefore, we use quantum mechanical transport models for n-channel MOSFETs based on the self-consistent Schrödinger and Poisson equations for the simulation of short channel effects on the performance of DG-MOSFET. In addition to it, the model is continuous over all gate and drain bias ranges, which makes it very suitable to simulate novel silicon transistor structures.

2. Results

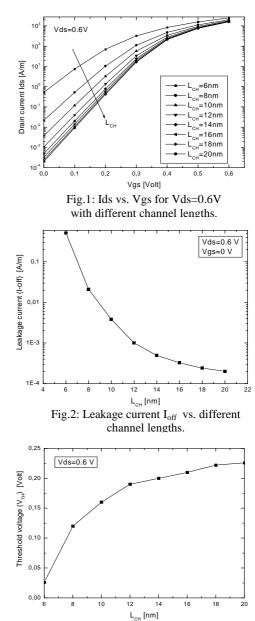


Fig.3: Threshold voltage vs. different channel lengths.

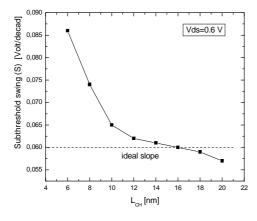


Fig.4: Sub-threshold swing vs. different Channel lengths.

## 3. Conclusion

A two dimensional self consistent Poisson Schrödinger model is used with appropriate boundary conditions to explore the short channel effect in double gate MOSFET as channel length varied in the range of 20nm down to 6nm. The model is particularly dedicated to ultra-scaled devices. The short channel behaviour of the double gate MOSFET is evaluated based on the threshold voltage, sub-threshold swing and leakage current variation with channel length. It is found that those parameters, which characterize SCE, present a significant degradation when decreasing the channel length.

## References

- [1] M. S. Lundstrom and Z. Ren, IEEE Trans. Electron Devices **49**, No.1 (2002).
- [2] Z. Ren, R. Venugopal, S. Datta, M. S. Lundstrom, D. Jovanovic and J. G. Fossum, IEDM Tech. Digest p.715 (2000).
- [3] Yiming Li and Hong-Mu Chou, IEEE Transaction on Nanotechnology **4**, No.5 (2005).
- [4] Vishal P. Trivedi and Jerry G. Fossum, IEEE Electron Device Letters **26**, No.8, (2005).
- [5] Qiang Chen, Evans M. Harrel and James D. Meindl, IEEE Trans. Electron Devices 50, No.7 (2003).
- [6] Qiang Chen, Bhavna Agrawal and James D. Meindl, IEEE Trans. Electron Devices 49, No.6 (2002).
- [7] Qiang Chen, Lihui Wang and James D. Meindl, "Physics-Based Device Models for Nanoscale Double-Gate MOSFETs," IEEE International Conference on Integrate Circuit Design and Technology (2004).

- [8] D. Frank, Y. Taur and II. Wong, IEEE Electron Device Letters **19**, 385 (1998).
- [9] M. Heydemmann, "Résolution numérique des équations bidimensionnelles de transport dans les semi-conducteurs," Doctorate dissertation, Paris Sud University (1972).
- [10] D. Rechem, M. Lakhdara and S. Latreche, "Modélisation bidimensionnelle d'un transistor MOS a canal N par la méthode des différences finies," International Conference in Applied Computing. November 2005, B.B. Arreridj, Algeria.
- [11] S. Latreche, "Etude de transistors bipolaire a émetteur polysilicium autoaligne réalises en technologie CMOS," Doctorate dissertation, University of Constantine (1998).
- [12] G. Baccarani and S. Reggiani, IEEE Trans. Electron Devices 46, 1656 (1999).