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The Effect of Tungsten Volume on Residual Stress and Cell Characteristics in MONOS

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ABSTRACT The effect of residual stress during the tungsten deposition process were investigated using metal–oxide–nitride–oxide–semiconductor (MONOS) devices. The variation of residual stress due to tungsten volume was measured under tensile and compressive stress conditions. Residual stress increased in proportion to the deposition volume. Stress influenced the Si/SiO_2 interface and caused deterioration of the electrical properties, which was experimentally observed during measurements of the interface trap densities and memory windows. We confirmed that residual stress led to degradation of the cell characteristics of MONOS devices, and the absolute value of stress significantly affected these issues regardless of the polarity. From our experiments results, we can predict the degradation of cell characteristics in memory devices, and confirm the need for appropriate stress control in manufacturing process.

INDEX TERMS Residual stress, tungsten volume, curvature method, interface trap densities, MONOS structure.

I. INTRODUCTION

Three dimensional (3D) NAND architecture has become mainstream in NAND flash memory markets, producing better reliability, bit-density, and cost effectiveness than comparable technologies [1]–[3]. Manufacturers are mass-producing 3D NAND flash memories through bit-cost scalable (BiCS) and terabit cell array transistor (TCAT) technologies [2], [3]. However, to meet the explosive demands for data storage, residual stress issues must be resolved, which are caused by mismatches between heterogeneous materials or thermal and mechanical loads encountered during fabrication. Residual stresses can further result in stack deformation, substrate distortion, and even cracking of the film or substrate [4], [5]. In this respect, 3D NAND technologies utilizing vertically stacked memory cells, to increase bit density, were more vulnerable to stress issues [5]–[7]. Specifically, the increased metal gate volume greatly influences the residual stress in the device by contributing to wafer bending, which therefore degrades the uniform depth of focus (DOF) required in the lithography process [1], [6], [7]. In additions, residual stress also enhances the non-uniformity in physical parameters, which is one of the causes of deterioration of device performance and reliability [4], [8]. Therefore, appropriate control of residual stress development through process condition control or structure optimization is necessary to obtain better cell characteristics. With respect to these issues, only a few studies have been undertaken.

In this work, we investigated the development of residual stress as a function of processing condition. The residual stress values were extracted using a wafer curvature method. The metal-oxide-nitride-oxide-semiconductor (MONOS) capacitor was chosen for measuring electrical properties. The memory window, gate leakage, and interface state were checked, which verified the effects of residual stress on device characteristics. From there, we provided a method based on process conditions for minimizing the influence of residual stresses on cell characteristics.

II. EXPERIMENTAL

The process steps to produce the MONOS structure are shown in Fig. 1. A two-inch-diameter p-type (100) silicon wafer was prepared as a substrate, and a 5-nm-thick tunneling oxide was grown by thermal dry oxidation at 900 °C. Then, a 6-nm-thick silicon nitride trap layer was formed by low-pressure chemical vapor deposition (LPCVD) at 800 °C, followed by a 13-nm-thick LPCVD blocking oxide at 700 °C. Measurement of the deposited film thickness and wafer bending were checked with an ellipsometer (UVISEL Plus; Horiba, Longjumeau, France) and stylus surface profiler (Surfcorder ET200; Kosaka Laboratory Ltd., Tokyo, Japan), respectively. The tungsten film was formed in an ultra-high vacuum sputter system, with an operation vacuum level of 1×10^{-5} Pa and a 100 W RF power source. The substrate temperature was kept constant at room temperature, and Ar was used as the working gas. Meanwhile, to minimize the effects of thermal and mechanical loads on the etching process required for gate formation, metal mask patterning was performed, and the post-annealing was omitted. Through this process, we enhanced the accuracy of our analysis, excluding other causes that affect wafer bending. For evaluation of effect of stress, the main cell characteristics, including capacitance-voltage (CV) and current-voltage (IV) tests was conducted using a Keithley 4200-SCS semiconductor parameter analyzer (Keithley Instruments Inc., Cleveland, Oh, USA) and a HP 4284 LCR meter.

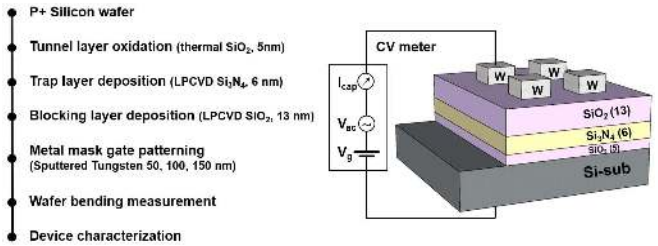

FIGURE 1. Key process steps and conditions for fabricating the MONOS device with varying gate thickness.

III. RESULTS AND DISCUSSION

A. RESIDUAL STRESS EXTRACTION

When an external force over the critical point is applied to the device due to thermal or mechanical factors, exerted force remains as a residual stress and causes irreversible deformation [9]. At the wafer level, the stress generated during the thin film deposition process leads to structural deformation, known as warpage, which can be divided into tension (positive sign) and compression (negative sign) depending on the deformed shape. The film under tension will try to contract, and in response, the substrate is deformed into a concave shape. If the film has compression force, the film will try to expand, and convex shape was occurred [9], [10]. Such deformation (residual stress) can be determined numerically by the Stoney equation, which is expressed as a function of wafer curvature and elastic parameters. The wafer curvature before and after deposition was measured. Then, the value of residual stress was calculated using the Stoney formula as follows:

$$\sigma_f = \frac{E_s}{6(1-\nu_s)} \cdot \frac{d_s^2}{d_f} \cdot \left(\frac{1}{R_{post}} - \frac{1}{R_{pre}}\right), \tag{1}$$

where σ_f is the total residual stress in n stacked films, E_s and ν_s are the Young's modulus and Poisson ratio of the substrate, respectively, d_s and d_f are the substrate thickness and film thickness (assuming $d_f << d_s$), respectively, and R_{pre} and R_{post} are the radii of curvature of the substrate before and after deposition, respectively [9]. This Stoney equation can be applied to a single thin film. In a multi-layer such as oxide/nitride/oxide (O/N/O) dielectric, the superposition principle form of the Stoney equation can be used. The total residual stress in the n-stacked multi-layer was:

$$\sigma_{total} = \frac{E_s d_s^2}{6(1-\nu_s)} \cdot \frac{1}{\sum_{i=1}^{n} d_{fi}} \cdot \sum_{i=1}^{n}\left(\frac{1}{R_{i,post}} - \frac{1}{R_{i,pre}}\right). \tag{2}$$

We calculated the value of residual stress of a single thin film and a multi-layer structure from these equations, and the detailed elastic parameters used in this study can be found in Table 1.

TABLE 1. Mechanical parameters for stress analysis.

Material	Young's modulus [GPa]	Poisson ratio
Silicon (100)	130	0.28
Silicon Oxide	70	0.2
Silicon Nitride	270	0.27
Tungsten	410	0.28

GPa = giga Pascal

B. STRESS WITH VARIABLE AR PRESSURE

It is known that metal film with its large elastic modulus can be severely affected to mechanical stress, and that the stress properties may change depending on process conditions such as method of growth, temperature, and working gas conditions [11], [12].

Since the stress control is possible by changing the process conditions, it is necessary to evaluate the stress pattern according to the effect of tungsten volume in both stress conditions (tensile, compressive) for comprehensive analysis. Therefore, we checked the tensile and compressive stress conditions through the changing of working gas pressure, and then investigated the effect of tungsten volume on stress and cell characteristics under both stress conditions.

First, we calculated the residual stress of a tungsten thin film on a bare wafer to assess the properties of tungsten stress under different working gas pressures. The deposition thickness of the tungsten film was selected to be 100 nm, and the Ar pressure was varied from 0.5 to 5 Pa. Fig. 2(a) shows the wafer bow profiles utilized for the calculation of residual stresses, and the values of the residual stresses extracted from the Stoney formula can be found in Fig. 2(b). The

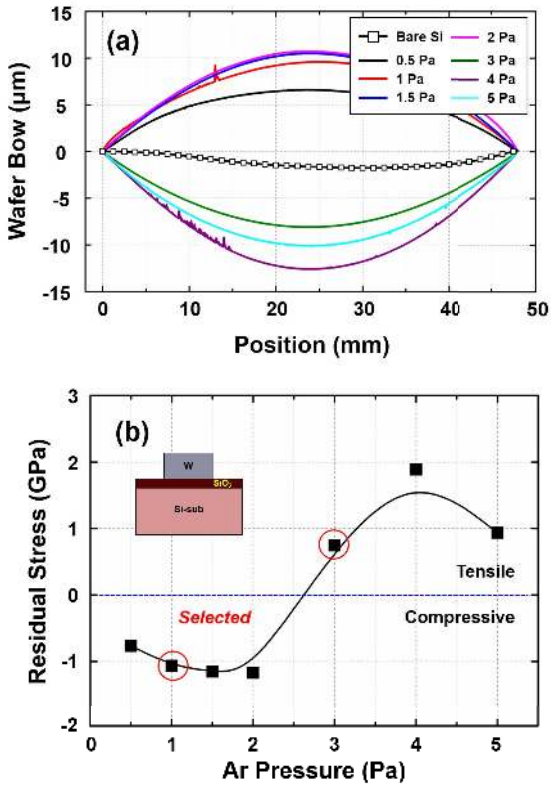

FIGURE 2. **(a) Wafer bow profile for bare Si and tungsten thin film under different Ar pressure (0.5 ~ 5 Pa) conditions, and (b) the value of residual stress calculated from the Stoney equation. The 1 and 3 Pa Ar pressure conditions were selected as a representative condition values for each stress polarity.**

wafer bending occurs from the tungsten process draw the convex (compressive) shape in lower Ar pressure conditions, then it becomes concave (tensile) shape as the Ar pressure increases. This residual stress distribution indicates the same tendency as in previous reports and was due to a difference in momentum based on the collision probability between target atom (W) and gas molecules (Ar) [12], [13]. Utilizing this distribution, we analyzed the residual stress as a function of the change in tungsten volume under both tensile and compressive stresses, respectively. Here, 1 and 3 Pa conditions were selected as the representative values of stress polarity, and 50, 100, and 200 nm thick tungsten films were deposited with MONOS structure, as shown in Fig. 3. As deposition thickness increased, residual stress gradually increased for both tensile and compressive conditions, though the compressive stress variation with thickness was larger. Generally, the stress reached the plastic regions, the film proceeds the relaxation step through the cracking (tensile) or bucking (compressive), and maintains the maximum value of stress [9]. Thus, a distinctly different value of residual stress in 200 nm thick conditions can be regarded as the plastic point difference according to the stress polarity. Consequently, the residual stress induced on a substrate increased as the deposited film volume increased regardless of stress polarity.

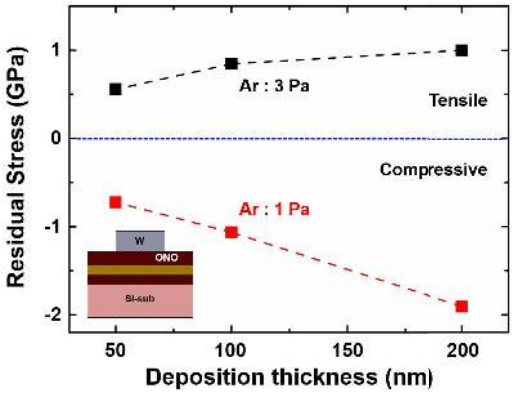

FIGURE 3. **Residual stress for MONOS capacitor under different Ar pressures (1, 3 Pa) and tungsten deposition thickness (50, 100, 200 nm) conditions.**

C. RELATIONSHIP BETWEEN STRESS AND INTERFACE STATE

To evaluate the effect of residual stress on cell characteristics, it is necessary to consider the effect of mechanical stress on the silicon/silicon-oxide (Si/SiO_2) interface state. Mechanical stress influences silicon-hydrogen bonding at the Si/SiO_2 interface, which changes the interface state. Normally, silicon is passivated by hydrogen molecules, which maintain a stable state. However, mechanical stress during fabrication breaks the silicon-hydrogen bonds, resulting in an unstable condition involving hydrogen desorption from the silicon molecule. Thus, dangling bonds formed where the hydrogen was removed, resulting in a trap site [14]. Finally, the interface traps increased, increasing the interface trap density (D_{it}) at the Si/SiO_2 interface. The effect of mechanical stress on Si-H bonding has already been studied with P_{b0}, P_{b1}, and Dimer models, which considered degradation of the interface state and reliability [15], [16]. This phenomenon also occurs irrespective of the stress characteristics and the impact of them is known to be stronger under compressive stress conditions [16]. Thus, assessing the Si/SiO_2 interface could be an effective way to confirm the effect of residual stress on cell characteristics. We measured the value of D_{it} using a conductance method to assess the interface state for different stress conditions. The conductance method is considered to be an effective method for determining D_{it}, as it measures equivalent parallel conductance as a function of gate bias and frequency [17]. Fig. 4 shows a box plot of D_{it} at the midgap of 10 samples obtained using the conductance method under different stress conditions. The value of D_{it} of the 50-nm-thick samples was less affected by deposition volume and had the smallest value among the other samples. The D_{it} values of the other samples gradually increased as deposition thickness increased. This tendency was observed irrespective of the stress polarity. At maximum conditions, the average D_{it} values were 2.15×10^{12} and 3.07×10^{12} $eV^{-1}cm^{-2}$ for tensile and compressive stresses, respectively. In other words, the value of D_{it} is significantly changed by the value

of stress that arise from tungsten volume. In particular, the absolute value of stress has affected the value of D_{it} regardless of polarity and is supported by the results under both side conditions produced by Ar pressure control.

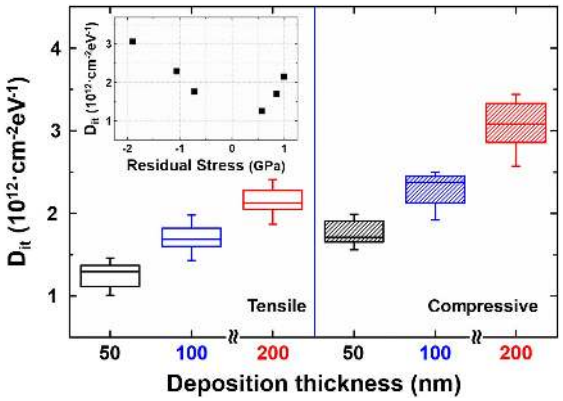

FIGURE 4. Interface trap densities of MONOS capacitor under different Ar pressure and tungsten deposition thickness conditions. Inset figure represents the interface trap densities as a function of residual stress under each condition.

D. INFLUENCE ON RELIABILITY

Checking the leakage characteristics has been considered as an effective way to evaluate the reliability of semiconductor devices. In metal-oxide-semiconductor (MOS) device, the increasing of gate leakage current represents the degradation of the dielectric quality, which can be a numerical parameter to indicate the device reliability. To confirm the correlation between cell reliability and D_{it} caused by the residual stress, we measured the gate leakage current in each condition. Fig. 5 shows the leakage current density versus gate voltage (J-V) curves in a sample for various tensile and compressive stress conditions. The J-V curve was obtained by sweeping the voltage from 0 to 20 V at a 0.1 V sweep rate. As the applied electric field becomes stronger, leakage current density increases, and saturation occurs above a certain voltage. We can determine that cells with high value of leakage current density and lower saturation points are more degraded from a reliability perspective. Meanwhile, the value of leakage current densities and saturation points exhibited significant differences depending on the stress conditions. The 50-nm-thick sample with tensile stress had the lowest D_{it} value with an 18 V saturation point and a 7.51×10^{-5} A/cm^2 leakage current density. However, the 200-nm-thick compressive sample with a high value of D_{it} showed severely degraded values of 6 V and 7.78×10^{-4} A/cm^2, respectively. In other words, the saturation point and leakage current density (which represents cell reliability) deteriorated as D_{it} increased, and the distortion became stronger under compressive stress conditions compared to tensile. It is known that as the high tensile stress applied to the oxide in the MOS structure, then the bandgap narrowing, and reduction of effective thickness deteriorated the breakdown characteristics [18], [19]. However, the reason for this difference in leakage characteristics for various stress conditions in our experiments can be considered the generation of current at the interface (J_{sg}) and trap-assisted tunneling (TAT) [16], [20]. The current model describing the transfer mechanism in the dielectric film, J_{sg}, is the sum of electrons and holes transported through surface states, which was proportionally related to D_{it}. That's why the leakage characteristics degraded under high D_{it} conditions. In addition, TAT through a dielectric was one of the other factors that deteriorated the reliability. Thus, the tendency of D_{it} in Fig. 4 and that of the leakage characteristics in Fig. 5 were the same, and the control of residual stress and D_{it} should be ensured to preserve dielectric film quality.

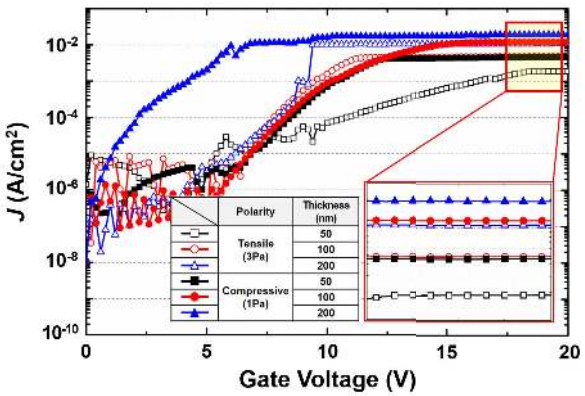

FIGURE 5. The leakage current density versus gate voltage curves of the MONOS capacitor under each condition. Inset figure represents the leakage current densities at high gate voltage region.

E. IMPACT OF STRESS ON MEMORY CHARACTERISTICS

We performed CV tests to investigate the impact of stress and the interface traps generated by stress on the memory characteristics of MONOS devices. Fig. 6(a) and 6(b) display the normalized CV hysteresis for the MONOS capacitor; the measurement was performed by bidirectionally sweeping from −18 and 18V and back. The AC signal frequency and voltage sweep rate were set to 1 MHz and 0.2 V·s^{-1}, respectively. All CV curves showed the typical accumulation-deletion-inversion properties, and the shift in flat band (ΔV_{FB}) was featured due to the trapped charge in the silicon nitride. However, our samples displayed low window memory in spite of the wide voltage sweep range. This phenomenon can be explained by the absence of post-annealing, which is effective method to eliminate the local traps and defects in dielectric layers. In addition, the difference in V_{FB} according to stress conditions arise from difference in metal work function which may vary with chamber conditions [21]. Despite these unexpected experimental obstacles, the variation of cell characteristics with stress was confirmed. Tensile and compressive stresses showed similar effects in the CV measurement. The value of the memory window originating from the shift in

V_{FB} was slightly larger for small stress (lower tungsten volume) conditions regardless of stress polarity, and their values gradually decreased as the residual stress increased. Considering that difference, the average memory windows of 10 samples were measured as indicated in the inset table of Fig. 6(a), and (b). As mentioned above, the highest value of ΔV_{FB} was observed in the lower stress conditions, and their values gradually decreased as the residual stress increased for tensile or compressive stress. This shows that the memory function is considerably deteriorated under high stress conditions, and is proportional to the absolute values, regardless of stress polarity.

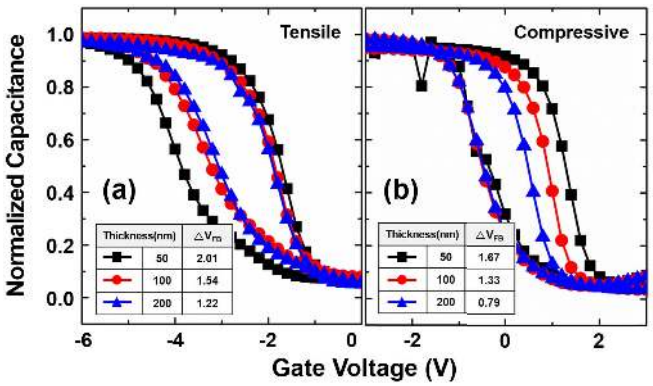

FIGURE 6. The normalized capacitance-voltage curves of MONOS capacitor under (a) tensile and (b) compressive stress condition. Inset table shows the memory window under each condition.

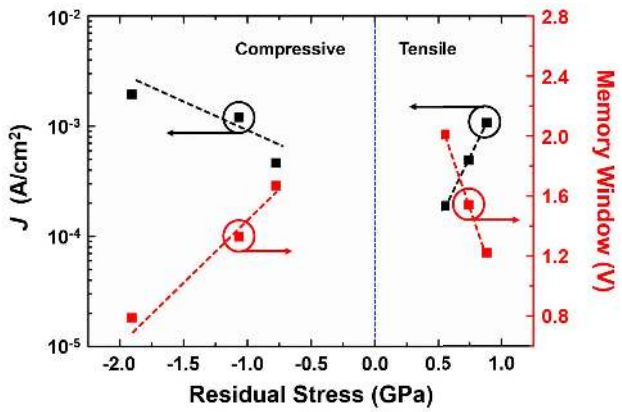

FIGURE 7. Variation of electrical properties (leakage current density and memory window) as a function of residual stress.

F. SUMMARY

Fig. 7 presents the electrical properties, including memory windows and leakage current densities, as a function of residual stress for each condition. The blue line implies the neutral value as the starting point, the left side represents the compressive stress, and the right side represents the tensile stress condition. As the distance from the blue line (stress-free) increases in the tensile or compressive directions, the deterioration of cell characteristics is intensified, observed as the degradation of memory window and leakage characteristics. This result proves that deterioration of cell characteristics can be prevented by minimizing residual stresses.

In addition, band diagram expression during charge trap operation can be helpful for understanding the experimental results, as shown in Figs. 8(a), (b). The band diagram with high D_{it} (Fig. 8(a)) illustrates a condition with a thick tungsten gate, whereas that with a low D_{it} (Fig. 8(b)) represented the opposite condition. When the applied gate bias was high enough to cause Fowler-Nordheim (FN) tunneling, the charge carrier was trapped by a silicon nitride trap level. However, for a high cell Dit induced by stress, the electrons in the silicon substrate were unexpectedly caught at the interface trap site. The number of carriers reaching the trap layer was reduced, resulting in a drop in trapped charge density at the same operating conditions. In addition, it is expected that the silicon conduction band split into Δ_2 and Δ_4 valleys due to large stress will impart the reduction of conduction band energy and bandgap narrowing, resulting in the decreasing of tunneling efficiency from silicon substrate to silicon nitride trap layer [19]. Therefore, trapped charge density was reduced in high residual stress conditions, which was verified by the CV test, as can be seen in Figs. 6(a) and 6(b).

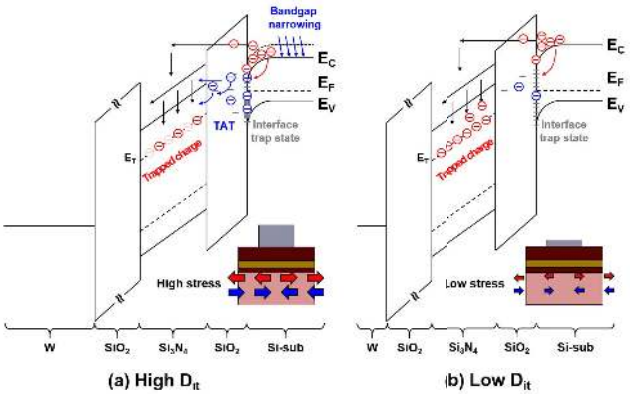

FIGURE 8. MONOS structure energy band diagram for charge trap operation with (a) high- and (b) low-stress conditions.

IV. CONCLUSION

In this paper, the effect of residual stress on the cell characteristics was investigated using a MONOS devices. We experimentally revealed that residual stress increased as the thickness of the tungsten film increases, regardless of stress property. From analyzing the Si/SiO_2 interface, it is confirmed that residual stress degrade the cell characteristics occurred as a result of increased interface trap density. Based on these results, we concluded that residual stress is a critical factor in cell characteristic deterioration, and the absolute value of residual stress is significantly affected by these issues regardless of stress polarity. Our results highlight the importance of stress control through physical parameter regulation to prevent the degradation of cell characteristics in memory device.

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