The Effect of Varactor Nonlinearity on the Phase Noise of Completely Integrated VCOs

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***Abstract*—This work discusses variations in phase noise over the tuning range of a completely integrated 1.9-GHz differential voltage-controlled oscillator (VCO) fabricated in a 0.5-μm bipolar process with 25-GHz f_t. The design had a phase noise of −103 dBc/Hz at 100 kHz offset at the top of the tuning range, but the noise performance degraded to −96 dBc/Hz at 100 kHz at the bottom of the tuning range. It was determined that nonlinearities of the on-chip varactors, which led to excessively high VCO gain at the bottom of the tuning range, were primarily responsible for this degradation in performance. The VCO has a power output of −5 dBm per side. Calculations predict phase noise with only a small error and provide design insight for minimizing this effect. The oscillator core drew 6.4 mA and the output buffer circuitry drew 6 mA, both from a 3.3-V supply.**

***Index Terms*—Bipolar transistor, circuit theory and design, fully integrated VCO, integrated inductors, phase noise, varactors.**

I. Introduction

HE INCREASING demand for portable communications equipment has driven research to produce transceivers at lower cost. This has led to an intense interest in integrating as many components as possible. One high-speed component that has been particularly hard to integrate is the voltage-controlled oscillator (VCO). This is largely due to the poor quality of on-chip passive components in silicon integrated circuit technologies, namely the low quality factor Q of on-chip inductors and the poor linearity of on-chip varactors. In this work, we present a design methodology for a high-power completely integrated Colpitts oscillator. Optimum design of this circuit for best phase-noise performance will be discussed. The effect of poor varactor linearity on phase-noise performance over the complete tuning range will be discussed, an issue not commonly addressed. We will show that with the use of simple theory, this effect can be predicted qualitatively and quantitatively with only a small error.

II. Design Considerations

In this section, the design of a differential Colpitts common-base VCO for low phase-noise performance is discussed. The circuit is shown in its simplest form in Fig. 1. Note that of the Colpitts topologies, either the common-base or the common-collector is suitable for integrated designs. The common-base was chosen because it is not as widely explored as the common-collector configuration [1]. As well, preliminary simulations showed it had performance equal to or marginally better than the common-collector circuit.

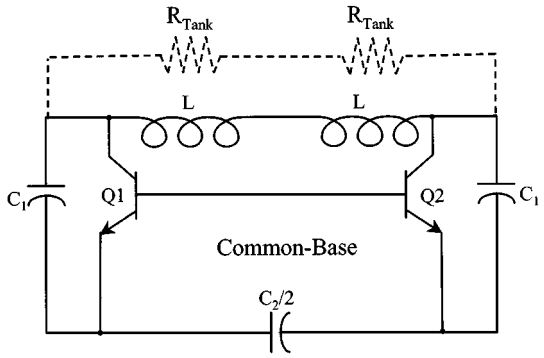

Fig. 1. Differential common-base Colpitts oscillator. Biasing not shown.

A. Frequency Tuning

The first task in designing an *LC* oscillator is to set the frequency of oscillation, and hence set the value of the total inductance and capacitance in the circuit. Assuming ideal transistors $Q1$ and $Q2$ the frequency of oscillation is given by

$$\omega_{\rm osc} = \frac{1}{\sqrt{LC_{\rm tot}}} \tag{1}$$

where $C_{\rm tot}$ is the series combination of C_1 and C_2.

To get the unloaded Q as high as possible, as well as increase output swing, it is desirable to make the inductance as large as possible. This is because the losses in the inductor are usually much higher than the losses in the capacitors and because the parallel resistance of the inductor is proportional to the size of the inductor [see (2)]. However, it should be noted that in practice, large monolithic inductors suffer from limited Q. Therefore, in a given technology there will be an optimum size for the inductor.

B. Design of On-Chip Inductors

Inductors prove to be one of the most difficult passive circuit elements to implement on-chip. When they are made in Si technology they suffer from the presence of relatively high-resistance metals and lossy substrates, although much work is being done to improve this [2]–[6]. In order to achieve the best possible Q at the desired frequency, careful layout of the inductor with the help of an existing simulation tool [7], [8] is required.

Manuscript received December 17, 1999; revised February 13, 2000. This work was supported by the Natural Sciences and Engineering Research Council of Canada (NSERC) and MICRONET.

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Publisher Item Identifier S 0018-9200(00)05929-1.

The parallel resistance that the inductor presents to the tank is given by

$$R_{\mathrm{Tank,\,L}} = Q_{\mathrm{ind}}\omega_{\mathrm{osc}}L = Q_{\mathrm{ind}}\sqrt{\frac{L}{C_{\mathrm{tot}}}} \tag{2}$$

The goal of any inductor layout is to design a spiral inductor of specified inductance, and optimize Q for best performance at the frequency of interest. In order to achieve this, careful layout of the structure is required. The resistance of the metal lines causes the inductor to have a high series resistance limiting its performance at low frequencies, while capacitive coupling to the lossy silicon substrate causes the inductor's effective resistance to rise even more at higher frequencies [9], [10]. Large coupling between the inductor and the substrate also causes the structures to have low self-resonance frequencies, placing restrictions on the size of the device that can be built. In order to reduce the series resistance, the line widths should be large; therefore, to obtain a given value of inductance the structure must occupy a greater area, increasing substrate loss. Narrower metal lines mean less substrate loss, but more series resistance. The designer must carefully balance these factors to get the best possible performance at the desired frequency.

Traditionally, on-chip inductors have been square. This is because these have been easier to model than more complicated geometries. A square geometry is by no means optimal however. The presence of the 90° bends adds unnecessary resistance to the structure [11]. Intuitively it is easy to see that as the structure is made more circular the performance will improve. Recent work has also shown that the use of differential inductors can reduce substrate losses and lead to higher Q factors in differential applications [12], [13]. As well, the use of a patterned ground shield underneath the inductor can also lead to improved performance [2]. However, few simulators other than full 3-D electromagnetic simulators are able to predict the performance of such structures so the designer is often left with experimentation as the only possible design approach. For these reasons the inductors used in fabricating the oscillator were made with a square geometry.

In this work a version of GEMCAP [7] was used to simulate inductor performance. Unfortunately, this software could only model square geometries. Despite the fact that the version of the software used did not handle the skin effect or model the underpass of the structure, the values of inductance were simulated very accurately. It also predicted the Q with reliable trends although it tended to be slightly optimistic.

C. Capacitor Ratios

In order to achieve good performance, the use of capacitors is necessary to transform r_e (the dynamic emitter resistance) of transistors $Q1$ and $Q2$ (see Fig. 1) to a higher value. The impedance transformation effectively prevents this typically low impedance from reducing the Q of the oscillator's *LC* tank. The impedance transformation is given by [14]:

$$R_{\mathrm{Tank,\,r_c}} = \left(1+\frac{C_2}{C_1}\right)^2 r_e \tag{3}$$

where $R_{\mathrm{Tank,re}}$ represents the parallel resistance across the tank due to r_e. Therefore, in order to get the maximum effect of the impedance transformer, it is necessary to make C_2 large and C_1 small. However, if this ratio is made too large then the gain around the loop will drop below one. In addition, the larger this ratio is made the more current must be driven through the transistors to achieve a given output power. This in turn leads to larger noise sources in the tank, thus degrading phase noise. The gain around the loop in the oscillator is given by

$$G = \frac{C_1}{C_1+C_2}g_m R_{\mathrm{Tank}} = \frac{g_m R_{\mathrm{Tank}}}{1+\dfrac{C_2}{C_1}} \tag{4}$$

where R_{Tank} is approximately equal to the parallel combination of $R_{\mathrm{Tank,L}}$ and $R_{\mathrm{Tank,re}}$. Since the loop gain given in (4) must be greater than one for oscillations to begin, this expression can be solved to give a crude estimate for the minimum bias current required to allow oscillations to start.

$$I_C > V_T\left(1+\frac{C_2}{C_1}\right)\frac{1}{R_{\mathrm{Tank}}} \tag{5}$$

where V_T is the thermal voltage. In the limit when C_1 gets very large this expression simplifies to

$$I_C > \frac{V_T}{R_{\mathrm{Tank}}}. \tag{6}$$

This corresponds to the case where the minimum current is required for start-up of the oscillator. However, this also corresponds to the case where the transistor loss will have the most impact on the Q of the tank and will lead to higher phase noise as shown above.

D. Design and Placement of Varactors

Diodes in the technology used for this work [15] are usually realized using the base–collector junction, as shown in Fig. 2. However, when using this junction there is also a parasitic diode between the collector and the substrate. Observe that the tiedown is typically connected to ground, hence the anode of the parasitic diode is normally grounded. The base–collector junction had a Q that varied from 22.9 to 33.5 with a properly optimized layout as shown in Fig. 2. However, the parasitic junction inherently has a low Q due to the low doping of the substrate. This makes it desirable to remove it from the circuit. Placing two varactors C_{var} in the oscillator as shown in Fig. 3 effectively ac-grounds both sides of the parasitic diodes and removes them from the differential circuit. Note that in this circuit the anode of the varactors is at approximately 1-V dc. Therefore, to prevent forward-biasing them, the control-voltage tuning range will be approximately from 1 to 3.3-V dc. The resistor R_{tune} prevents decoupling both sides of the oscillator. It also provides protection from accidentally forward-biasing the varactors which could otherwise cause large currents to flow.

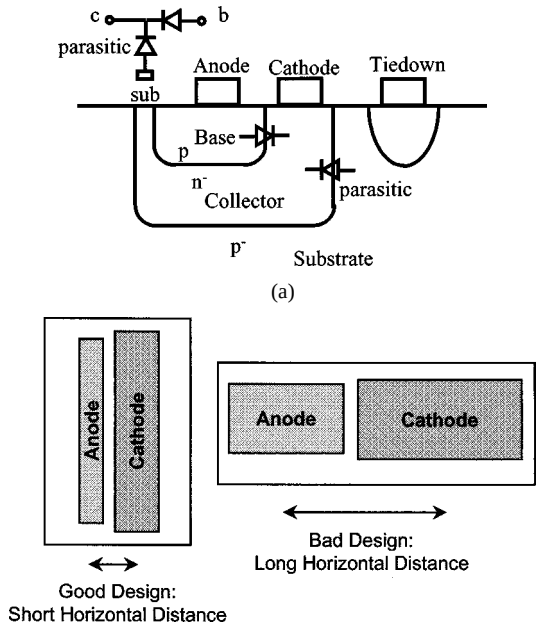

Fig. 2. Integrated varactor with parasitic diode. (a) Cross-sectional view of the diode. (b) Example layout for the varactor.

Unfortunately in bipolar processes the base–collector junction is usually made with constant doping. This leads to a nonlinear C–V characteristic that can be approximated by the following [16]:

$$C(V) = C_o\left(1 - \frac{V}{\psi_o}\right)^{-1/2} \tag{7}$$

where C_o is the value of the capacitance of the junction with zero volts across it, and ψ_o is the built-in potential of the junction. If available, the use of a junction with a linearly graded doping profile can be shown to lead to increased linearity. The formula for its C–V characteristic is

$$C(V) = C_o\left(1 - \frac{V}{\psi_o}\right)^{-1/3}. \tag{8}$$

In the limit for large applied reverse bias the varactors can suffer from collector–base punch-through. This will cause the capacitance to become almost constant. At this point, the VCO frequency will cease to vary with changes in the voltage on the control line. As will be shown in Section IV, this occurs in the region of low phase noise.

Equations (1) and (7) could be used to find an expression for the frequency of oscillation as a function of control voltage. However, it is more useful to find such a relationship through simulation and measurement. Nevertheless it should be noted that the shape of the C–V curve described by (7) is nonlinear and will lead to a nonconstant value of $K_{\rm VCO}$ for the oscillator.

E. Addition of Emitter Degeneration

Fig. 3 shows the completed oscillator circuit. The current sources are represented with symbols for simplicity. If sufficient current is driven through the transistors $Q1$ and $Q2$ in the circuit depicted in Fig. 3 such that reasonable output power is achieved, the value of r_e is quite small even after it has been transformed

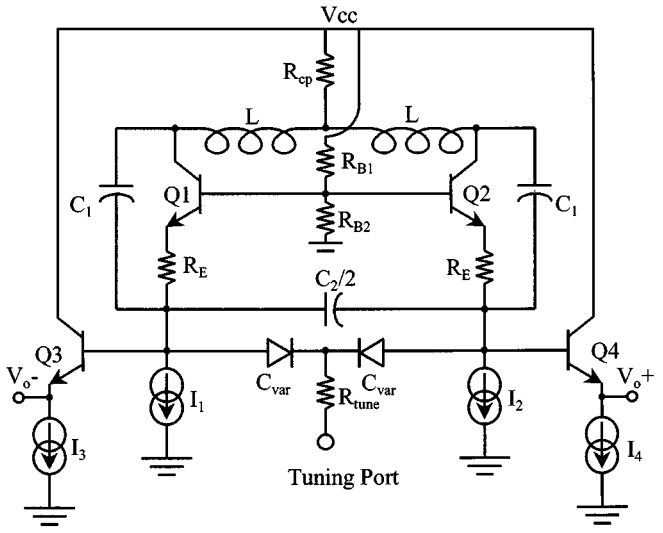

Fig. 3. Final common-base design including output buffers and biasing.

to the collector. If steps are not taken, this resistance will limit the performance of the design. In order to increase the Q of the tank without sacrificing output power, emitter degeneration R_E is added to the circuit. Degeneration will also further increase the linearity of the transistor amplifiers at the cost of adding some additional noise. This allows the signal levels to increase more before the transistor nonlinearity causes saturation. Care must be taken as the addition of excessive degeneration results in less negative resistance and oscillations will not start. Thus making this resistor too large leads to low output power, and therefore high phase noise. Making R_E small also leads to excessive nonlinear mixing of noise around the carrier that further increases phase noise. Therefore, either simulation or careful analysis must be used to set this value. Simulations showed that 20 Ω was close to optimal.

F. Addition of Output Buffers

The placement of a 50-Ω load either directly across the tank or at the emitter of these circuits such as when testing with a spectrum analyzer would significantly reduce the Q of the circuit. For this reason, output buffers have been added to the circuit. These buffers are emitter followers $Q3$ and $Q4$ with high input impedance and they transform the 50-Ω load into a larger impedance. They were placed at the emitter instead of at the collector in order to take advantage of the impedance transformation provided by the capacitors (C_1, C_2, and $C_{\rm var}$). This buffer also makes the circuit less sensitive to load pull when driving an active load such as the input to a mixer, and gives increased output power since it can drive 50 Ω without affecting signal amplitude in the oscillator core.

G. Quality Factor (Q) of an Oscillator

The Q of an *LC* resonator is a figure of merit used for *LC* tanks and oscillators. It is extremely important because the phase noise produced by the oscillator is a strong function of the Q of the tank. It can be shown that [14]

$$Q = \omega_o R_{\rm Tank} C_{\rm tot} = R_{\rm Tank}\sqrt{\frac{C_{\rm tot}}{L}} \tag{9}$$

where $R_{\rm Tank}$ is the total equivalent resistance in parallel with the tank, $C_{\rm tot}$ is the total capacitance of the tank, and L is the inductance. For the oscillator in Fig. 3, $R_{\rm Tank}$ is composed mostly of the parallel resistance of the on-chip inductor (due to its limited Q), and of the transformed dynamic emitter resistance in series with R_E. Thus, for this circuit the resistance in parallel with the tank including the effect of R_E can be approximated by

$$\frac{1}{R_{\rm Tank}} = \frac{1}{Q_{\rm ind}\omega_{\rm osc}L} + \frac{1}{\left((r_e + R_E)\left(1 + \dfrac{C_2 + C_{\rm var}}{C_1}\right)^2\right)}. \tag{10}$$

Some numeric values using this formula will be given in Section V.

III. Output Power of the Oscillator

An oscillator relies on the nonlinearity in the transistor amplifier to limit the amplitude of the oscillation. As the voltage swings get larger the transistor starts to behave in a nonlinear manner which causes the loop gain to be reduced until it is exactly unity. At this point the oscillation amplitude stabilizes. If the amplitude of the oscillation is quite small due to a small-signal loop gain (not much more than unity) then transistor cut-off will probably be enough to cause oscillations to stabilize. As the gain is increased and oscillations become more vigorous the transistor will alternate between cut-off and saturation. In this state, the current through the transistor will appear as narrow pulses coinciding with the top of the voltage swing. In this region of operation, a formula is given by [17] to predict the amplitude, as follows:

$$V_{\rm Tank} \approx 2I_{\rm Bias}\left(1 - \frac{C_1}{C_1 + C_2 + C_{\rm var}}\right)(R_{\rm Tank,\,L}//R_{\rm load}) \tag{11}$$

where $R_{\rm load}$ is the resistance presented to the tank by the load. Note that this formula will be slightly less accurate for designs that use degeneration because that will tend to widen the current pulses. For the oscillator in this paper this formula would lead to an output voltage of

$$V_{\rm out} \approx 2A_f I_{\rm Bias}\left(\frac{C_1}{C_1 + C_2 + C_{\rm var}}\right)\left(1 - \frac{C_1}{C_1 + C_2 + C_{\rm var}}\right) \cdot (R_{\rm Tank,\,L}//R_{\rm load}) \tag{12}$$

where A_f is the loss due to the followers. However, it should be noted that oscillations would not grow forever with increasing bias current. Eventually the voltage will reach a hard limit set by one of the supply rails. Further increasing the current will result in a clipped output voltage waveform such that the voltage amplitude of the fundamental frequency is the first harmonic of a square wave. In this region, the formula will become increasingly inaccurate.

IV. Phase Noise in VCOs

When VCO phase-noise performance is reported, it is typically measured at only one point in the tuning range [1]–[21]. However, the phase noise of on-chip designs is not necessarily constant over the tuning range [22]. Unfortunately, on-chip varactors have a nonlinear C–V curve, and this can make the phase noise over the tuning range nonuniform. Any noise on the control line can lead to additional phase noise as shown in [14], however, any noise generated by the VCO at the varactor terminals will also modulate the carrier and create additional phase noise. This term can be added to the well known Leeson's formula [23] to take this additional noise mechanism into account.

$$L(f_m, K_{\rm VCO}) = 10\log\left(\left(\frac{f_o}{2Qf_m}\right)^2\left[\frac{FkT}{2P_s}\left(1 + \frac{f_c}{f_m}\right)\right] + \frac{1}{2}\left(\frac{K_{\rm VCO}V_m}{2f_m}\right)^2\right) \tag{13}$$

where

$L(f_m,K_{\rm VCO})$	phase noise in dBc/Hz;
f_o	frequency of oscillation in Hz;
f_m	frequency offset from the carrier in Hz;
F	noise figure of the transistor amplifier;
k	Boltzmann's constant in J/K;
T	temperature in K;
P_s	RF power produced by the oscillator in W;
f_c	flicker noise corner frequency in Hz;
$K_{\rm VCO}$	gain of the VCO in Hz/V;
V_m	total amplitude of all low frequency noise sources in V/$\sqrt{}$Hz.

Since the varactor is nonlinear, $K_{\rm VCO}$ varies over the tuning range. Therefore, in some circumstances, the phase noise in the oscillator can be completely determined by the low-frequency noise. At the bottom of the tuning range where the VCO has a high gain, the low-frequency noise dominates. Conversely at the top of the tuning range where the gain is small, the Leeson's-style noise dominates and determines the phase noise of the oscillator. Thus, the designer must be very careful to minimize these low-frequency noise sources as well as maximizing the Q of the oscillator tank. Note that the varactor can be forward-biased at the top and bottom of its signal swing, but this excess phase noise has nothing to do with forward-biasing the varactor (very little phase noise is generated there regardless) or reducing the varactor's high-frequency Q due to forward-biasing. This same variation can be demonstrated in simulation using an ideal voltage-controlled capacitor if the C–V characteristics match those of a real varactor. Note also that the excess gain term sometimes included in Leeson's formula has been ignored. This term, used to model nonlinearities that can contribute to the noise through nonlinear mixing of higher frequency noise around the carrier, is not significant if the oscillator is designed to have very little excess gain, as is the case here.

V. Calculation of Phase Noise

From the preceding discussion it is easy to see how one might go about predicting the phase noise of the VCO. The Q of the oscillator can be calculated using (9) assuming $R_{\rm Tank}$ can be approximated by (10). For this VCO the bias current through $Q1$ and $Q2$ is 3.2 mA, resulting in an r_e of 7.8 Ω and R_E has

TABLE I
CALCULATION OF R_{Tank}

Reverse Bias of the Varactor	C_{var}	$\left(1+\frac{C_2+C_{var}}{C_1}\right)^2$	$R_{Tank,re+RE}$	R_{Tank}	Tank Q
0 Volts	2.9pF	6.91	192.1Ω	99.6Ω	2.68
1Volt	2.1pF	5.76	160.1Ω	90.2Ω	2.35
2 Volts	1.9pF	5.49	152.6Ω	88.0Ω	2.27
3 Volts	1.8pF	5.35	148.7Ω	86.6Ω	2.22

been selected to be 20 Ω, C_1 is 3.5 pF and C_2 is 2.8 pF. Based on these values, the following table summarizes the effectively transformed emitter resistance seen at the tank ($R_{\mathrm{Tank,\,re+RE}}$) where the parasitics in $Q1$ and $Q2$ were neglected for simplicity. Also assuming a Q of 5.5 (see Fig. 5) for the 3-nH inductor ($R_{\mathrm{Tank,\,L}} = 207\,\Omega$ at 1.9 GHz), the total equivalent resistance is obtained using (10). From Table I, it is also easy to see that without R_E, the Q of the oscillator would be drastically reduced.

Note that accounting for the finite varactor Q will not change the results by any measurable amount. Even in the worst-case scenario, the varactor has a parallel resistance of 629 Ω which gets transformed (through the capacitor ratio) to 4.35 kΩ in parallel with the tank. Thus, varactor loss was ignored in this analysis.

Simulations using SPICE will give accurate predictions of the noise figure of the amplifier (we are making the assumption here that using the small-signal noise figure is an accurate method of calculating the transistors noise contribution to the tank) and output power of the circuit. Alternatively, the output power can be estimated from the formula in Section III. V_m can be calculated by summing the noise sources in transistors and resistors present at the terminals of the varactor. Note that this is the noise at f_m modulated to $f_o - f_m$ or $f_o + f_m$. Therefore in calculating the noise one can simplify the circuit knowing that the capacitors are all open circuits and the inductors are short circuits at these frequencies. In minimizing the noise present in the VCO, two things are of paramount importance. First, the current through the transistors must not be made larger than necessary for a given power level, and second, R_{tune} must be kept relatively small. Note that this resistor's purpose is to avoid decoupling both sides of the oscillator and prevent large currents from flowing in case the varactor is forward-biased, however, it does represent a noise source directly applied to the tuning port. If low-frequency noise starts to dominate in the design, it is recommended to reduce the ratio of $C_2 + C_{\mathrm{var}}$ to C_1 at the expense of reducing the Q of the tank in order to reduce the current and therefore reduce the noise at the varactor terminals. K_{VCO} can be predicted provided a model is available for the varactor. Such calculations resulted in the predicted values presented in the next section.

VI. RESULTS

Both the varactor and inductor were tested on-wafer as one-port devices. The collector side of the varactor (see Fig. 2) was grounded so that the parasitic diode was removed form the circuit and the effect of only the desired collector–base junction was measured. Fig. 4 shows the C–V curve for the structure. The varactor's capacitance is 2.9 pF for 0-V reverse bias and 1.8 pF for 3-V reverse bias. This gives a capacitor-tuning ratio of 1.6. The Q of the varactor (also shown in Fig. 4) was measured and was greater than 20 over the whole tuning range with this terminal grounded. Note that grounding the base and measuring the Q from the collector side of the junction will show a reduced Q for the two varactors in parallel, usually below five. This further illustrates the importance of the varactor placement in this circuit. The inductor was also measured on-wafer as a one-port test structure. Fig. 5 shows the measured inductor Q and inductance (which was about 5.5 at the frequencies of interest).

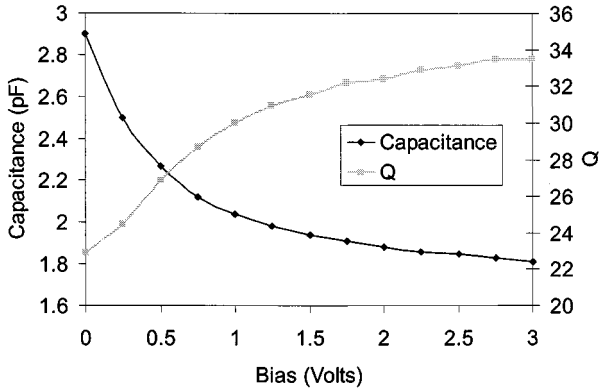

Fig. 4. Measured C–V curve and Q for the varactor used in the VCO.

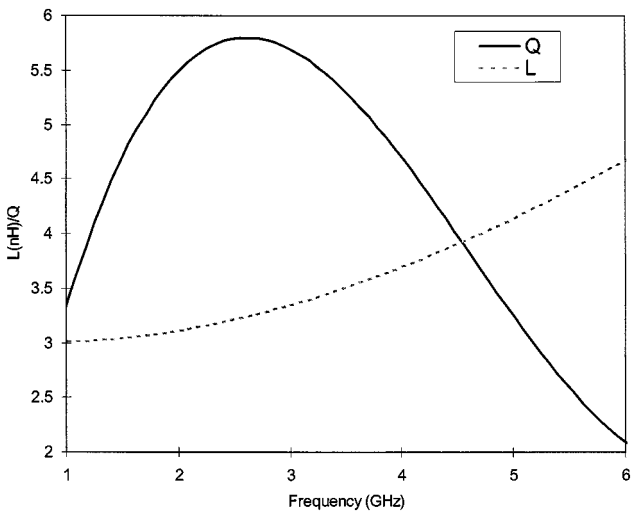

Fig. 5. Measured performance of a 3-nH spiral structure.

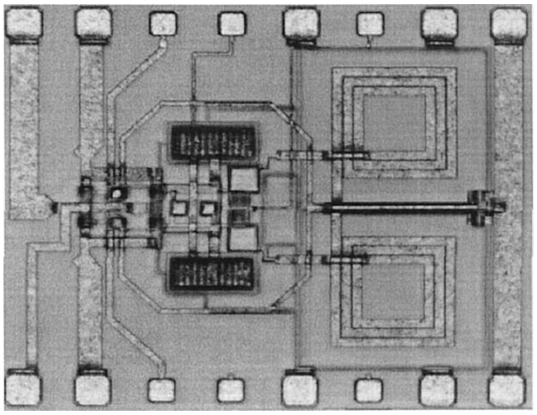

Fig. 6. Microphotograph of the VCO.

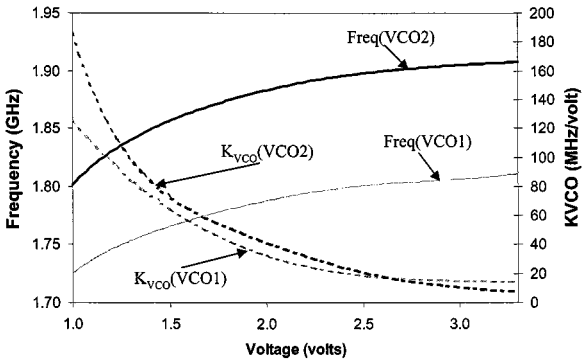

Fig. 7. Frequency versus tuning voltage characteristic for both VCO designs.

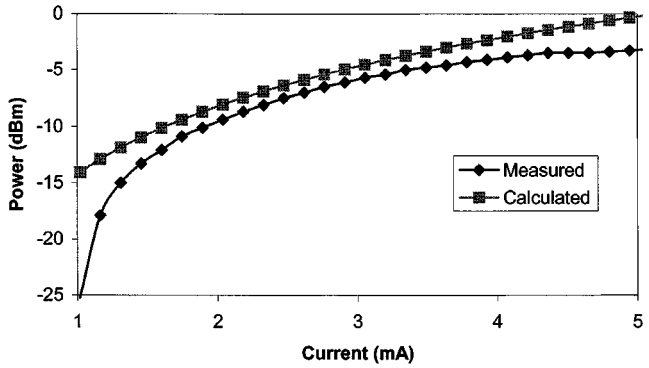

Fig. 8. Output power versus bias current for VCO2. (Both single-ended.)

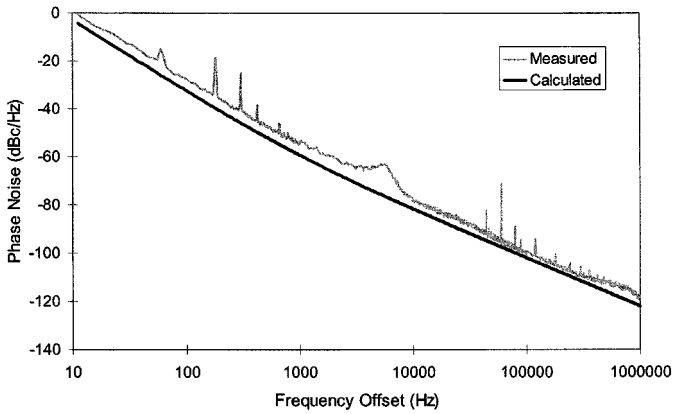

Fig. 9. Phase noise versus frequency offset at 1.9 GHz for VCO2.

A microphotograph of the VCO itself is shown in Fig. 6. The layout was made as symmetric as possible to ensure a true differential circuit. The VCO occupied a chip area of 1.1 mm $\times$ 0.8 mm. The inductors were placed apart from the rest of the circuit to ensure good performance, and a guard ring of substrate contacts was placed around them to prevent the VCO signal from traveling through the substrate. Two versions of the VCO were fabricated. The first version of the VCO had $R_{\rm tune} = 4\,{\rm k}\Omega$ and drew 5 mA through each of $Q1$ and $Q2$. The second version of the VCO was reworked to re-optimize device sizes to reduce the low-frequency noise and make the phase noise more uniform over the tuning range. This second design drew 3.2 mA through each of $Q1$ and $Q2$ and had $R_{\rm tune} = 50\,\Omega$. The capacitor ratio was reduced somewhat in this design to compensate for the reduced gain in the transistors so that the oscillator output power would not change. A third oscillator was fabricated, identical to the first design, but substituted fixed capacitors for the varactors for comparison.

The VCO was measured both by wafer probing and after packaging. It had a tuning range of 90 MHz for the first design and 100 MHz for the second design. All designs had a single-ended output power of -5 dBm at their nominal bias points. The oscillators were operated from a 3.3-V supply. Phase noise measured for both packaged and unpackaged parts differed by less than 3 dB. Plots of frequency versus tuning voltage for both versions of the VCO are shown in Fig. 7. Note that $K_{\rm VCO}$ decreases from over 100 MHz/V down to below 20 MHz/V over the tuning range for both designs. The output power of the second design was plotted relative to bias current and compared to estimates obtained with the formula presented earlier. Note that there is good agreement provided that the current is not too low or too high. These results are shown in Fig. 8. The phase noise versus frequency offset for the second version of the VCO at 1.9 GHz is shown in Fig. 9. This measurement was done at the top of the tuning range. The phase noise measurements agreed well with values predicted by (13), also shown in Fig. 9. The phase noise was measured under these conditions to be -103 dBc/Hz at 100 kHz offset. The oscillator with no tuning mechanism (without a varactor) was found to oscillate at 1.72 GHz. It was made identical to the first design with the fixed capacitors set to have the same capacitance as the varactors at the bottom of the tuning range. It had a phase noise of -105 dBc/Hz, further demonstrating the importance of the low frequency noise to this circuit.

A plot of phase noise versus tuning voltage for both versions of the oscillator is shown in Fig. 10. This clearly shows that the performance is not uniform over the tuning range. In fact it varies by as much as 10 dB in the first design. The second version of the VCO reduces the range to only 7 dB of variation and gives better overall performance. Calculations using (13) also predicted almost the same variation for both designs. Note that a VCO with constant gain and the same tuning range would have an almost constant phase noise that would rest between these two extremes. This very clearly demonstrates the effect of the varactor on the phase noise. There were of course some slight discrepancies between measured and calculated phase noise. It

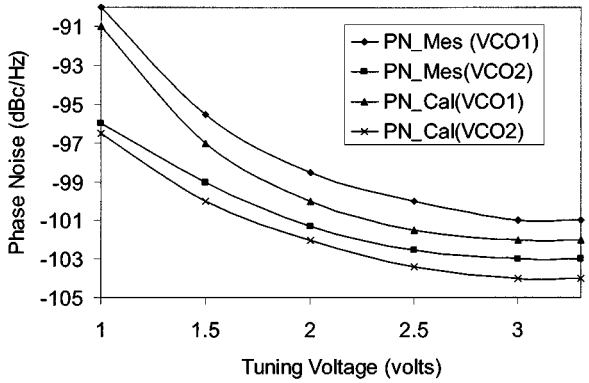

Fig. 10. Measured versus calculated phase noise at 100-kHz offset versus tuning voltage.

should be remembered that oscillators are themselves highly nonlinear and Leeson's formula itself contains approximations including the assumption that the transistor's small-signal noise figure is appropriate. As well, it is difficult to account for all noise sources and transistor parasitic resistance with precise accuracy. Thus, a small error in calculated versus measured results is expected. Nevertheless even using these simple formulas, reasonably accurate results of VCO phase-noise performance can be achieved.

VII. Conclusion

VCO phase noise variation over the entire tuning range has been studied. Theoretical calculations and measurements agree very well. A methodology for the design of a completely integrated differential VCO has been presented. A 1.9-GHz VCO was fabricated in a 0.5-μm bipolar technology with a phase noise of -103 dBc/Hz at 100-kHz offset. The analysis in this work shows that the use of linear varactors will lead to more uniform performance levels. Careful consideration of low-frequency noise is necessary in order to optimize the phase-noise performance of the VCO and to ensure that the phase noise is made as uniform as possible over the tuning range.

Acknowledgment

The authors would like to thank Dr. J. Ojha of Nortel Networks' Technology Access and Applications Department for design support and access to technology. The helpful comments of the reviewers were also greatly appreciated.

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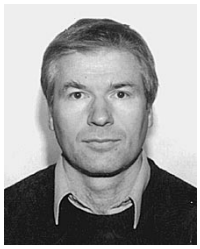

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