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The Effects of AlN and Copper Back Side Deposition on the Performance of Etched Back GaN/Si HEMTs

Georges Pavlidis, Member, Samuel H. Kim, Idriss Abid, Malek Zegaoui, Farid Medjdoub, and Samuel Graham, Senior Member

***Abstract*—The breakdown voltage of GaN/Si high electron mobility transistors (HEMTs) for power electronics has shown to be improved by removing the silicon substrate. The drawback to this approach is the increase in the device's thermal resistance which limits the power dissipation that the device can achieve before severe degradation. This study shows the ability to improve the thermal dissipation of these devices by depositing Copper (Cu) below Aluminum Nitride (AlN) filled etched back GaN-on-Si HEMTs. The device's channel temperature is measured via Raman thermometry. The device's transient thermal dynamics is investigated via transient thermoreflectance imaging and the temperature profile across the gate metal is monitored. In addition to the device's thermal properties, residual stress analysis of the GaN channel is performed via photoluminescence. A notable decrease in the tensile residual stress is observed with the removal of the substrate and the addition of the AlN and Cu layers. Overall, the backside copper is shown to decrease the gate temperature of the etched backed AlN filled devices while maintaining a high breakdown voltage.**

***Index Terms*— AlGaN/GaN HEMTs, self-heating, transient, Thermal Characterization, Temperature**

I. INTRODUCTION

THE ability to fabricate AlGaN/GaN high electron mobility transistors (HEMTs) on silicon (Si) substrates has the potential to reduce the cost of GaN HEMT power electronics [1]. For high voltage operation, large electric fields are developed across the channel making it necessary to maintain high off-state breakdown voltages with large electron densities [2], [3]. Since the electric field extends below the epi layer, the use of a Si substrate in the high electric field region limits the device's capabilities due to its weak electrical field strength [4]. To overcome this obstacle, the removal of the Si substrate has shown to increase the device's breakdown voltage up to 3000 V [5]–[7]. While removing the Si improves the device's electrical capabilities, the device's overall maximum power dissipation is limited due to excessive junction temperature rise [8], [9]. Recent progress to improve the performance of these etched back devices has been reported by applying backside metal processes using copper [10] or aluminum [11]. Prior to depositing copper, PVD AlN is deposited on the backside (Figure 1b) to enable higher blocking voltage capabilities as compared to the reference GaN-on-silicon devices [10]. Furthermore, the subsequent addition of 2 μm of Cu (Figure 1c) is shown to recover 85% of the maximum current density (in reference to a non-etched device) [10]. The origin of this improvement is predicted to be caused by the strong reduction in junction temperature. While the effects of these backside metal techniques on the thermal performance of etched back HEMTs has been numerically studied [12], experimental quantification has yet to be reported.

In this work, the thermal performance of etched back GaN/Si HEMTs with AlN/Cu filled trenches is assessed. To determine the effect of the additional layers, three different devices on the same wafer were prepared starting with GaN/Si HEMTs with an AlN nucleation layer and AlGaN buffer layer (shown in Figure 1). A detailed description of the processing can be found in [10]. Fabricating the devices on the same wafer reduced processing or epi variations during characterization.

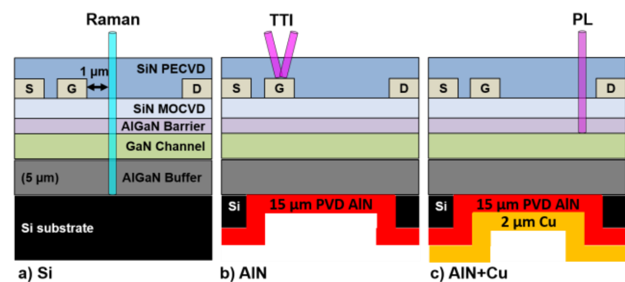

Fig. 1. Stack configuration of a) GaN/Si HEMTs for power electronics with b) etched back substrate and AlN filled trench and c) further addition of Copper (Cu) backside metal deposition. The three experimental techniques employed in this study (Raman thermometry, Transient Thermoreflectance Imaging (TTI) and Photoluminescence (PL) for residual stress analysis) are depicted in the figure.

Steady state thermal analysis is conducted via Raman thermometry [13] to determine the reduction in junction temperatures caused by the addition of the Cu layer. The transient thermal dynamics of each device is also monitored by the gate metal temperature via Transient Thermoreflectance

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Imaging (TTI) [14].

In addition to assessing the device's thermal performance, the effect of the additional layers on the residual stress of the GaN channel is measured via Photoluminescence (PL) [15]. Previous studies have shown that the removal of the Si substrate can alter the residual stress in the GaN layer and ultimately impact the device performance [16]. Reducing the tensile residual stress in HEMTs can prevent the formation of large tensile strains during operation which can induce electrically active defects and mechanical damage [17].

II. Steady State Raman Thermometry

Using a 488 nm laser, Raman measurements were taken 1 μm from the gate on the drain edge at the center of the gate width (shown in Figure 1a). The gate to drain spacing for the devices was 40 μm. Since the GaN layer thicknesses did not change between the device structures, the two-peak method [13] was used to measure the volumetric averaged temperature rise across the GaN layer. Figure 2 shows the steady state thermal response of the devices under DC biasing for two different drain biases: 10 V and 28 V. The gate bias was adjusted to increase the power density.

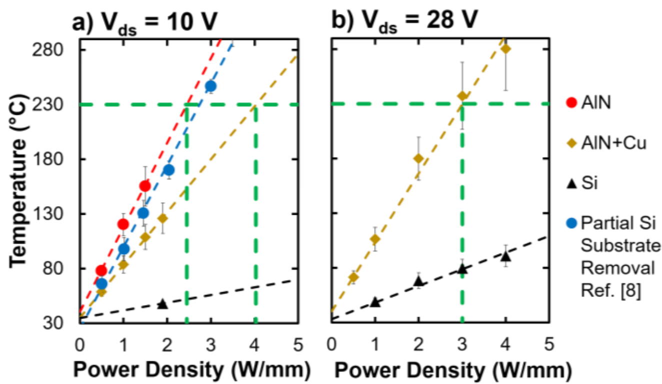

Fig. 2. Comparison of device temperature measured via Raman thermometry at varying power densities for a constant drain bias of a) 10 V and b) 28 V. All measurements were taken at a constant plate temperature of 30 °C.

Temperature measurements were taken at different power densities under a constant base plate temperature of 30 °C. To extrapolate the maximum power density achieved at a 200 °C temperature rise, linear regression was used. For the 10 V drain bias condition, the temperature rise is shown to decrease when transitioning from solely the AlN layer to the combination of AlN and copper. As expected, the Si device achieved a much lower junction temperature in comparison to the etched devices even after the addition of the AlN and the Copper layer.

For a constant drain bias of 10 V, a 11.6x and 7x reduction in maximum power density is observed for the AlN and AlN+Cu device respectively. Increasing the drain voltage to 28 V, the heating profile becomes more localized and the temperature measured via Raman at the gate edge becomes significantly higher [18]. The effect of this localization is confirmed when measuring the thermal performance of the AlN+Cu devices under 28 V bias (a 4.3x power reduction is estimated in contrast to an estimated 7x under 10 V drain bias).

Overall, the power reduction (proportional to the thermal resistance) of the AlN device is shown to be greater than the power reduction reported in previous literature for a locally etched Si device without backside desposition [8] (the thermal performance of the locally etched Si device reported in [8] is plotted in Figure 2a). This increase in thermal resistance can be attributed to the full etching of the substrate below the device. In the previous scenario, the substrate was locally removed below the channel and thus resulted in a smaller increase in thermal resistance. Fully etching the substrate removes the possibility of the localized heating to be conducted via the substrate.

To compare the contribution of the thermal resistance associated with the AlN layer thickness to the overall thermal resistance, the thermal conductivity of the AlN must be measured. Time Domain Thermoreflectance (TDTR) [19] was thus used to measure the thermal conductivity of thin AlN films deposited using PVD. For thicknesses of 4-8 μm of AlN, the thermal conductivity of AlN was measured to be 40-45 W/mK. Extracting the overall thermal resistance of the AlN device via Figure 2, the AlN layer thickness was estimated to contribute to 11% of the thermal resistance (the remainder of the contribution to the thermal resistance was predicted to be caused mainly by the thermal boundary resistance between the GaN and the AlN).

III. Transient Thermoreflectance Imaging

To benchmark the transient thermal performance of these devices, the temperature rise under pulsed biasing was estimated using TTI (Figure 3a). Overall, the presence of a thick SiN passivation layer made it difficult to assess the temperature distribution of the GaN channel [14]. Several LED excitation sources resulted in strong thermoreflectance signals from the GaN region but thin film interference effects caused non-uniformities in the signal [20] and resulted in large uncertainties due to low signal to noise ratios. The most consistent signal was found to be achieved from the gate metal when using a 365 nm LED source. The C_{th} was estimated via calibration [21] to be 1.034 x 10^{-4} °C^{-1}. To directly compare the transient thermal performance to the steady state Raman results, the devices were pulsed biased with a drain bias of 28 V for a 100 μs time period with a 10% duty cycle. The gate bias was adjusted for each device to match a peak current of

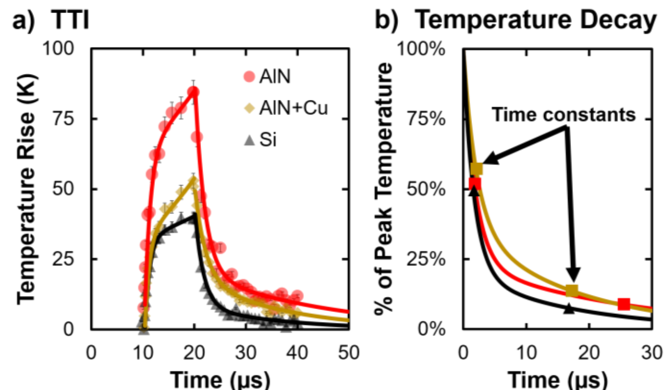

Fig. 3. a) Transient temperature profiles of gate metal measured via Transient Thermoreflectance Imaging (TTI) using a 365 nm LED source b) Comparison of temperature decay of gate metal when no power is dissipated. Markers indicate the time constants calculated when applying a second order exponential fitting to the temperature decays.

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20 mA (5.6 W/mm). Performing a transient sweep of the three devices, the temperature rise and decay of each device can be plotted against each other (Figure 3a).

To capture the peak temperature of the device, the TTI measurements were averaged across 1 µm of the gate metal along the gate width at the center of the device. Similar to the steady state analysis, the AlN device resulted in the highest temperature rise (approximately double the temperature rise detected in the Si device). Regarding the devices' transient dynamics, second order exponential fittings were applied to each transient rise and decay curves. Since steady state conditions were not reached within the 10 µs pulse, the temperature decay fittings were used to extract time constants (Figure 3b). Due to the lower thermal spreading resistance, the silicon device is found to have the shortest time constants ($\tau_{1,Si} \approx 1.7$ µs and $\tau_{2,Si} \approx 16.8$ µs). Despite the AlN/Cu resulting in lower peak temperature than the AlN device, the AlN/Cu device's temperature is shown to decay slower than the AlN device within the first 20 µs. Moving beyond 20 µs, however, the AlN device is shown to decay slower than the AlN/Cu device and is calculated to have a larger time constant ($\tau_{2,AlN} \approx 25.5$ µs compared $\tau_{2,AlN+Cu} \approx 17.3$ µs). This discrepancy suggests that there exists a higher thermal spreading resistance within the first few micrometers of the AlN/Cu device in comparison to the AlN device. While the higher resistance may impede the transient heat dissipation through the device, the overall temperature of the device is reduced by the addition of the Cu back metal layer.

IV. RESIDUAL STRESS ANALYSIS

In addition to monitoring the device's thermal performance, the residual stress of the GaN layer was also measured via Photoluminescence (PL). Previous studies have shown that the residual stress in GaN is reduced when fully etching the Si substrate [8], [16]. To determine whether the addition of new materials would impact the stress relaxation, PL stress mappings were conducted across the channel between the gate and drain in 10 µm steps along the gate width and 5 µm steps across the channel (see Figure 4). The residual stress maps were measured using a Horiba Jobin Yvon LabRAM HR800 with a 325-nm laser as the excitation source. The reference for the band gap strain-free GaN which was used to predict the residual stress of the GaN layer was taken from [15].

The residual stress mappings for the three different devices is plotted in Figure 4. As previously shown in literature [15], [22], the residual stress in GaN grown on Si is found to be tensile (in this study ≈ 950 MPa). The removal of the substrate and the addition of the PVD AlN layer demonstrates a reduction in tensile stress (580 MPa). This reduction in stress is beneficial for device reliability and highlights the ability to etch without "cracking" large area membranes for large industrial power devices. Measuring the stress distribution after the copper layer has been deposited, a slight increase in the overall average stress is observed (750 MPa).

V. CONCLUSION

Overall, the removal of Si substrate allows for higher breakdown voltages in the off state but prevents the excessive Joule heating during operation from being efficiently dissipated. In order to maintain a high electric field strength, the thermal performance of the etched Si can be improved by depositing a combination of materials such as AlN and Copper. The thermal profiles of these devices were assessed using steady state Raman thermometry and Transient Thermoreflectance Imaging (TTI) and the improved thermal performance by addition of these layers compared to the etched Si was quantified as a function of bias. Further residual stress analysis of the GaN channel was performed via Photoluminescence. The removal of the silicon substrate in combination with the deposition of the back layers was shown to reduce the overall tensile stress in the GaN. The relaxation of the GaN layer may potentially increase the device performance and reliability. Beyond improving the performance of lateral GaN HEMTs, the applications of these structures could also benefit the recent development of fully vertical GaN-on-Si devices with selective removal of the substrate and buffer layers [23].

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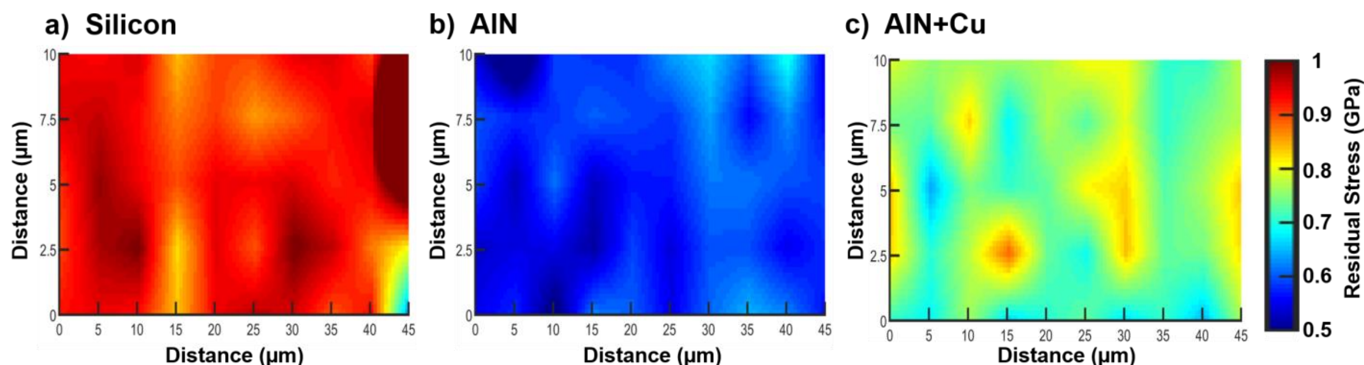

Fig. 4. PL residual stress mappings of the a) GaN/Si HEMTs with b) etched back substrate and AlN filled trench and c) further addition of backside metal deposition of Copper. Stress mappings were performed between the gate and drain in in 10 µm steps along the gate width and 2.5 µm steps across the channel.

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