The EKV 3.0 Compact MOS Transistor Model: Accounting for Deep-Submicron Aspects

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ABSTRACT

The EKV 3.0 compact MOS transistor model for advanced IC design is presented. Its basis is an ideal analytical charge-based model including static to non-quasistatic dynamic aspects and noise. The ideal model is extended to account for the major second-order effects in deep-submicron CMOS technologies resulting from technology scaling and from short-channel effects. It is shown how these nonidealities affect the ideal device characteristics. The increasingly important moderate and weak inversion operation are emphasized. The hierarchical structure of the model is presented, essential features and effects are outlined and illustrated with respect to device characteristics in deep-submicron CMOS.

I. INTRODUCTION

The "charge-sheet" approach to modeling of CMOS based on surface potential (e.g. [1]) has recently gained a renaissance in the community of MOS transistor modeling. Following the EKV model approach [2], a family "charge linearization" models has exploited the incrementally linear relationship [3][8][9] between inversion charge and surface potential to achieve an analytical charge-sheet model with the following essential characteristics:

- Symmetric handling of source/drain effects combined with substrate reference.
- Coherent charge-based modeling of static large-signal and dynamic small signal aspects including non-quasi-static aspects, as well as noise.
- Analytical, continuous, physically correct description of weak, moderate and strong inversion and linear/saturation operation.

The foundations of this model approach are summarized in [8][9][12]. The model remains closely related to the surface potential model and preserves its essential features. Beyond this, it provides a versatile analytical description of the ideal physics of long-channel devices, including static to non-quasi-static effects, with a favorable trade-off among accuracy and efficiency.

The present paper shows how this model is extended to account for effects in advanced deep-submicron CMOS technologies with emphasis on weak and moderate inversion behavior. This compact model, called EKV 3.0, is designed to address needs of advanced analog IC design. The EKV 3.0 MOS transistor model is built hierarchically, with successive steps to account for all major physical effects affecting static and dynamic operation of the device. Selected effects are illustrated with emphasis on operation in weak and moderate inversion, since these require increased attention and refined modeling.

Table I: Summary of basic model expressions and normalization factors.

$I_S = 2n_q U_T^2 \mu C_{ox}' \frac{W}{L}$ $Q_0 = 2n_q U_T C_{ox}'$	$U_T = kT/q$ $G_0 = \frac{I_S}{U_T} = 2n_q U_T \mu C_{ox}' \frac{W}{L}$
$I_D = I_F - I_R = I_S \cdot (i_f - i_r)$ $Q_{iS(D)}' = \frac{q_{f(r)}}{Q_0}$	$\upsilon_P = \frac{V_P}{U_T}$ $\quad \upsilon_{S(D)} = \frac{V_{S(D)}}{U_T}$

Table II: Fundamental relationships in the ideal charge-based model.

$\upsilon_p - \upsilon_s = \ln(q_f) + 2q_f$	$\upsilon_p - \upsilon_d = \ln(q_r) + 2q_r$
$i_f = q_f^2 + q_f$ $q_f = \sqrt{1/4 + i_f} - 1/2$	$i_r = q_r^2 + q_r$ $q_r = \sqrt{1/4 + i_r} - 1/2$
$g_{ms} = G_0 \cdot q_f$ $\frac{g_{ms}}{i_f \cdot G_0} = \frac{2}{\sqrt{1 + 4i_f} + 1}$	$g_{md} = G_0 \cdot q_r$ $\frac{g_{md}}{i_r \cdot G_0} = \frac{2}{\sqrt{1 + 4i_r} + 1}$

Table III: Definition of basic physical model parameters, pinch-off voltage, slope factor and linearization factor.

$C_{ox}' = \frac{\varepsilon_{ox}}{T_{ox}}$ $V_{TO} = V_{FB} + \Psi_0 + \gamma_s \sqrt{\Psi_0}$	$\gamma_s = \frac{\sqrt{2q\varepsilon_{si}N_s}}{C_{ox}'}$ $\Psi_0 \cong 2\phi_F = 2U_T \ln\left(\frac{N_S}{n_i}\right)$
$V_P \cong \frac{V_G - V_{TO}}{n_v}$	$n_v = 1 + \frac{\gamma_s}{2\sqrt{\Psi_0 + V_P}}$ $n_q = 1 + \frac{\gamma_s}{2\sqrt{\Psi_0 + V_P/2}}$

II. IDEAL CHARGE-BASED MODEL

The ideal model of the MOS transistor provides the relationships among the fundamental variables within the MOS structure [2][7][8][12]. A detailed derivation of the ideal charge based model is found in the companion paper [12] and in [8]. A consistent normalization procedure leads to the definitions of model quantities and relationships [8] as summarized in Table I and Table II. The normalization quantities used are the *specific current* I_S [2], the thermal voltage U_T,

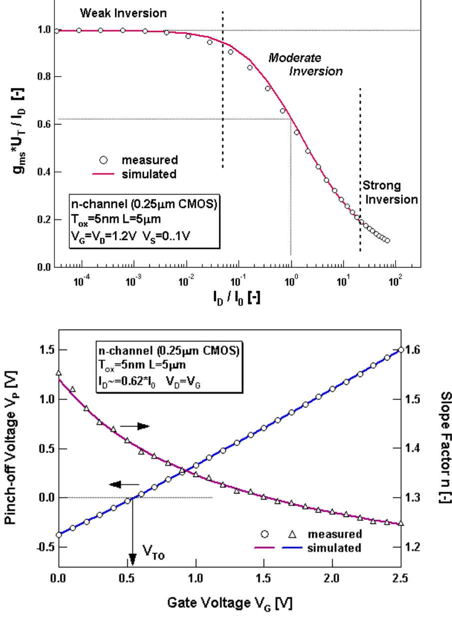

Fig. 1. Source transconductance to current ratio in saturation from weak to strong inversion, measured and simulated pinch-off voltage and slope factor, 0.25um CMOS.

the *specific charge* Q_0 and the *specific transconductance* G_0 [8].

The gate-, source- and drain transconductances are defined as,

$$g_{mg} \equiv \frac{\partial I_D}{\partial V_G} \qquad g_{ms} \equiv -\frac{\partial I_D}{\partial V_S} \qquad g_{md} \equiv \frac{\partial I_D}{\partial V_D} \tag{1}$$

where V_G, V_S, V_D are voltages referred to the substrate.

The ideal relationships are established among voltages and inversion charge densities $q_{f(r)}(\upsilon_p - \upsilon_{s(d)})$ [3][4][5], current and inversion charge densities $i_{f(r)}(q_{f(r)})$, transconductances and inversion charge densities $g_{ms(d)}(q_{f(r)})$. All expressions are symmetrical for source and drain sides. The ideal relationship among transconductance to current ratio [4][5][6] and current is provided.

Finally, expressions for the *pinch-off voltage* V_P, as well as the *slope factor* n_v [2] and *charge linearization factor* n_q [9][8] are given and related to the physical and electrical device parameters in Table III: *oxide capacitance* C_{ox}', *substrate factor* γ_s, Ψ_0 being approximately twice the Fermi potential, the *flat-band voltage* V_{FB} and the resulting *threshold voltage* V_{TO}, as well as the *mobility* μ. Electrical constants have their usual meaning.

The source transconductance to current ratio $g_{ms}U_T/I_D$ in saturation, is represented versus the normalized drain current I_D/I_S (on a logarithmic axis) in Fig. 1 a). The so-called *inversion factor* $IC = I_D/I_S$ is convenient to distinguish operation at different levels of inversion: weak inversion corresponds roughly to $IC < 0.1$, where $g_{ms}U_T/I_D$ reaches its maximum of 1; moderate inversion to $0.1 < IC < 10$ and strong inversion to $IC > 10$. The ideal model fits the measurements well for all levels of inversion, particularly weak and moderate inversion. In very strong inversion, a deviation is due to reduced mobility not accounted for in the ideal model expression. This characteristic is "universal", since it is practically independent of technology, gate bias, and temperature for long-channel transistors [5][8]. A notable change in very short-channel devices will be discussed later.

The Fig. 1 b) illustrates the pinch-off voltage V_P and slope factor n_v vs. gate voltage characteristics for the same transistor. The pinch-off voltage is essentially dependent on threshold voltage and substrate factor, and is therefore naturally technology-dependent. n_v provides an important relationship between gate, source- and drain transconductances:

$$g_{mg} = \frac{g_{ms} - g_{md}}{n_v}. \tag{2}$$

The slope factor n_v is related to the inverse weak inversion slope $S \cong 2.3 \cdot n_v \cdot U_T$, defined as the required change in V_G to change drain current by one decade [8]. Since n_v depends on gate voltage, S is also gate-voltage dependent rather than a constant. In saturation, $g_{mg} \cong g_{ms}/n_v$, therefore, the inverse weak inversion slope with a change in V_S is $S_S \cong 2.3 \cdot U_T$ and therefore always lower than with a change in V_G.

III. MODEL EXTENSIONS IN EKV 3.0

A. *Structure*

The ideal charge-based model is extended so that all of its aspects from static to dynamic operation, including non-quasistatic modeling [12] as well as noise [8], are handled within the same coherent framework. The modeling of quasistatic charges and transcapacitances is addressed in [7][8].

The dynamic aspects of the model were developed using several approximations. Mobility is assumed bias-independent and constant in the whole channel, an assumption which has a negligible incidence on the accuracy of charges/transcapacitances modeling. However, accurate modeling of static aspects such as drain current and transconductances of course implies the accounting for bias-dependence of mobility and short-channel effects. This is equally important as a basis for correct description of mobility in the non-quasistatic model. Further information on the approach to the modeling of mobility effects can be found in [8].

Furthermore, important aspects in deep submicron CMOS affect the device operation. These are generally related to the use of highly doped channel and polysilicon gate, leading to polydepletion and quantization effects in the channel. The device structure of present standard deep submicron CMOS technology is in general symmetric between source and drain, however, important non-uniformities exist both in the vertical and longitudinal directions. Finally, the non-ideal field distributions in short- and narrow-channel devices degrade their electrical characteristics in many ways.

The Table IV provides a synthesis of the main effects considered in EKV 3.0 that affect weak and moderate inversion operation. The affected relationships are summarized and the related model parameters are indicated.

As a principle, all the refinements introduced revert to the basic model expressions if a particular effect is not dominant. Note that all changes of a given quantity are automatically propagated throughout the whole model structure.

Table IV: EKV 3.0 static model structure and extensions based on ideal long-channel model.

modeled/affected relationships:	*physical/electrical parameters:*
Modeling of substrate/gate doping related effects	
Vertical Non-Uniform Doping	
$V_P(V_G)$, $n_v(V_P)$	γ_{s1} , γ_{s1} , V_R , dV_R
Longitudinal Non-Uniform Doping/Oxide Charge	
$\gamma_s(L)$, $V_{FB}(L)$	L_K , N_K , Q_K
Polydepletion Effect	
$V_P(V_G)$, $n_q(V_P)$, $n_v(V_P)$	γ_p
Quantum Effect	
C_{oxe}' , γ_{se} , γ_{pe} , Ψ_{0e}	σ_{qm}
2D Charge-Sharing	
$\gamma_s(V_S,V_D,L)$, $V_{Ge}(V_G,W)$	η_L , η_W , V_{bi}
Drain Induced Barrier Lowering	
$V_P(V_G,V_S,V_D,L)$	σ_L , σ_D

B. Device Non-Uniformities

The use of channel implants and pocket/halo implants leads to important non-uniformities both in vertical and lateral direction. Vertical non-uniformity of the channel profile, using conventional profiles or retrograde profiles, alter the $V_P(V_G)$ relationship, and as a consequence, also $n_v(V_G)$. The physical parameters γ_{s1} , γ_{s1} , V_R , dV_R are related to the actual doping levels near the surface or deeper in the substrate, and to their spread with depth.

The longitudinal non-uniformity of the device structure results mostly from the use of pocket implants as well as dopant distribution during thermal processing. Longitudinal non-uniform doping distribution in the substrate and oxide charge non-uniformity lead to the well-known reverse short-channel effect (RSCE), resulting in a threshold voltage roll-up with decreased channel length. Furthermore this also affects device mobility due to the increased levels of channel doping. The physical parameters involved are related to the characteristic length L_K and pocket implant doping N_K , and oxide charge density Q_K , respectively

C. Polydepletion and Quantum Effects

Depletion in the polysilicon gate and quantization effects in the inversion charge layer lead to the characteristic reduction of inversion/accumulation capacitance, and threshold voltage shifts as illustrated in Fig. 2. The modeling of the quantum effects account for the surface potential increase depending on the effective field in the channel according to the Van Dort model. In terms of model internal quantities, polydepletion and quantum effects both reduce the charge linearization factor n_q and hence charges (via Q_0) and transcapacitances, as well as drain current (via I_S) and transconductances [9][10][11]. This effect is most sensible in moderate to strong inversion. In weak inversion, the increase in n_v is responsible for a degradation of the weak inversion slope (for a change with V_G).

The physical device parameters are the gate factor γ_p related to the gate doping, and a fitting parameter for quantum effects σ_{qm} related to the Van-Dort model. Furthermore, quantum effects can be directly interpreted as a change in the electrical parameters [10][11]: increased apparent Ψ_0 , reduced apparent C_{ox}' , increased apparent γ_s and increased/reduced γ_p depending on the relative importance of polydepletion and quantum effects.

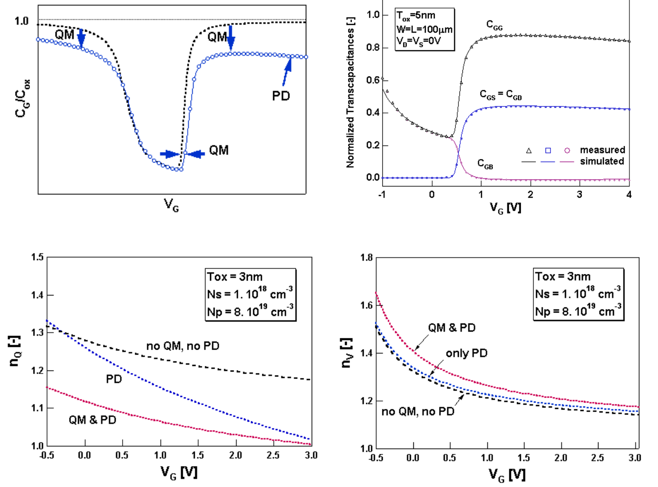

Fig. 2. Effect of polydepletion and quantization effects on gate capacitance (top left), transcapacitances of an 0.25um CMOS technology (top right), linearization factor n_q and slope factor n_v (bottom).

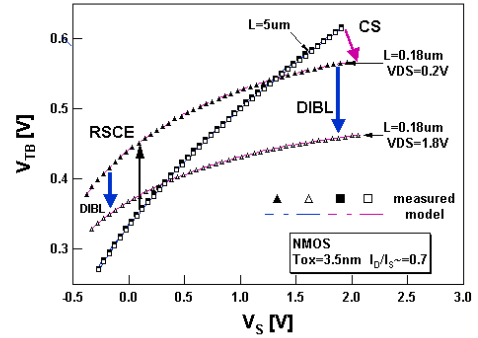

Fig. 3. Effect of reverse short-channel effect (RSCE), charge-sharing (CS), and drain induced barrier lowering (DIBL) on $V_{TB}(V_S)$ characteristics for an 0.18um CMOS technology.

D. Charge-Sharing for Short- and Narrow Channel

Geometrical considerations on the depletion charge in short-channel transistors lead to a simple model in which the depletion charge controlled by the gate is reduced; its electrical equivalent, γ_s , is therefore reduced and becomes a function of channel length, V_S and V_D , As a consequence, the slope of the threshold voltage dependence on V_S is reduced as indicated in Fig. 3. This reduction of the substrate effect also corresponds to a decrease of n_v . Threshold voltage V_{TB} [2] (referred to substrate) for a long-channel and a short-channel device of an 0.18um CMOS technology are shown, which have been measured with a constant current technique in moderate inversion.

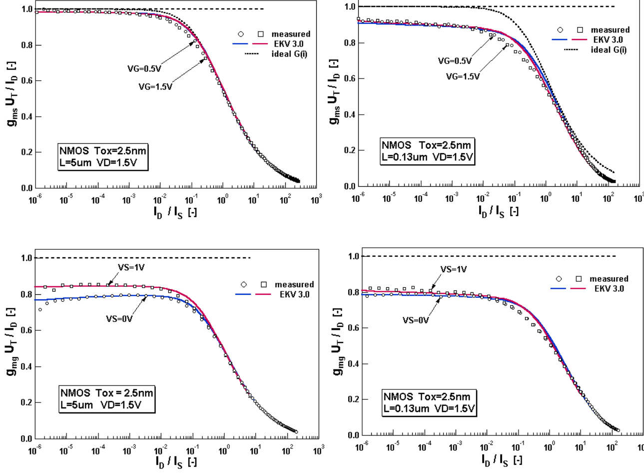

Fig. 4. Source- (top) and gate (bottom) transconductance to current ratio in saturation vs. normalized drain current from weak to strong inversion for 0.13um CMOS for long-channel (left) and short-channel (right). The top right figure demonstrates substantial source-transconductance to current ratio degradation for short-channel devices due to DIBL effect.

E. Drain Induced Barrier Lowering

Drain induced barrier lowering (DIBL) is a major effect governing short-channel devices of deep submicron CMOS technologies. Its major manifestation lies in threshold voltage reduction with increased drain bias, as indicated in Fig. 3. A quasi-2D solution of the Poisson equation yields a symmetric expression in terms of source and drain voltages for the barrier reduction $\Delta\Psi_s$, which is introduced into the pinch-off voltage as,

$$V_P = V_{P0} + \frac{\Delta\Psi_s(V_S, V_D, L)}{n_{v0}} \tag{3}$$

where V_{P0} and n_{v0} are pinch-off voltage and slope factor without considering DIBL. $\Delta\Psi_s$ has an exponential length-dependence and its importance is also related to the physical device parameters. Two parameters only, σ_L, σ_D, are used to adjust the importance of the DIBL effect with geometry and bias. As shown in Fig. 3, the combination of all effects, including non-uniform doping effects, RSCE, polydepletion/ quantum effects, charge sharing and DIBL, allows to correctly account for the observed bias effects.

Finally, in Fig. 4, the source- and gate transconductance to current ratios for an 0.13um CMOS technology are shown for long- and short-channel devices. The EKV 3.0 model shows accurate modeling of both transconductance to current ratios *simultaneously*, at all levels of inversion. Of particular interest is the degraded weak inversion behavior of $g_{ms}U_T/I_D$ at short channel, which, to the knowledge of the author, has not been previously published. This degradation can clearly be attributed to drain induced barrier lowering.

Naturally, DIBL also affects output conductance in an important way. Although not shown here due to lack of space, the DIBL model introduced in EKV 3.0 shows excellent simultaneous modeling of all transconductances at all channel lengths.

IV. CONCLUSIONS

The EKV 3.0 MOS transistor model structure has been presented. The ideal charge-based model is closely related to surface-potential modeling using the same physical parameters. It provides a versatile analytical framework with a coherent modeling hierarchy for static and dynamic model aspects, supporting advanced analog IC design.

Model extensions in EKV 3.0 have been illustrated with particular emphasis on weak and moderate inversion operation. The inversion charge linearization scheme has been extended to include both polydepletion and quantum effects within the same approach. Non-uniformity of the device in both vertical and lateral direction are considered and combined with refined models for charge-sharing and drain induced barrier lowering, using a minimum set of physical device parameters. Strong DIBL causes the source transconductance to current ratio to depart significantly from its ideal long-channel behavior in moderate and weak inversion.

The EKV 3.0 model allows to consistently account for bias- and scaling effects on all transconductances at all levels of inversion and is therefore particularly suitable for analog IC design using deep-submicron CMOS technologies.

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