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The Electromagnetic Compatibility of Integrated Circuits-Past, Present, and Future

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The Electromagnetic Compatibility of Integrated Circuits—Past, Present, and Future

Mohamed Ramdani, *Senior Member, IEEE*, Etienne Sicard, *Senior Member, IEEE*, Alexandre Boyer, Sonia Ben Dhia, *Member, IEEE*, James J. Whalen, *Life Senior Member, IEEE*, Todd H. Hubing, *Fellow, IEEE*, Mart Coenen, *Member, IEEE*, and Osami Wada, *Member, IEEE*

***Abstract*—Throughout the decades of continuous advances in semiconductor technology, from the discrete devices of the late 1950s to today's billon-transistor system-on-chip, there have always been concerns about the ability of components to operate safely in an increasingly disruptive electromagnetic environment. This paper provides a nonexhaustive review of the research work conducted in the field of electromagnetic compatibility (EMC) at the IC level over the past 40 years. It also brings together a collection of information and trends in IC technology, in order to build a tentative roadmap for the EMC of ICs until the year 2020, with a focus on measurement methods and modeling approaches.**

***Index Terms*—Emission, history, ICs, modeling, roadmap, standards, susceptibility.**

I. Introduction

ELECTROMAGNETIC compatibility (EMC) research focusing on ICs is not just a recent topic. Early electrical simulators, forerunners of the well-known SPICE simulation tools, were originally designed for simulating the susceptibility of electronic devices to radio frequency interference (RFI). This paper is a modest attempt to review the key developments that have marked the history of research in IC immunity and emissions.

In the past ten years, concerns about EMC have risen in importance as low emissions and high immunity to interference have emerged as key differentiators in overall IC performance. Advances in process integration, higher switching speeds, and more complex circuits tend to increase the amount of parasitic emissions generated by ICs. Reduced supply voltages and an increased number of interfaces tend to decrease the immunity to RFI. EMC has become one of the major causes of IC redesign, mainly due to inadequate design methods and lack of expertise in parasitic noise reduction and immunity improvement. Specific workshops [1] and dedicated sessions at major conferences have enhanced dialogue and exchanges within the IC-EMC community. With the International Electrotechnical Commission (IEC) international standardization committee, applicable standards have emerged both for IC emission and susceptibility characterization [2], and are discussed in Section IV-C. A collaborative book dedicated to the field of EMC at IC level has also been published [3].

The idea of a historical review and roadmap following advances in the EMC of ICs emerged from the authors during EMC Compo 2005 in Munich, Germany. The target was to publish in 2009 an anniversary paper to acknowledge the 30th anniversary of the special issue devoted to the effects of RFI on ICs [4], which appeared in 1979.

An overview of topics that have enjoyed particular scientific interest over the past decades and hold potential for future developments is given in this paper, which comprises four parts. Section II concerns the early work on EMC at the component level and a selection of publications prior to 1996. In Section III, a set of references covering the period 1996–2009 is given. The prospective part of the paper starts with Section IV, which concerns the global trends in the semiconductor technology and the evolution of key parameters that have a direct impact on EMC. The last section gives prospective scenarios for the evolution of parasitic emission and immunity of ICs, as well as roadmaps focusing on standard measurement methods and EMC models.

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II. Early Studies on the EMC of ICs

We list here a selection of papers that illustrate advances in the understanding of IC performance in terms of parasitic emission and susceptibility to RFI. This nonexhaustive selection is given in chronological order. The earliest EMC investigations, which primarily concerned the protection of components exposed to a harsh environment, are detailed in Section II-A. During the 1990s, concerns grew over the safety implications of parasitic emissions from components embedded in automotive and aeronautic systems. At the same time, the power and frequency range of transmitters were increasing, creating a more severe and uncontrollable electromagnetic (EM) environment. A selection of important publications related to this evolution is given in Section II-B.

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SCEPTRE: A Program for Automatic Network Analysis*

Abstract: This paper describes the mathematical formulation of a computer program for automatic transient analysis of electronic networks. The formulation is based on the "state-variable" approach to network analysis and differs from other such programs primarily in the way that the network equations are manipulated to produce a solution. SCEPTRE includes a number of features aimed at providing greater flexibility and convenience for users of the program. Important among these features is that no prescribed equivalent circuit for active elements is required for program operation. Also, linearly dependent voltage and current sources in a network can be handled by the program, and provision has been made to allow a free-form format for input data. The paper includes a discussion of the program's ability to solve networks containing time-varying passive elements, and considers the factors that influence program running time.

* Work supported by the Air Force Weapons Laboratory under contract AF 29(601)-6852. Dissemination of the SCEPTRE program is controlled by the Air Force Weapons Laboratory, Attn: WLRET (Capt. Gary Pritchard), Kirtland Air Force Base, New Mexico 87117.

627

IBM JOURNAL · NOVEMBER 1967

Fig. 1. Software SCEPTRE was originally designed for simulating the radiation of electronic devices [5].

A. Beginning

Not many people know that research into the EMC of ICs had its roots in military research. As early as 1965 at the Special Weapons Center at Kirtland Air Force Base, New Mexico, studies were conducted into the effects of EM fields trigged by nuclear explosions on electronic devices used in missile launch sites. As a result of this effort, the simulation software SCEPTRE [5] was developed at International Business Machines (IBM) (see Fig. 1) for simulating the effects of nuclear radiation on electronic components. With this software, it was possible to correlate simulations and experimental measurements obtained on an EM impulse test bench.

At the electronic equipment level, techniques were developed to protect radio, television, and radar transmitters. Several military standards were published in the United States to define the interference levels that equipment should be able to withstand and to specify measurement methods for characterizing the effect of electromagnetic interference (EMI).

One of the earliest academic publications on the simulation of ICs concerned the 741 integrated operational amplifier (a versatile linear amplifier including around 100 bipolar and passive devices, with 25-mA output current capabilities, originally designed for audio applications), and was published by Wooley and Pederson [6] in 1971. The author succeeded in simulating the different stages of this component with the simulation software CANCER at the University of California at Berkeley (computer analysis of nonlinear circuits, excluding radiation). This software had no link to EMC concerns but allowed easy simulation of device behavior at that time.

In 1975, Richardson *et al.* [7] examined the response of low- and medium-frequency transistors to microwave energy. The rectified signal changes the quiescent operating point and the current gain of the transistor (see Fig. 2).

In 1978, a handbook (see Fig. 3) was published by the McDonnell Douglas Astronautics Company [8] that was expected to make a significant contribution to the EMC community. It contained information on the susceptibility of ICs to high-power RF and microwave energy. It presented the results of thousands of tests on ICs, including the most commonly used digital and linear types, and showed the lowest power levels (versus frequency) at which these circuits were observed to be susceptible. This information was useful in a variety of EMC design and analysis activities at this time.

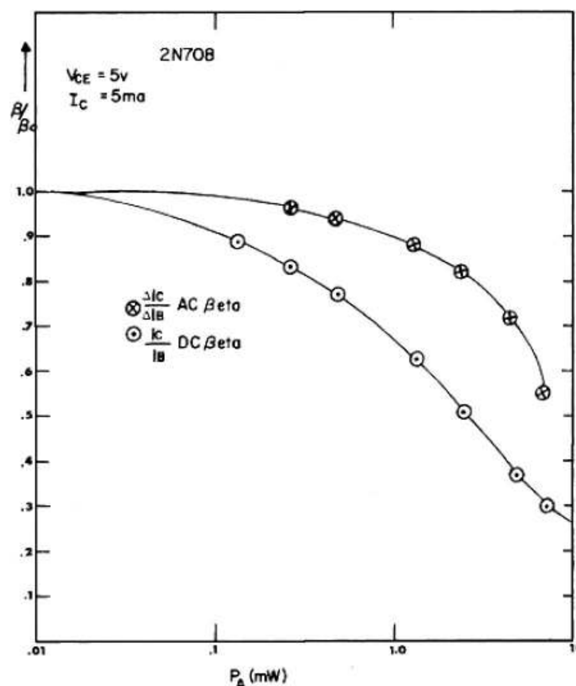
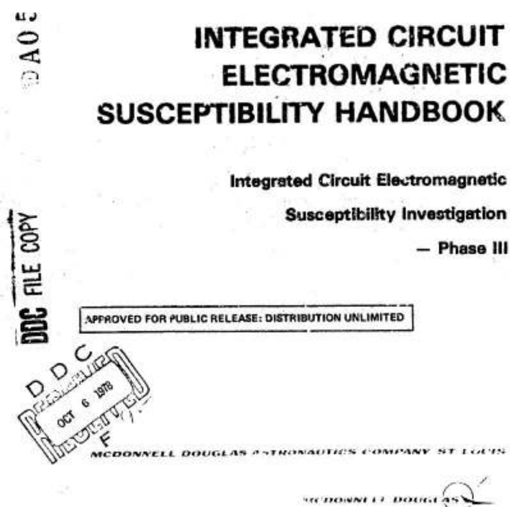


Fig. 2. Reduction in dc and low-frequency ac current gain for a 2N708 transistor versus absorbed 2 GHz microwave power [7].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Integrated Circuit Electromagnetic
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— Phase III

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MCDONNELL DOUGLAS ASTRONAUTICS COMPANY ST. LOUIS

Fig. 3. First handbook on susceptibility published by McDonnell Douglas Astronautics Company [8].

B. Selected Papers

We list here a selection of papers that illustrate advances in the understanding of IC performance in terms of parasitic emission and susceptibility to interference.

As a pioneer in the field of IC EMC, Whalen [4] published in 1979, in a special issue of the IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY (see Fig. 4), papers devoted to the effects of RFI on ICs. In his editorial, Whalen justified the need for the special issue in terms of the growing risk of

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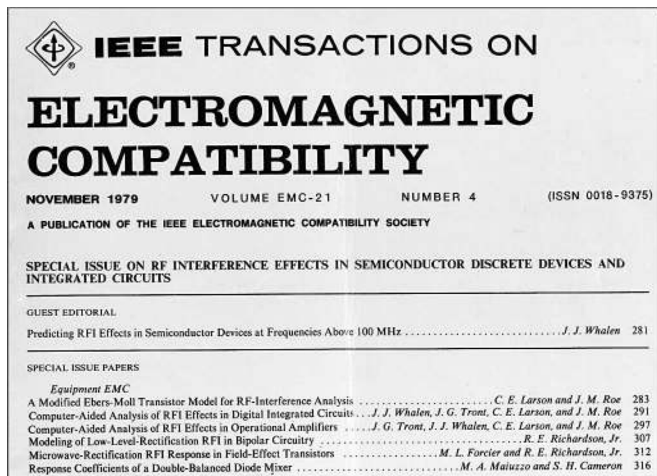
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SPECIAL ISSUE ON RF INTERFERENCE EFFECTS IN SEMICONDUCTOR DISCRETE DEVICES AND INTEGRATED CIRCUITS

GUEST EDITORIAL

Predicting RFI Effects in Semiconductor Devices at Frequencies Above 100 MHz . . . . J. J. Whalen 281

SPECIAL ISSUE PAPERS

Equipment EMC

A Modified Ebers-Moll Transistor Model for RF-Interference Analysis . . . . C. E. Larson and J. M. Roe 283
Computer-Aided Analysis of RFI Effects in Digital Integrated Circuits . . . J. J. Whalen, J. G. Tront, C. E. Larson, and J. M. Roe 291
Computer-Aided Analysis of RFI Effects in Operational Amplifiers . . . . J. G. Tront, J. J. Whalen, C. E. Larson, and J. M. Roe 297
Modeling of Low-Level-Rectification RFI in Bipolar Circuitry . . . . R. E. Richardson, Jr. 307
Microwave-Rectification RFI Response in Field-Effect Transistors . . . . M. L. Forcier and R. E. Richardson, Jr. 312
Response Coefficients of a Double-Balanced Diode Mixer . . . . M. A. Maiuzzo and S. H. Cameron 316

Fig. 4. First IEEE Transaction devoted to susceptibility for ICs.

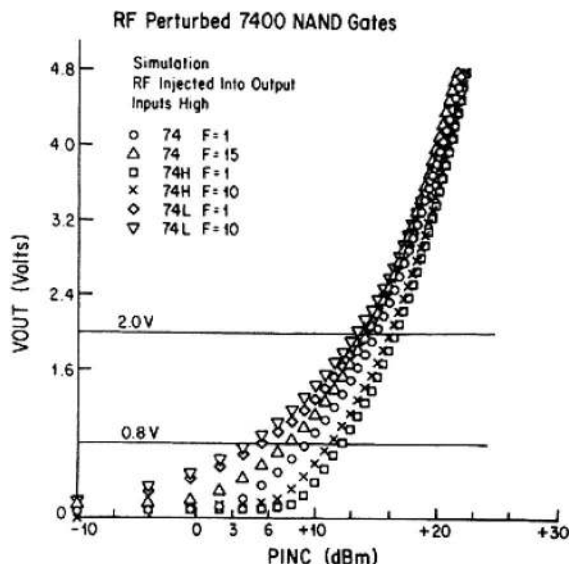

Fig. 5. SPICE simulation values of the output VOUT versus the incident RF power incident power (PINC) for three 7400-NAND-gate types with different fan-outs [4].

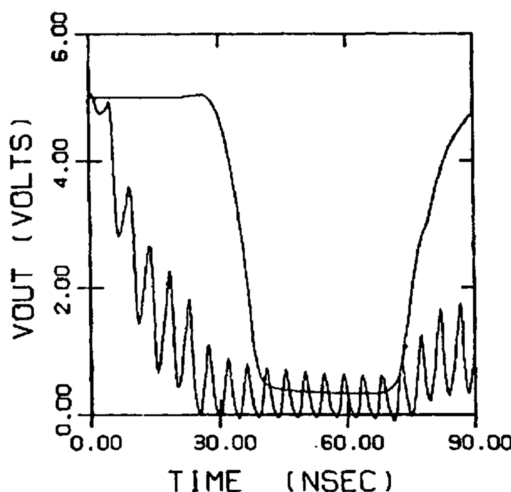

Fig. 6. VOUT versus time for VM 20 V and $f = 220$ MHz. A plot of the unperturbed VOUT has been superimposed on the curve [11].

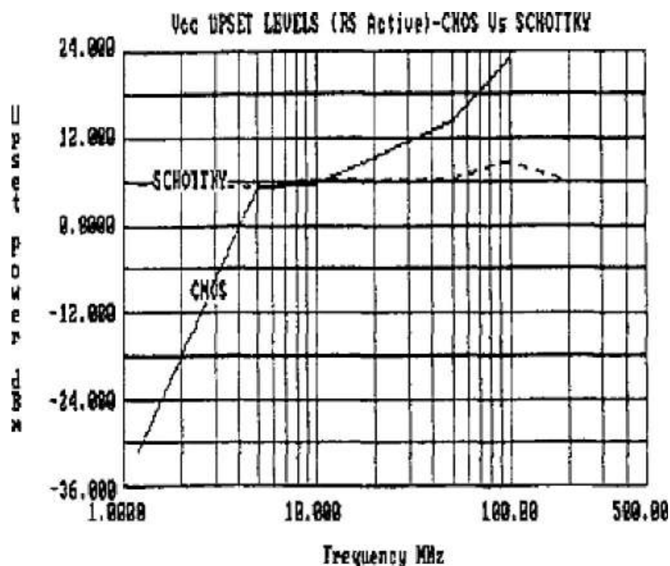

Fig. 7. RF upset power versus frequency comparison for the CMOS circuit versus the Schottky circuit with RF entry into the Vcc pin [13].

interference from EM sources in the very high-frequency band. The special issue dealt specifically with the effects of EMI on semiconductor devices and the modeling of these effects by means of dedicated simulation tools.

Whalen studied the effect of RFI upon bipolar digital ICs, such as 7400 NAND (see Fig. 5) gates and showed that output varies with the incident power, as shown in Fig. 5.

The need to modify available device models to account for the unusual conditions of RFI was expressed by Larson *et al.* [9], who proposed a modification of the bipolar transistor model with a specific discussion on rectification in p-n junctions.

CMOS technology gave rise to ever larger and denser chips that began to displace bipolar technology, mainly because of superior performance in terms of power dissipation. The first susceptibility analysis of MOS components was published in 1980 and involved memory circuits. Roach [10] characterized the sensitivity of 1-kB n-type MOS (NMOS) memories. In 1985, a study was published by Tront [11] concerning the behavior of the 8085 processor in the presence of 100 and 220 MHz RFI. Using the simulation software SPICE, he reproduced some of the phenomena observed during measurements (see Fig. 6).

Watchdog circuits were added to microprocessors by Lu [12] for structural integrity checking (SIC). Watchdog circuits were found to be of great importance for processor recovery and safe reset after undergoing EMI. In 1985, Kenneally *et al.* [13] reported a comparison of measurements of RF upset levels on two types of D-type flip-flops, which were functionally identical but built from different technologies: CMOS and low-power Schottky (see Fig. 7). Measurements on the clock and data ports suggested that: 1) the CMOS device is “RF harder” than the Schottky device by at least 3–18 dB above the 5–10 MHz range and nearly insensitive above 100 MHz and 2) below that range, the Schottky device may be “RF harder” by 3–6 dB, but there

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were not enough measurement data to confirm this performance below 5 MHz.

In 1988, Mardiguian [14] included in his book a chapter completely devoted to analog and logic active devices. In this chapter, the author reviewed emission and susceptibility aspects (in-band and out-of-band susceptibility) in a number of microelectronics devices.

In 1990, Bakoglu [15] compiled a remarkable synopsis of the parasitic effects in ICs, packaging, and printed circuit boards (PCBs). He described different problems linked to transient current consumption at active edges of the clock and detailed the basic mechanisms for IC resonance. Package models were provided for dual in-line (DIL), quad flat pack (QFP), and pin grid array (PGA) families.

In 1991, Laurin *et al.* published a study of the effects of RF perturbations on the oscillator circuits [16] used in a Motorola 6809 processor. While placing an electric current loop close to the oscillator, they observed function losses in the microprocessor and data losses on the serial data bus.

Also in relation to microprocessors, Tang [17] showed that EMI could cause nonfatal failures that resulted in counting inaccuracies in microprocessors. In 1993, he performed conducted and radiated susceptibility measurements, and was able to demonstrate a specific byte-swap problem on the most significant byte of a counter, leading to severe counting errors. Solutions based on software modifications and PCB layout improvements were proposed. The author pointed out that low-speed systems were as vulnerable to EMI as high-speed systems.

In 1991, a study was published by Graffi *et al.* [18] describing the behavior of 741 operational amplifiers when a 200 kHz–50 MHz interference signal was superimposed on normal signals. They obtained good correlations between experimental measurements and simulations using a simplified macromodel that accelerated the computation by a factor of up to 50.

Synchronous switching noise is one of the most significant chip-level concerns for EMC and signal integrity engineers. In 1994, Hardin *et al.* [19] proposed a technique that is referred to as spread spectrum clock generation (SSCG). This technique consists of the frequency modulation of a digital clock signal with a unique waveform. The amplitudes of the harmonics of the clock signal and all signals synchronized with it are significantly reduced, and thus the energy of each frequency harmonic is spread over a wider bandwidth, thereby reducing the amplitudes of the harmonics but only when the detection bandwidth is less than the frequency modulation spread (see Fig. 8).

In 1995, Laurin *et al.* [20] proposed two methods for investigating the effects of radiated RFI on the operation of logic circuits, one for large signals and one for small signals. Both methods are based on the use of circuit simulators that allow accurate modeling of the solid-state devices forming a logic circuit. In the circuit simulator environment, incident RFI fields are replaced by an equivalent set of current sources, and the circuit wiring is replaced by an equivalent network. The source currents and admittance parameters of the wire structure are derived using a thin-wire moment-method code.

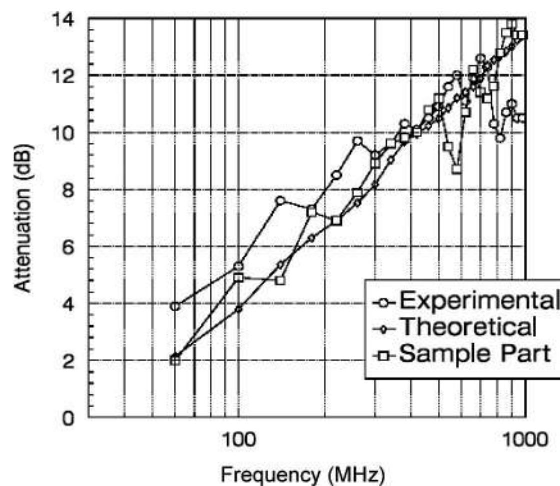

Fig. 8. Measured and theoretical values of attenuation provided by SSCG [19].

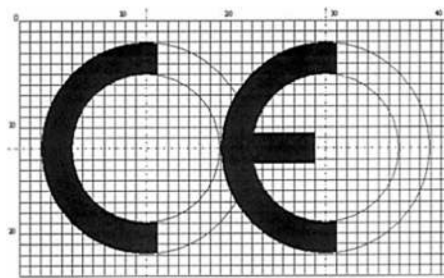

Fig. 9. CE conformity marking, which indicates the conformity of electrical and electronic equipment with European directives.

III. Research in EMC for ICs Between 1996 and 2009

Over recent years, the EM environment of ICs has gone through a gradual process of expansion in terms of frequency bandwidth utilization, power used in wireless communications, and signal modulation complexity. The need for low-emission and highly immune ICs within the frequency band 1 MHz–1 GHz rose rapidly, putting IC support engineers and designers under extraordinary pressure. In the following sections, we highlight the most important events and introduce some important scientific contributions to emission (Section III-B) and susceptibility (Section III-C) for the period 1996–2009.

A. Introduction

The year 1996 was a milestone for EMC history since European directives related to EMC of electrical and electronic equipment (89/336/EEC) became fully operational [21]. Electronic systems had to comply with specific limitations in terms of parasitic emission levels and susceptibility to external perturbations. Numerous EM compliance centers were established in this period to ensure that qualification tests conformed with European Directives (see Fig. 9). Note that none of these directives applied directly to ICs.

However, demand for low-emission and highly immune ICs rose rapidly and impacted IC support engineers and IC designers. Growing demand concerned EMC characterization

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TABLE I
EUROPEAN RESEARCH PROJECTS DEDICATED ON EMC OF ICs

Name of the project	Years	Description
JESSI AC-5	1989-1997	EMC modeling and measurement methods
MEDEA A408 – EMC Workbench	1996 - 1999	EMC at IC and PCB level, on-chip crosstalk and IC emission modeling
MEDEA + A509 - MESDIE	2000 - 2003	EMC at IC level, test chip manufacture, low emission rules
EPEA	2007 - 2010	EMC platform for embedded applications, immunity standard for components

methods, methodologies for modeling parasitic emission, and guidelines for IC design with improved EMC. The pace of development of component-level EMC knowledge has quickened since 1996.

Several academic laboratories started activities related to the EMC of ICs; research teams combining industrial companies and academics were established during this period to respond to the industrial need for improved EMC performance. Table I gives some examples of European projects launched between 1996 and 2009 related to EMC of ICs. Consequently, an increased number of scientific contributions together with special issues [22] and a book specifically focusing on the topic [3] were published.

For many years, most international conferences (IEEE EMC Symposia, EMC Europe, EMC Zurich, EMC Asia) have had at least one or two sessions entitled "EMC at Component Level." However, the first workshop entirely dedicated to IC EMC was held in January 1999 in Toulouse, France (*CEM Compo 99*), followed by a second edition in June 2000, also in Toulouse. The third workshop (*EMC Compo 02*) attracted approximately 70 experts mainly from France, Germany, Italy, and Belgium. In 2004, more than 100 experts from academic institutes and industry attended the fourth workshop (*EMC Compo 04)* held in Angers, France. The 2005 edition was organized in November in Munich, Germany (*EMC Compo 05*), and the 2007 edition (see Fig. 10) in November in Turin, Italy (*EMC Compo 07*) with a steady growth in attendees, particularly from Asia [23].

B. Research Work Related to Parasitic Emissions of ICs (1996–2009)

We list here a selection of papers that illustrate advances in the understanding of IC performance in terms of parasitic emissions. The papers are classified according to a set of subtopics.

1) Simultaneous Switching Noise: Parasitic emission of ICs has their origin in the phenomenon called simultaneous switching noise (SSN). This voltage drop comes from the *RLC* response of a chip's power and ground supply rails and its package to current demands produced by a large number of logic gates at each clock commutation. In the early nineties, SSN was thought to be influenced only by the number of switching output drivers.

Fig. 10. Web site of EMC Compo 2007, the 6th International Workshop on EMC of ICs [23].

However, Senthinathan and Prince [24] were one of the first to establish more precise formulations aiming at estimating the peak voltage of ground bounce. They demonstrated that SSN is also influenced by the effect of the negative feedback of power and ground bounce. They presented results showing the dependence between the noise amplitude and the number of switching I/Os, ground connection pins, and channel length. Vaidyanath *et al.* [25], [26] reused the same formulations to study the influence of driver loads and interactions between power planes and signal traces within a package on the SSN. These works highlighted the key role of the power distribution network in understanding and estimating noise propagation.

2) Parameters Influencing Parasitic Emission: Parasitic EM emissions of components are strongly related to several parameters such as the IC technology, the package, the number of switching gates, and I/Os. Robinson *et al.* [27] compared the radiated emissions produced by inverters and NAND gates from various logic families. Measurements with an antenna mounted 3 m away from a test board on an open-field test site showed significant behavioral differences, as illustrated in Fig. 11. A logarithmic increase in the amplitude of emissions with clock frequency is shown in [28].

Constant increases in IC complexity require packages with higher pin density and broader bandwidth. However, packages also influence noise emissions due to their inductive behavior, in particular, when heat sinks are applied.

Comparative studies were published by Slattery *et al.* [29], regarding 8- and 16-bit microcontrollers, that characterized the impact of IC technology, packaging, and temperature on the spectrum. Emission levels of programmable components like microcontrollers are also influenced by the embedded software. Publications from Fiori and Musolino [30] and Mutoh *et al.* [31] investigated the influence of software on EMI and showed that operating different programs induces variations in the emission spectrum. Slattery *et al.* also used TEM mode cells [32] to compare the emission characteristics of several microprocessors.

3) Reduction of Parasitic Emissions: Several strategies have been proposed for reducing the parasitic noise emitted by ICs. The main strategy, effective for both conducted and radiated

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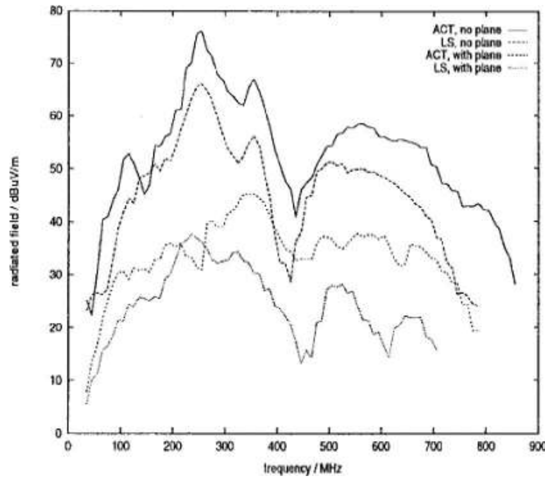

Fig. 11. Radiated far-field emissions produced by simple ICs for various technologies [27].

emissions, consists in controlling the impedance of the supply path under target specifications [33] by reducing parasitic inductances, applying adapted supply strategies, or including decoupling capacitors. Sudo [34] showed that package inductances act as filters and decreasing package inductance contributes to the amplitude of reductions in power/ground voltage drops. However, this strategy is inefficient for reducing radiated emissions. Kim *et al.* [35] presented TEM cell measurements of complex processors with and without local decoupling capacitors. The most popular strategy is the use of onboard and on-chip decoupling capacitors. The measured benefit of on-chip decoupling capacitors compared to off-chip capacitors was significant, especially above 100 MHz, as shown in Fig. 12.

Several works were published soon after [36] and [37], which confirmed that implementing large embedded capacitors, with values from 1 to 50 nF, was a very effective way of reducing emissions. Efficient techniques for implementing on-chip capacitance consist in placing on-chip decoupling on top of each VDD and VSS power rail for maximum coupling effect, and connecting junction capacitance in the free area underneath the routing channels [38]. Thin-oxide gate capacitance or metal–insulator–metal (MIM) capacitance may be used to generate high-value capacitance (several nanofarad). Hayashi and Yamada [39] produced several test chips in order to validate methodologies for predicting SSN amplitude. These test chips used different strategies to reduce parasitic emissions: on-chip decoupling, small serial resistors on power/ground supply rails, and separated supply for the core and I/Os. They showed that applying these strategies simultaneously is the most effective way to reduce noise. This principle was reused by Vrignon *et al.* [40] in the Cesame test chip. Their objective was to test the effect of different design techniques aimed at reducing noise, such as adding a local on-chip decoupling capacitor, adding a resistor on the power supply rails, using a power supply grid, and bulk isolation. Moreover, for the first time, on-chip current sensors were implemented within the test chip to probe the internal noise profile. They demonstrated the positive impact of

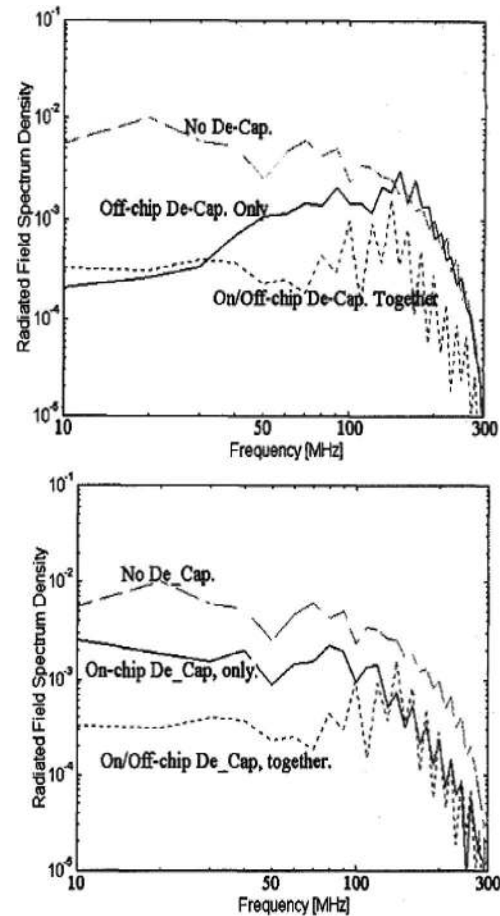

Fig. 12. Effect of off-chip and on-chip decoupling capacitors on the emission spectrum [35].

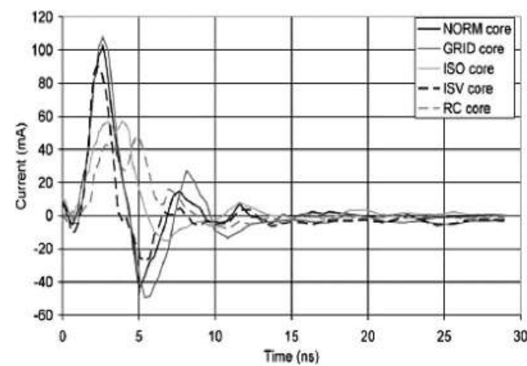

Fig. 13. Effect of different routing strategies on supply noise [40].

added on-chip capacitance and serial resistors, as illustrated by Fig. 13.

An interesting alternative to decoupling capacitance for future ICs that exhibit large current transients is the local reduction of voltage drops through the implementation of distributed voltage regulators close to noisy blocks, as proposed by Budnik and Roy in [41]. This helps to regulate more tightly the operational supply voltage. Fig. 14 presents the supply voltage drop in a 45-nm implementation either with a conventional on-chip decoupling network, or with a different kind of an on-chip regulator. This

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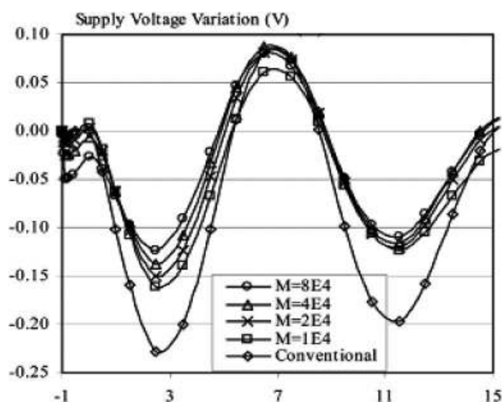

Fig. 14. Supply voltage drops in a 45-nm implementation either with a conventional decoupling network or distributed on-chip regulators [41].

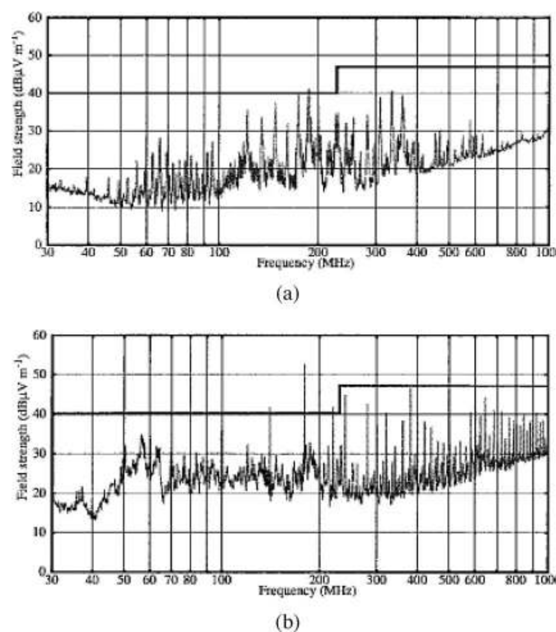

Fig. 15. (a) Asynchronous processor compared to (b) synchronous ARM60 processor [45].

new technique can reduce the voltage drop by 60% compared to conventional decoupled networks.

Parasitic emissions of ICs come from two main sources: I/Os and digital synchronous cores. As the number of I/Os increased, I/O noise became a major issue and many innovative solutions have been proposed to reduce it. For example, Takashima *et al.* [42] and Stan and Burleson [43] proposed a new bus architecture called the partially inverted data bus to reduce the number of simultaneous switching lines. Many publications can also be found in the literature, including the work of van Wershoven [37], who showed that active slew rate control on I/O could further reduce the high-frequency content of radiated emissions.

Noise from digital circuits is related to the synchronous nature of their core. One strategy to reduce the emissions of synchronous circuits consists in controlling the waveform of clock signals to modify the spectral content or spread the dynamic current consumption. Hardin *et al.* [19] were among the first to propose the idea of reducing peak emissions from the core in the harmonics of the clock frequency by fluctuating the clock period in a controlled manner. This same principle can also be reused to reduce the noise generated by I/Os. In some digital designs, the clock frequency is modulated and typically deviates from its fundamental frequency by 0.5%–2%. For example, with an 800-MHz fundamental clock, the bandwidth occupied will be 16 MHz, and at the third harmonic (2400 MHz), the occupied bandwidth will be 48 MHz, which has the same bandwidth as wireless communication systems [e.g., Universal Mobile Telecommunications System (UMTS)]. Such entire wireless communication bands—Bluetooth, zigbee, wireless local area network (WLAN), etc., at 2400 MHz—were blocked when using spread spectrum techniques. As clock frequencies went up further, these in-band issues disappeared.

In complex ICs, not all on-chip functionality is needed simultaneously. As a result, clocks may be disabled to minimize power and/or eliminate leakage currents [44].

An interesting alternative to IC core noise reduction may be found in asynchronous design. While electrical activity is only concentrated on clock edges for synchronous circuits, asynchronous design allows the electrical activity to be spread in time. This key intrinsic property suggests that asynchronous circuits generate lower EM emissions than synchronous circuits, even if they use a larger number of active gate circuits. Furber *et al.* published results [45], presented in Fig. 15, showing a significant reduction of the peak harmonic (near 180 MHz) as well as high-frequency harmonics in the asynchronous design version of the ARM60 processor. An important reference for the asynchronous design technique is Sparso and Furber's book [46]. New methodologies that aim to minimize the parasitic emission of asynchronous circuits have been recently proposed in the literature [47].

System-in-packages (SIPs) allow better and faster integration of electronic systems and provide an interesting alternative to system-on-chip (SOC) for enhancing isolation from noise in a mixed-signal circuit [48]. From the EMI point of view, interconnection lengths and parasitic inductances of packages are reduced in SIP, which contributes to decreasing both power and ground bounce and radiated emissions. The superior performance of multichip modules (MCMs) or SIPs compared to systems implemented with discrete components is illustrated in [32] and [49]. Moreover, SIP offers the possibility of integrating an on-package decoupling capacitor with high values and high-quality factors [38] or specific filters such as EM band gaps [50].

Reducing radiated emissions can also be achieved by applying absorbent material directly on the board or package level. Soo-Hyung *et al.* analyzed the impact of absorbent materials laid on top of a package [51], such as ferrites mixed with epoxy, and observed a 3–20 dB reduction in the emission spectrum envelope, especially beyond 300 MHz.

Alternative methods [52] have also been provided at EMC Compo 2005 dealing with optimization techniques for minimizing *IR* drop and supply bounce.

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4) Emission Prediction: Advances in emission modeling arose in the late 1990s, corresponding to a period of unprecedented pressure from IC customers demanding low-emissive components. The combination of leading-edge technology and tremendous time-to-market demands gave rise to huge efforts in component modeling, including signal and power integrity, to avoid costly redesigns. Embedded processors for automotive applications evolved in a competitive battle to produce low-emission microcontrollers while operating clock frequencies close to the gigahertz range.

A significant research effort was dedicated to the prediction of power integrity and parasitic emission in large-scale circuits at early design phases. The main difficulty to solve was the complexity of a full-chip analysis, which includes the circuit netlist, the power distribution network, and the package and board models.

McCredie and Becker [53] successfully modeled the switching noise of an application-specific IC (ASIC) mounted on a compact ball grid array (BGA) with around 1000 I/O pins using distributed current sources, on-chip and on-package decoupling capacitance models as well as serial connection inductances. In 1995, Goodman *et al.* [54] published the results of a comparison between measurements and simulations of signal propagation in PGAs, and demonstrated various deleterious effects on signal transmission depending on the geometry of the package pins. While using discrete *RLC* components to model package leads, bonding, and integrated I/O structures, they used transmission lines for the PCB tracks to validate their models up to 4 GHz.

Chen and Neely [55] proposed and described a hierarchical power supply distribution model containing a 12×12 flip-chip package, a 50×50 on-chip power bus, and a distributed switching circuit model. They performed a full-chip switching noise analysis including the inductive ΔI noise and the resistive *IR* noise. One advantage of their methodology is the production of voltage drop distribution maps at the surface of the chip for identification of the noise source and optimization of design variables to minimize the noise, as shown in Fig. 16.

Hayashi and Yamada [39] reused this methodology to predict not only the SSN but also the conducted power-line EMI noise, and applied it to four test chips with different on-chip decoupling capacitance values. Zhao *et al.* [56] developed a similar methodology to investigate the problem of on-chip decoupling capacitance allocation at the floor plan level and succeeded in reducing the peak power supply noise by 40% while the decoupling area was reduced by 20%. More recently, Steinecke *et al.* [57] presented a set of tools called EXPO and NEMO dedicated to predicting power integrity, power-domain crosstalk, and EMI noise either at floor-planning or prelayout stage.

C. Research Studies Related to Susceptibility of ICs to EMI (1996–2009)

Many research studies published during the period 1996–2009 focused on the characterization of IC immunity to RF disturbances, mostly from 1 MHz to 1 GHz. Research into immunity faced several issues, such as expensive and time-consuming measurement setups, modeling approaches that were much more complex than for emissions, and the difficulty in observing and evaluating the real impact of external perturbations on complex ICs. This section includes selections that deal with the effect of RFI on circuits, susceptibility characterization, prediction, and guidelines for improved immunity.

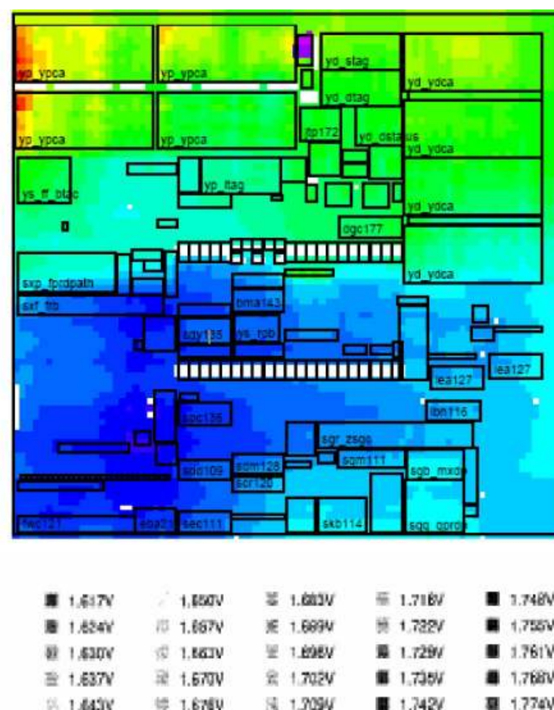

Fig. 16. Simulation of on-chip voltage drop distribution [55].

1) Effect of RFI on Circuits: EMI has various effects on circuits that exhibit different sensitivity levels. The effects of EM wave coupling to PCB traces and the consequences of this coupling on simple circuits were analyzed by Laurin *et al.* [58]. With field strengths as high as 200 V/m, no disturbance was observed on the component. Adding a metal wire that was a half-wavelength long at the interference frequency resulted in fields as low as 2 V/m causing severe malfunctions due to erroneous switching. The authors differentiated between the static and transient regimes. In the static regime, only high-energy perturbations affected logic levels, while even weak perturbations could affect switching delays and circuit thresholds in the transient regime. An 8-bit microcontroller was disturbed in a TEM cell in [59]. While memory devices required fields as high as 275 V/m to be corrupted, significant changes in quiescent currents appeared above 70 V/m. However, these amplitudes remain much larger than the ambient fields that are expected in a typical electronic product environment.

While the demand for mobile communications was exploding, the behavior of ICs in the presence of gigahertz range interference was not being extensively studied. In 2000, an updated version of the 1978 McDonnell Douglas Astronautics Company *Integrated Circuit Electromagnetic Susceptibility Investigation Handbook Phase III* [8] published by the National Aeronautics and Space Administration (NASA) gave valuable information on the immunity levels of simple ICs up to 10 GHz [60]. It

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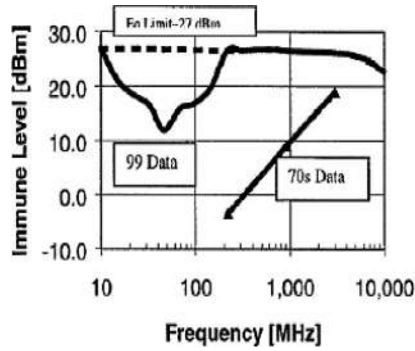

Fig. 17. Immunity of two generations of a NAND gate 74LS00 [60].

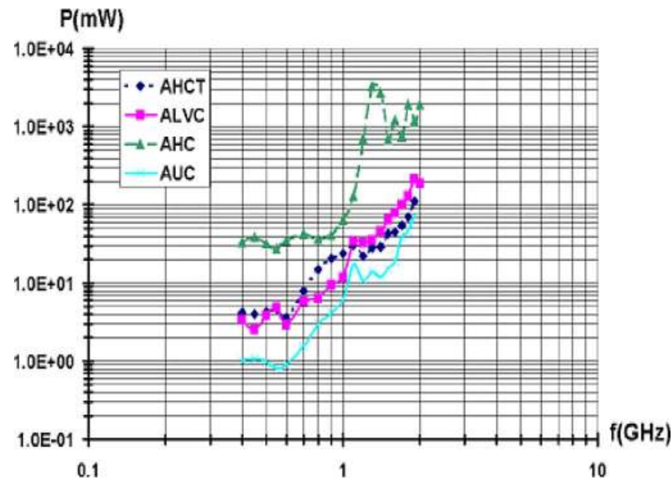

Fig. 18. Susceptibility comparisons between different CMOS technologies [61].

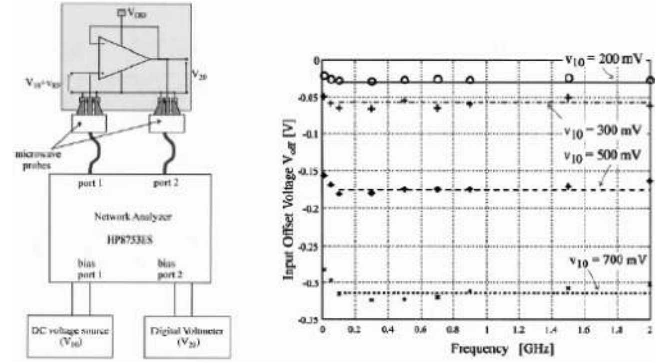

Fig. 19. Response of an operational amplifier to 100 MHz–2 GHz RFI using microwave on-chip probing [62].

presented measurement results for simple components along with a very interesting comparison to similar measurements performed in the early 1980s. Like the results shown in Fig. 17, the immunity level of recent components proved to be higher than those 1970s versions, which could be explained by the improvement in I/O protection.

A comparative study was done in [61] on different families of CMOS inverters mounted within different types of package on the same test board. Conducted aggressions were performed on a selection of inverters within the frequency range 400 MHz–2 GHz. The results showed that technology induces disparities between the susceptibility levels of the different families, mostly linked to the amplitude of noise margin. The results also showed that the influence of the package is not significant. Finally, a trend toward immunity increase with frequency was observed, as shown in Fig. 18.

Susceptibility issues not only concern digital circuits but also analog components, which are often more sensitive to RFI. Fiori and Crovetti [62] published a study relating to RFI on analog amplifiers up to 2 GHz. The measurement setup employed microwave probes positioned directly on the chip so as to maintain a 50-Ω impedance correspondence from the measurement equipment to the IC. They observed increased dc shifts in the amplifier voltage offset with the RFI amplitude without significant frequency dependence from 100 MHz to 2 GHz, as shown in Fig. 19.

Although SIP technologies allow a significant reduction in the parasitic inductance of interconnections and enable the integration of high-quality decoupling capacitors, embedding heterogeneous ICs causes several couplings for noise produced by high-speed digital parts to sensitive blocks like analog or RF [63]. The noise propagates mainly by the power distribution network through interconnections and vias at resonance in the package's power/ground planes [64]. The same type of internal parasitic paths exists in mixed-signal SOCs [65].

2) Susceptibility Characterization: Standard measurement methods have been developed to characterize the immunity of components. Susceptibility characterization often needs complex setups, and extracting the actual immunity of a component is not a trivial process. Moreover, susceptibility setups have to reproduce realistic disturbances in terms of level, waveform, or coupling to the circuit. Thus, many publications were proposed during this period that aimed to improve the susceptibility setup.

Flintoft *et al.* [66] proposed measuring the reemitted spectrum of disturbed components to probe the susceptibility of a digital circuit. The nonlinear effects (e.g., cross-modulation products) due to the disturbance could be detected in the reemission spectrum before appearance of any static failures, which allowed blocks responsible for failures to be identified. Radiated susceptibility tests depend on a large number of parameters, such as the direction of the incident field or its polarization because of all the shielding enclosures of electronic equipment. A new test method using slowly rotating EM fields was proposed in [67] to determine the most sensitive orientation causing a failure.

Before the nineties, most publications relating to susceptibility of ICs referred to harmonic disturbances. However, circuits in electronic products are subjected more to transient disturbances, and a large variety of impulsive interference is generated in modern electronic applications. Therefore, researchers and engineers began to study the effect of transients on the susceptibility of CMOS devices [68]. Camp and Garbe [69] observed that transient immunity tends to decrease as technology progresses (see Fig. 20). Reasons might be the decreased noise margins, the clock frequency, or the increased complexity of the IC.

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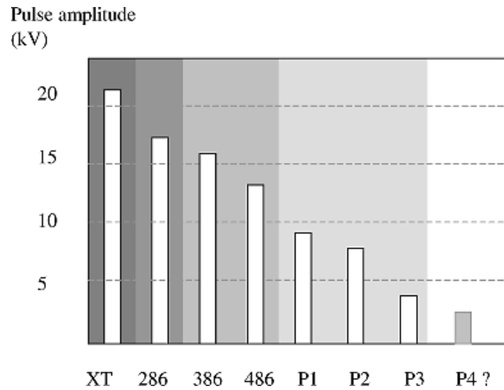

Fig. 20. Immunity to transients tends to decrease with computer generation [69].

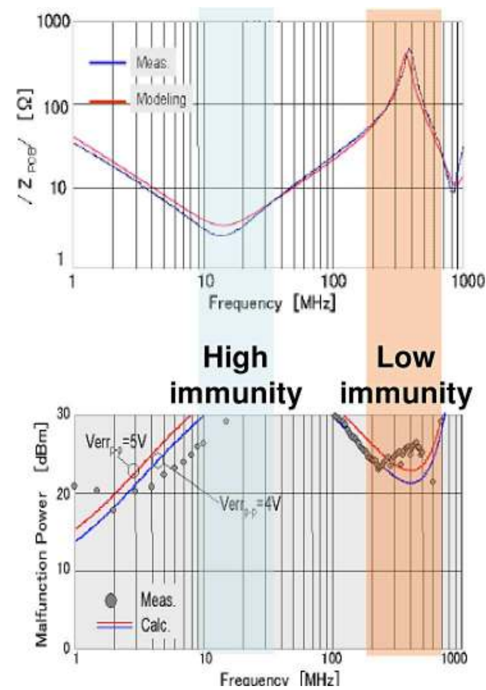

Fig. 21. Immunity prediction of a microcontroller and link between the susceptibility threshold and the impedance profile [78].

Transient immunity setups are often complex due to the need to synchronize the device under test and the applied stress. Indeed, the authors in [70] and [71] showed that susceptibility of synchronous components is time-variant and depends on the delay between the appearance of the transient and the clock edges. Synchronous devices are most susceptible to impulsive disturbances within a small time window prior to the clock edge. Wendsche *et al.* [71] and Bakshi and Coenen [72] developed an immunity test setup that aimed to stress the device under test during a defined time window in order to identify the most susceptible time window. The latter was published as IEC 62215-2.

3) Susceptibility Prediction: Simulation of susceptibility is more challenging than emission prediction. The complexity of the injection path model and the circuit netlists and the huge computational time required for iterative time-domain simulations are major issues. Several alternatives have been proposed such as the harmonic balance method, described in [73] and applied to simple circuits (single transistor, op-amp). In some cases, the susceptibility of a circuit can be approximated from basic mathematical formulations. For example, the dynamic margin of components due to jitter, which induces variations in signal propagation delays in ICs, used a simple mathematical approach in [74] and [75]. Different behavioral models have been proposed to forecast the susceptibility of simple circuits [76]. With such approaches, a purely mathematical model may predict susceptibility. A neural network built from direct power injection (DPI) measurement data was used in [77] to predict susceptibility of an inverter to harmonic disturbances. Nevertheless, this kind of approach has not yet been used for susceptibility prediction of large-scale circuits.

Ichikawa *et al.* [78] highlighted the correlation between the susceptibility of the power distribution network of a microcontroller and its impedance profile. From this observation, a macromodel of the component was proposed to simulate its susceptibility threshold. Even if the linear equivalent circuit and current source (LECCS) model used by the authors was initially proposed to model the conducted emissions of a circuit, the susceptibility threshold was successfully reproduced, as shown in Fig. 21.

The LECCS model has been used for prediction of radiated emission related to power bus resonance [79]–[81] and also to immunity [82].

A macromodel dedicated to emission prediction based on IC emission model (ICEM) [84] was used in [83] to predict the immunity of a microcontroller. The ICEM approach was reused in [85] to perform self-susceptibility. A behavioral model of a sensitive analog block was coupled with the ICEM model of a noisy digital part. The susceptibility threshold was successfully predicted and improvements were justified through this predictive approach.

4) IC Immunity Improvements: Despite the difficulty of forecasting IC susceptibility, many guidelines have been proposed to improve immunity of ICs. Chappel and Zaky [86] discussed the possibility of hardening ICs to EMI through specific design techniques such as Schmidt triggers, low-voltage differential swing (LVDS), and delay-insensitive structures, which raised the immunity level of circuits from a low 1.5 V to more than 5 V, in the frequency range 1–10 MHz (see Fig. 22).

Typically, circuits are more sensitive to delay variations than voltage variations. Therefore, asynchronous circuit design also offers an interesting alternative for improving susceptibility. Bouesse *et al.* [87] compared the susceptibility of different versions of a crypto processor either in a synchronous or asynchronous version. Fig. 23 presents the susceptibility comparison of synchronous and asynchronous versions of the same circuit implemented in different technologies. The asynchronous version in 0.18 μm provides a gain of 10 dB above 200 MHz. Moreover, the 0.13-μm version of the asynchronous processor features an immunity improvement of 30 dB from 200 MHz to

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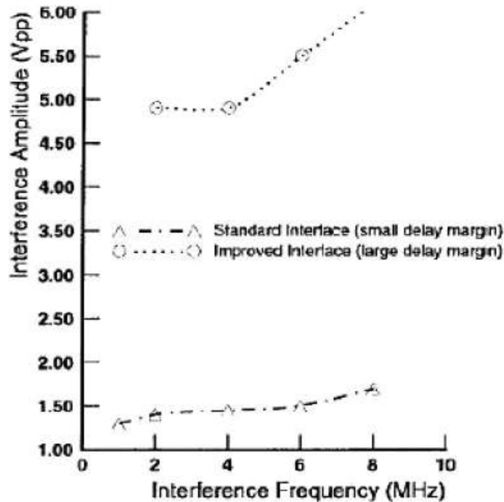

Fig. 22. Two circuits with identical functionality but very different immunity levels [86].

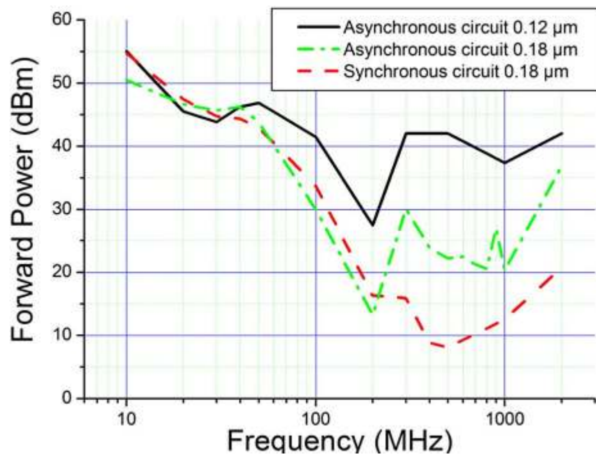

Fig. 23. Measurements of the conducted susceptibility of synchronous and asynchronous versions of a crypto processor [87].

1 GHz and demonstrates the robustness of asynchronous designs toward high-frequency interference.

In 2007, Alaeldine *et al.* [88] showed that adding on-chip capacitance was also an efficient solution for improving IC immunity. They compared the susceptibility to DPI aggression of several digital cores that differed from their routing strategy. As shown in Fig. 24, experimental results demonstrated that the core with the local on-chip capacitance had the greatest immunity.

The immunity of programmable circuits like microcontrollers depends directly on their microinstruction sets [89]. Through experience gained on a variety of microprocessors and microcontrollers, some engineers started developing strategies for hardening microprocessors through appropriate code optimization. In 1997, Coulson [90] identified the vulnerable points and proposed specific circuits such as supply supervisors, watchdogs, and software-based techniques such as memory integrity checking, token passing, and redundancy coding. Ong and Pont [91] studied the effect of software-based techniques on the reliability

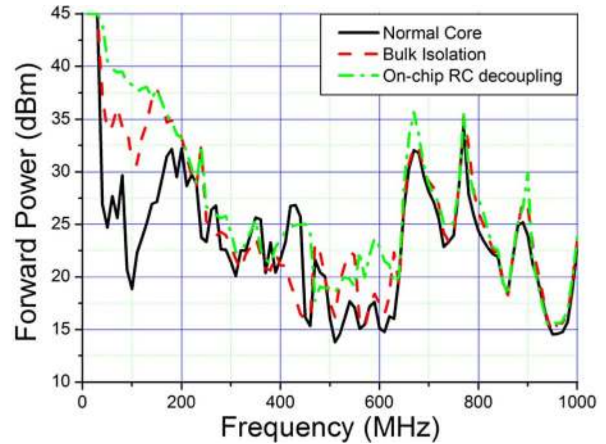

Fig. 24. Comparison of the susceptibility thresholds of three digital cores with different routing strategies [88].

of embedded applications in the presence of EMI. The defensive software approach based on function tokens was found to be inefficient and not generally applicable. In contrast, the implementation of no-operation [NOP, or jump to zero (JZ)] fills in unused memory proved to have a positive impact on system reliability.

Much work has been published on the design of an EMI-robust operational amplifier, which is a fundamental block of analog devices. Richelli *et al.* [92] published a paper about a new approach to designing an EMI-robust CMOS operational amplifier. The proposed amplifier was based on a fully differential folded cascode for the input stage and a symmetrical output buffer [93]. Fiori published several papers on the design of op-amps immune to EMI, such as [94], and tried to find architectures that aimed to attenuate the amplitude of interference reaching sensitive nonlinear devices, using compensation networks or double differential pairs.

D. Summary

In order to respond to ever more constraining EMC regulations, researchers and engineers have made a continuous effort to develop innovative techniques for making circuits EMC compliant. Table II sums up the main design techniques used to reduce parasitic emissions and improve immunity of circuits, with their respective advantages and drawbacks.

IV. Standardization in IC EMC

EMC test setups for automotive electronic systems are defined in standards such as the International Special Committee on Radio Interference (CISPR) 25 [95] for parasitic emissions and International Organization for Standardization (ISO) 11452 [96] for susceptibility to EMI. ICs are often the main cause of disturbance in electronic equipment. In recent years, there has been considerable demand for simple, reliable, and standardized measurement methods focusing only on ICs that electronic system designers could use to:

1) select components based on their low emission performance and high immunity to EMI;

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TABLE II
CURRENT TECHNIQUES USED TO REDUCE PARASITIC EMISSION AND/OR IMPROVE IMMUNITY OF ICs

Reduction techniques of emission or susceptibility	Features	Advantages	Drawbacks
External decoupling capacitor	Implementation of on-board capacitance	Low cost technique to reduce parasitic emission and susceptibility [33]	Efficient up to several hundred MHz off-chip [35]
On-chip decoupling capacitance	Implementation of large embedded capacitance (1 – 50 nF) [39] [40]	Efficient above 100 MHz [33]	Occupies a large silicon area and effective at RF
Reduce package inductance	Use of low inductance package and leads in parallel [34]	Reduction of power and ground voltage bounce	Package cost at higher transfer bandwidth
Power grid	Reduction of impedance of power distribution network [40]	Reduction of power voltage drop	Noise propagation not attenuated
Placement routing	EMC aware placement and routing	Isolation of sensitive blocks from noisy blocks	
Clock disable function	Disables clock on unused blocks [44]	Reduction of clock emission	Complex cell
Spread spectrum clocking	Adds controlled jitter to clock signals [19]	Reduction of emission spectrum amplitude	Limited to several % of duty cycle Complex cell
Slew rate control	Control of the I/O slew rate [37]	Reduction of high frequency contribution of I/O noise amplitude	Complex cell
Bus architecture	Bus management to lower the number of simultaneous I/O switchings [42] [43]	Reduction of I/O noise	Difficult to implement in CAD tools
EM absorbing materials	Adds thin layer of ferromagnetic materials [51]	Reduction of radiated emission	Inefficient for conducted emission reduction Limited frequency efficiency
Robust digital input	Adds structures like Schmitt trigger or differential stages [86]	Improvement of immunity of digital I/O	Complex design
Robust analog input	Improves the structure of analog input stages [92] [93] [94]	Improvement of immunity of analog circuits	Complex design
Defensive software	EMC hardening of programmable components [90]	Efficient in improving immunity of I/Os and ensuring memory integrity [91]	
Substrate isolation	Uses low doped substrate, guard rings and isolation well to reduce noise propagation through substrate [65]	Reduction of interference issues in mixed signal circuits	Latch-up risks with low doped substrate Noise injection by power supply of isolation structure

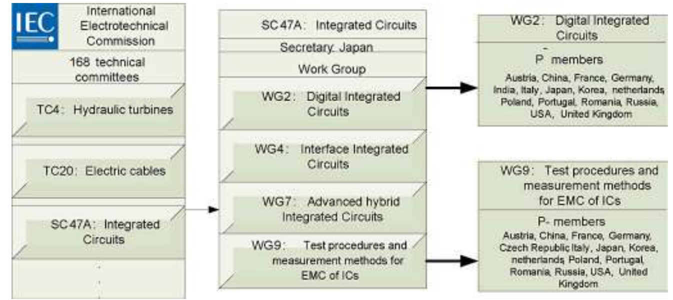

Fig. 25. Structure of IEC working groups for EMC of ICs.

2) define optimum filtering and decoupling components to be added to PCBs close to the active component;
3) optimize IC placement and routing to fulfill EMC specifications at equipment level;
4) evaluate the impact of IC redesign, technology improvement, or package modification.

Component-level measurement methods are different from those used at the system level, because they have to take into account the high complexity and the small size of ICs. They need to characterize the IC itself separate from its environment. The IEC has established a specific subcommittee in 1996, 47A, working on ICs (see Fig. 25). In 1996, the working group 9, which focused on measurement methods for ICs, has worked steadily to establish low-cost, easy-to-use, and reliable methods for characterizing the EMC performance of components. This working group has released two major standards, one for radiated and conducted emissions under project number IEC 61967 [97], and more recently, a second one for RF immunity under project number IEC 62132 [98].

The immunity standard IEC 62132 is only devoted to the characterization RF disturbance immunity. Electrical fast transients (EFTs) have become a very common type of interference generated in modern electronic applications. The purpose of the new standard proposal IEC 62215 [99] is to specify methods for characterizing the impulse immunity of circuits.

The demand for standardization in IC EMC does not only concern measurement methods but also modeling methodologies. In 1997, the IEC created a new task force (working group 2) to extend the modeling and simulation requirements of the electronic industry to the IC domain.

A. *Measurement Standard for IC Emissions*

The IEC 61967 standard [97] was originally dedicated to IC EM emissions up to 1 GHz, and now the frequency range is extended above 1 GHz. It contains six parts and some additional parts are planned to be proposed as detailed in Table III. Fig. 26 illustrates the measurement methods defined in the standard. It can be seen from Table III that five parts have already been completed, while two subparts have the status of "New Proposal" in 2009, and one is still a "Technical Specification."

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TABLE III
ROADMAP FOR STANDARD IEC 61967—MEASUREMENT OF IC EM EMISSIONS

Standard	Description	Stage in 2009
IEC 61967-1	General conditions and Definitions	International standard
IEC 61967-2	TEM/GTEM cell	International standard
IEC/TS 61967-3	Surface scan	Technical specification
IEC 61967-4	1/150 Ω conducted	International standard
IEC 61967-5	Work Bench Faraday Cage (WBFC)	International standard
IEC 61967-6	Magnetic probe	International standard
IEC 61967-7	Mode Stirred Chamber	New proposal (planed)
IEC 61967-8	IC strip-line	New proposal (to be published)

B. Measurement Standard for IC Immunity

The standard IEC 62132 [98] is dedicated to IC susceptibility to RF. The frequency range was originally up to 1 GHz and recently it was extended above 1 GHz. At present the standard contains four to five parts and some additional methods have been proposed as detailed in Table IV. Fig. 27 illustrates these measurement methods. There are some similarities with the emission standard in the structure of the document, since the TEM cell and the workbench Faraday cage (WBFC) method have been proposed for both emission and susceptibility characterization. The roadmap for standardization of susceptibility measurement methods (Table IV) is shifted in time compared with the emission roadmap. The most mature susceptibility measurement methods are the WBFC and DPI approaches.

While transient environments and test methodologies at the product level are well defined and understood, the equivalent environments and methodologies for ICs are still undefined by national or international standards. As a result, work is in progress within the IEC and elsewhere to define a transient immunity environment and test methods that are suitable for the evaluation of ICs, under project number IEC 62215 [99], entitled "Integrated circuits—Measurement of impulse immunity." The standard intends to cover transient immunity to impulses, electrostatic discharge (ESD), EFTs, and electrical overstress (EOS). This standard reuses some test methods defined in the standards IEC 61000-4-4 [100] and ISO 7637-2 [101]. An interesting overview of all these standards was given in 2004 by Carleton [102]. Table V presents the roadmap for standardization of these measurement methods.

C. IC Modeling

The first important contribution to standard EMC modeling originates from the I/O buffer information specification (IBIS) working group that proposed a standard aimed at describing the electrical performance of I/O structures of ICs [103]. The IBIS format was originally developed by INTEL engineers. Since 1993, the group called IBIS Open Forum, affiliated to the Electronic Industries Alliance (EIA), has continued to improve and update this standard through several versions [104]. An important feature of IBIS is the description of package and I/O characteristics that are of first-order importance for EMC simulation. Fig. 28 presents the structure of input and output described according to the IBIS specification. The most important keywords relating to EMC are listed in Table VI.

Initially, IBIS only focuses on signal integrity at the I/O level and does not provide any information about noise within the IC core. Only an ideal peripheral power supply was considered. From version 4.1 onwards, EMC is also served for I/Os. In 1997, the French standardization committee, "Union Technique de l'Electricité" (UTE), focused on EMC modeling of components and developed a generic model for IC parasitic emission prediction called ICEM. In 2002, ICEM appeared as a new IEC proposal standard IEC 62014-3 [84], [105]. Simultaneously, the Japanese proposition called I/O interface model for IC (IMIC) was also adopted as IEC 62404 [106]. These different works, propositions, and technical documents provided the foundations for a new standard proposition IEC 62433 [107], [108]. This generic standard aims to evaluate the EM behavior [conducted, radiated emission, as well as susceptibility; IC immunity model (ICIM)] and performance of ICs. Fig. 29 presents the generic structure of the conducted emission model ICEM conducted emission (CE) [103]. Table VII sums up the different IEC standards dedicated to the modeling of EMC at IC level.

The main challenge that EMC engineers face for the future is how to develop test and modeling methods capable of handling billion-device ICs in an ever more complex EM environment, without incurring prohibitive costs and time penalties.

D. Summary

Prediction of EMC performance becomes necessary to ensure EMC compliance of circuits before manufacture. Table VIII reviews the most widely referenced EMC modeling methods.

V. GLOBAL TRENDS IN SEMICONDUCTOR TECHNOLOGY

In this section, the global trends in semiconductor technology are illustrated with a focus on the evolution of key parameters that have a direct influence on EMC. The International Technology Roadmap for Semiconductor (ITRS) [109] provides very detailed insight into the evolution of the microelectronics industry, highlighting trends, technology targets, and milestones for the next 15 years. This prospective roadmap is probably one of the most referenced documents in the microelectronic industry. A less known roadmap focuses on design automation tools with a chapter related to EMC [110]. From these roadmaps, we have extracted a subset of parameters and associated trends for more detailed presentation. In particular, we focus on the processor frequency, switching currents, I/O trends, and the evolution of the noise margin.

A. Technology Scale-Down

With each lithography scaling step, the linear dimensions are reduced approximately by a factor of 0.7 such that the silicon area is reduced by a factor of 2. Smaller cell sizes lead to higher integration density and a lower silicon cost per device. By 2022, the ITRS roadmap projects the minimum physical gate length of

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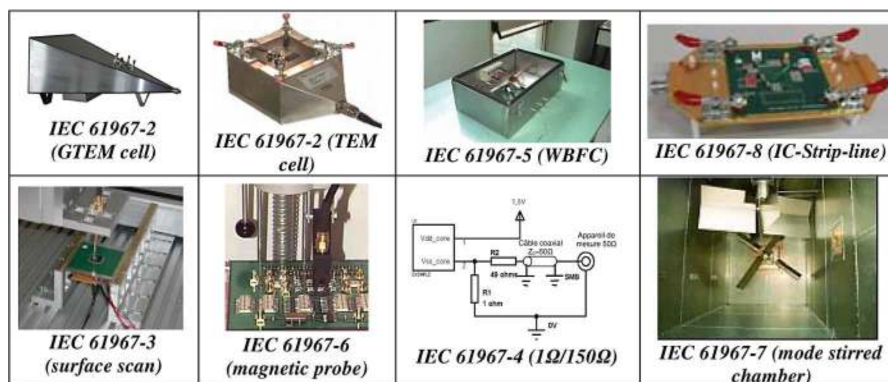

Fig. 26. Measurement methods related to the IC emission standard IEC 61967 [97].

TABLE IV
ROADMAP FOR STANDARD IEC 62132—MEASUREMENT OF IC SUSCEPTIBILITY

Standard	Description	Stage in 2009
IEC 62132-1	General Conditions and Definitions	International standard
IEC 62132-2	TEM-Cell and Wideband TEM-Cell Method (GTEM)	Committee draft for voting
IEC 62132-3	Bulk Current Injection (BCI)	International standard
IEC 62132-4	Direct RF Power Injection (DPI)	International standard
IEC 62132-5	Work Bench Faraday Cage (WBFC)	International standard
IEC 62132-6	Local Horn Injection Antenna (LIHA)	New proposal (to be published)
IEC 62132-7	Mode Stirred Chamber	New proposal (planed)
IEC 62132-8	IC Strip-line	New Proposal (to be published)
IEC 62132-9	Near Field ScanImmunity (NFSI)	New proposal (planed)

transistors to be close to 7 nm (see Fig. 25), which is considered by most researchers to be the physical limit of silicon.

Over the coming decade, the number and variety of potential sources and victims of disturbance are set to increase exponentially. This will lead to an astronomical increase in the risk of interference with system integration.

Fig. 30 presents the technology nodes used for manufacturing microprocessors and microcontrollers, with prospects until 2020. Two trends are shown, one relating to high-end processors and the second relating to cost/performance microcontrollers. It can be seen that the embedded microcontrollers use technologies nearly five years after their introduction in high-end microprocessors.

B. Ever Faster ICs

One very important trend associated with lithography scaling is the decrease in the gate switching delay, due to sustaining driver currents, capable of charging and discharging smaller parasitic capacitances, shorter wire lengths, and lower gate capacitance. According to ITRS 2007, the on-chip clock frequency is increasing (14 GHz predicted for 2012) as well as the communication speed between chips, e.g., with an SIP. To reach these higher speeds and reduce power requirements, ICs are designed with transistors that require less supply voltage (0.5 V in 2022) to lower the power consumption. As logic thresholds reduce accordingly, the noise margin is going down, resulting in more vulnerability to EMI.

By 2022, processors are expected to run at 20 GHz, as shown in Fig. 31. From a frequency point of view, a difference may be seen between high-performance microprocessors and microcontrollers. The saturation scenario considers several limiting factors such as MOS mobility degradation, interconnect delay, and power dissipation. Parallel architectures may compensate for these limitations while maintaining the pace in performance improvements.

The frequency increase also concerns the data transfer between ICs, as shown in Fig. 32. Universal Serial Bus (USB), Peripheral Component Interconnect (PCI), and serial Advanced Technology Attachment (ATA) protocols have been developed to operate around 1 GHz while new protocols approaching 10 GHz have been specified with an increased bandwidth to support ultrahigh-speed data transfer.

C. More Switching Noise

A regular decrease in the average gate switching current with the technology scale-down can be observed in Table IX [109]. Intrinsically, this should have a positive impact on the transient switching noise. However, the steady increase in IC complexity, power consumption, and faster switching speeds jeopardizes these benefits in terms of di/dt noise. Moreover, the increase in gate density associated with the increase in interconnect density leads to the use of gates with a huge fan-out [111] that tends to increase the total peak current, as shown in Fig. 33. The main advantage is that not all circuit gates will act simultaneously dependent upon required operation. Dedicated ICs are designed with a single functionality, but, already today, as with future designs, overall block activity level will be 30% or less (and accordingly, the power consumption will drop). Due to triple-well techniques in nanometer processes that allow for supply-enabling, the core impedances vary over the modes of operation.

D. Increased Number of I/Os

Starting with 90-nm technology, chips with more than 1000 I/Os may be designed. The simultaneous switching of active buffers may thus be the dominant contributor to parasitic emissions. Fig. 34 shows the evolution of the maximum number of I/Os per chip, which follows a quasi-exponential law [109]. An accurate evaluation of I/O behavior and its transient current consumption are of utmost importance for emission and immunity prediction.

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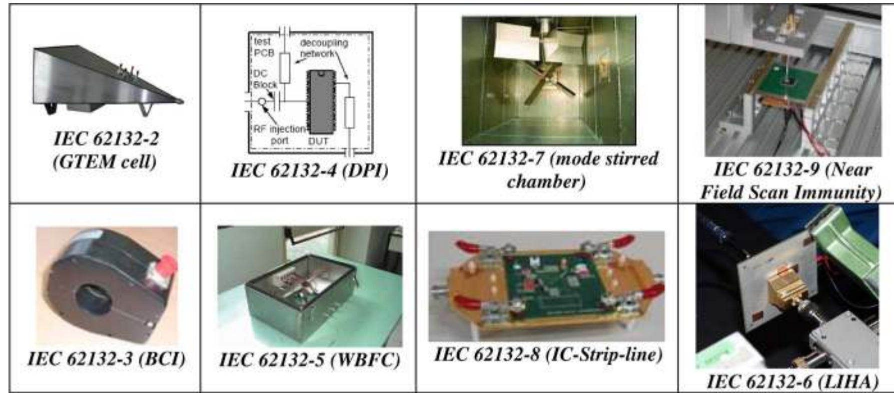

Fig. 27. Measurement methods related to the IC susceptibility standard IEC 62132 [98].

TABLE V
ROADMAP FOR STANDARD IEC 62215—MEASUREMENT OF IC TRANSIENT IMMUNITY

Standard	Description	Stage in 2009
IEC 62215-1	General Conditions and Definitions	New proposal (planed)
IEC 62215-2	Synchronous Transient Injection	Technical specification
IEC 62215-3	Non-synchronous Transient Injection	New proposal (to be published)
IEC 62215-4	Surge	New proposal (planed)
IEC 62215-5	Supply Dips	New proposal (planed)
IEC 62215-6	Near field Scan Immunity	New proposal (planed)

TABLE VI
ROLE OF IBIS IN EMC OF ICS

IBIS feature	EMC Application
R,L,C Package [R_pack][C_pack][L_pack]	Used for definition of the Passive Distribution Network (PDN)
Input protection diodes [power_Clamp] [GND_clamp]	Susceptibility Analysis
Output driver characteristics (static I/V curves, transient simulations) [pullup][pulldown]	Input/Output driver emission
Supply structure for each pin [Pin Mapping]	PDN definition
Pin input capacitance [C_Comp]	Immunity analysis

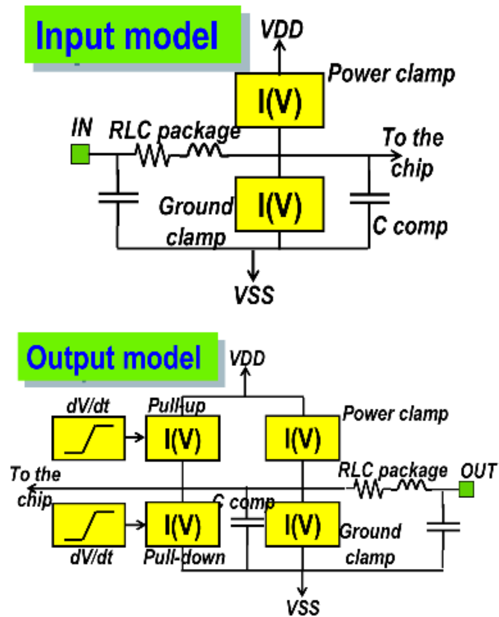

Fig. 28. IBIS model structure [103].

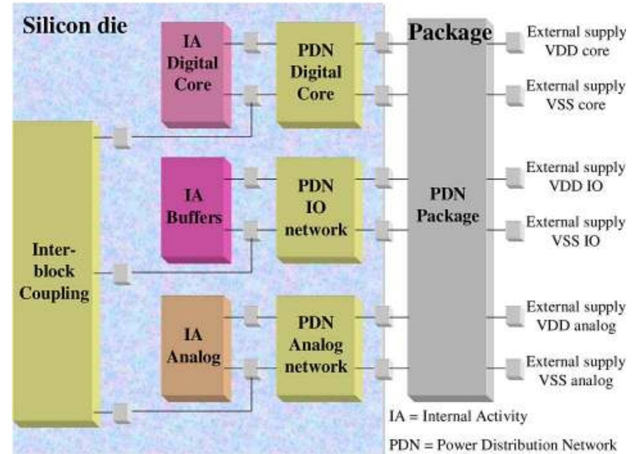

Fig. 29. Generic measurement model for emission prediction given by ICEM-CE (IEC63433-2) [107].

E. Less Noise Margin

An important trend in IC technology is the steady reduction in the power supply. In Fig. 35, three voltage trends are shown: the I/O voltage that tends to be reduced step-by-step (5, 3.3, 2.5, and 1.8 V), the core supply that has constantly decreased from 5 V (0.5 μm node) to around 1 V (45 nm node), and the associated noise margin that has been cut by a factor of 5. The voltage reduction should slow down in future technologies (7 nm node supplied at 0.5 V in 2022), but the noise margin is expected to cross the 100-mV line by 2015. A reduced noise margin means an increased sensitivity to external interference.

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TABLE VII
ROADMAP FOR STANDARDS RELATED TO EMC OF IC MODELING

Standard	Description	Stage in 2009
IEC 62014-1	Input/output buffer information specifications (IBIS) v3.2	International standard
IEC/TR 62014-3	Models of integrated circuits for EMI behavioral simulation – Integrated Circuit Emission Model (ICEM)	Transferred to 62433
IEC/TS 62404	Models of integrated circuits for EMI behavioral simulation - I/O Interface Model for Integrated circuits (IMIC)	Technical specification
IEC 62433-1	EMC IC modeling - General modeling framework	Committee draft
IEC 62433-2	EMC IC modelling- Part 2: Models of Integrated Circuits for EMI behavioural simulation - Conducted Emissions modelling (ICEM-CE)	Committee draft for voting (published as FDIS)
IEC 62433-3	Models of Integrated Circuits for EMI behavioral simulation, Radiated Emission Model (ICEM-RE)	New proposal (planed)
IEC 62433-4	Models of Integrated Circuits for EMI behavioral simulation, Conducted Immunity Model (ICIM-CE)	New proposal (planed)
IEC 62433-5	Models of Integrated Circuits for EMI behavioral simulation, Radiated Immunity Model (ICIM-RE)	New proposal (planed)
IEC 62433-6	Models of Integrated Circuits for EMI behavioral simulation, Impulse Immunity	New proposal (planed)
IEC 62433-7	Models of Integrated Circuits for EMI behavioral simulation, Intra IC Compatibility	New proposal (planed)

TABLE VIII
EMC MODELS

Method	Simulation	Advantages	Drawbacks
IBIS [99]	Signal Integrity	Medium complexity Non confidential data Accurate I/O and package modeling	Limited to 1 GHz Does not handle I/O supply
ICEM [80][104]	Conducted and radiated emission	Low complexity Non confidential data	Limited to 1 GHz Medium accuracy
IMIC [102]	Conducted and radiated emission	Low complexity Non confidential data	Limited to 1 GHz Medium accuracy
Full chip simulation [39][56] [57] [58]	Core noise, SSN Voltage drop distribution	High accuracy Decoupling capacitor allocation	High complexity Time consuming Confidential information

The internal voltage and clock frequency are made dependent upon performances required within the time window available to minimize power, which means that sensitivity has become a function of the mode of operation.

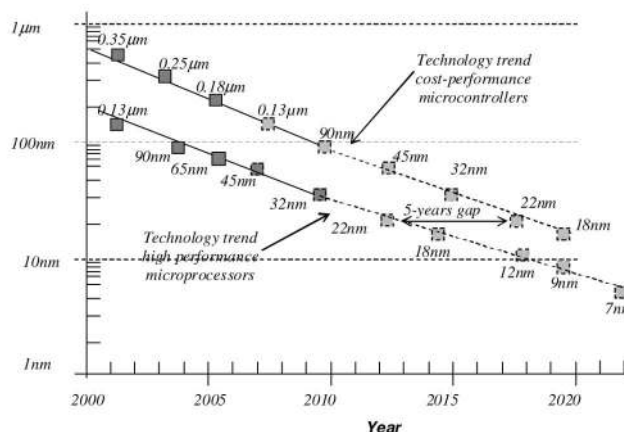

Fig. 30. Technology scale-down toward nanoscale devices associated with microprocessor and microcontroller manufacture [109].

F. Wider Spectrum

A huge number of RF systems operate at frequencies ranging from several kilohertz to nearly 100 GHz. Fig. 36 describes a number of wireless commercial systems operated in 2009. EMC issues rise from the coexistence of many different types

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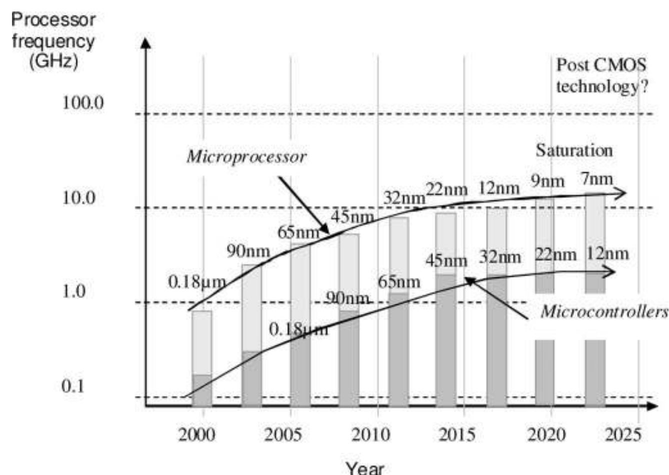

Fig. 31. Microprocessor and microcontroller frequency increase until 2020 [109].

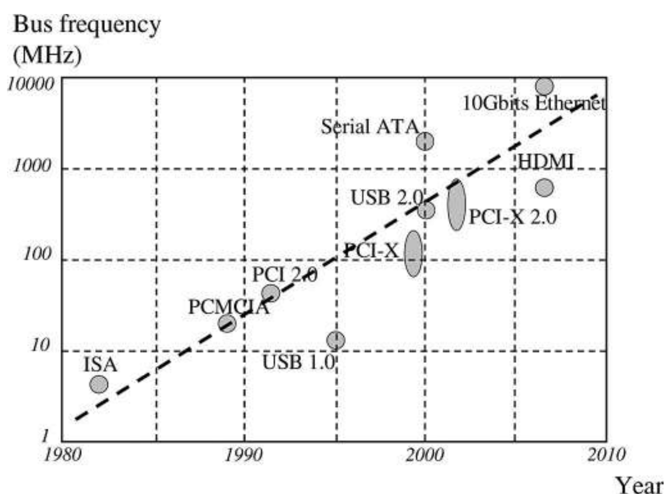

Fig. 32. Frequency increase of data bus transfer [109].

of equipment in the same safety-critical environment such as a car, an airplane, or implanted electronics.

The use of several operating clocks induces a spread of the emission spectrum. Fig. 37 compares the spectrum envelope of two components, one with a single clock $f_0 = 100$ MHz and the other with multiple clocks f_1, f_2, and f_3.

VI. EMC Roadmap

This last part gives prospective scenarios for the evolution of parasitic emissions and the immunity of ICs, as well as roadmaps focusing on standard measurement methods and EMC models.

A. Evolution of EMC Constraints

There is global pressure from IC customers to achieve low emissions. IC designs without EMC optimization suffer from high unintended emissions, and require costly onboard decoupling, protection, and filtering. At the start of this decade, due to low-emission design guidelines, unintended emission levels were reduced, even beyond customer expectations.

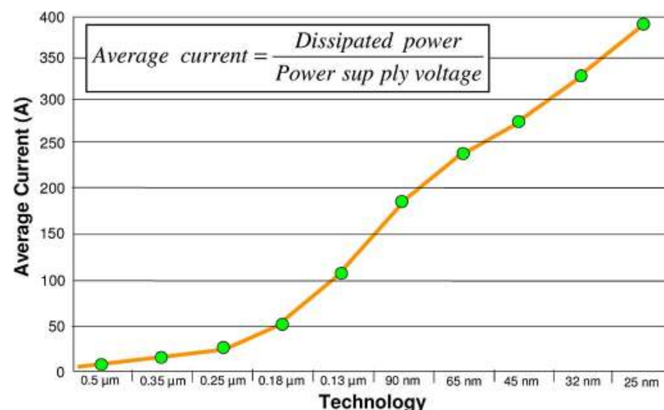

Fig. 33. IC current peak increase with the technology scale-down [109].

Without EMC optimization, the technology trend toward more complex and faster designs is expected to lead to increased emission levels (Fig. 38, upper curve). Although EMC optimization techniques have partially filled the gap between IC customer requests and IC performance (Fig. 38, middle curve) [3], new innovative techniques need to be investigated to compensate for the induced parasitic effects of technology scale-down. In 2020, the required efficiency of these techniques should allow a reduction in unintended emissions of 40 dB. Despite these continuous efforts, there is a gap between IC customer requests and intrinsic IC performance. Not only do generic low-emission design guidelines need to be generalized and integrated in SOC design flows, but advanced design techniques should also be applied to respond to IC customer pressure for less conducted and radiated noise.

The technology trend toward lower noise margins, more I/O structures, and higher bus speeds should lead to even higher susceptibility to RFI (Fig. 39, lower curve). Generic high-immunity design guidelines should be introduced in SOC design flows, as a response to IC customer pressure for higher immunity (Fig. 39, middle curve).

Again, innovative design guidelines are mandatory to follow the steady customer demand for improved IC immunity (Fig. 39, upper curve).

B. EMC Measurement Methods

Mature standardization methods exist for characterizing both emissions [97] and susceptibility [98], enabling reliable comparisons of EMC performance between ICs.

The roadmap for measurement methods relating to EM emissions is shown in Table X. Below 3 GHz, stable standards exist for both conducted and radiated emission measurements. For the 3–10 GHz frequency band, solutions for conducted mode measurements do exist but they have not been standardized. The gigahertz TEM (GTEM) cell is one possible method for characterizing IC radiated emissions up to 18 GHz. From 10 to 40 GHz, the GTEM cell concept may still be applicable as well as the anechoic chamber that concerns the radiated mode. Conducted mode emission measurements within 10–40 GHz are still an issue.

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TABLE IX
EVOLUTION OF KEY PARAMETERS VERSUS TECHNOLOGY NODE

Technology	External supply (V)	Average Current (A)	Gate density (/mm^2)	Gate current peak (mA/gate)	Capacity (fF/gate)
1.2 µm (1985)	5 V	<1	8 K	1.1	60
0.8 µm (1990)	5 V	<1	15 K	0.9	40
0.5 µm (1993)	5 V	3	28 K	0.75	30
0.35 µm (1995)	5-3.3 V	12	50 K	0.6	25
0.25 µm (1997)	5-2.5 V	30	90 K	0.4	20
0.18 µm (1999)	3.3-2.0 V	50	160 K	0.3	15
0.12 µm (2001)	2.5-1.2 V	150	240 K	0.2	10
90 nm (2004)	2.5-1.0 V	186	480 K	0.1	7
65 nm (2006)	2.5-0.7 V	236	900 K	0.07	5
45 nm (2008)	1.8-0.8 V	283	2000 K	0.05	3

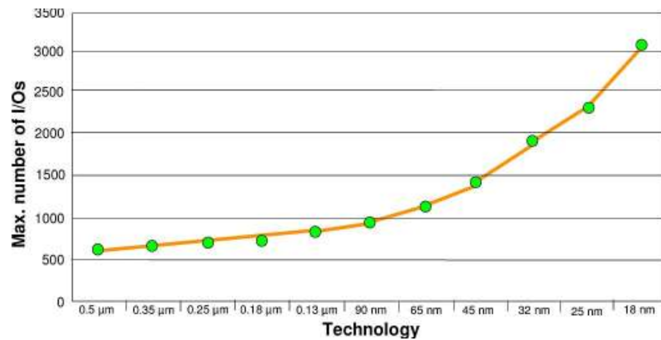

Fig. 34. Maximum number of I/Os [109].

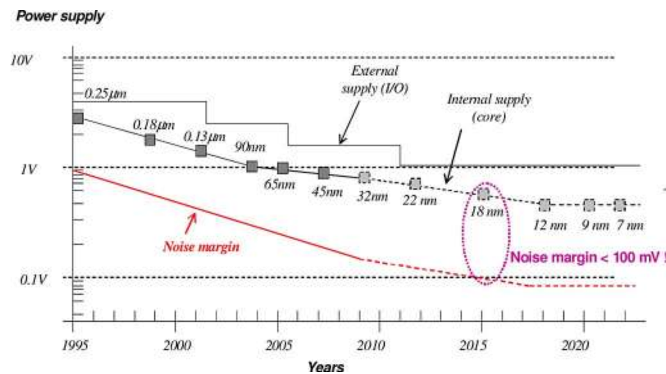

Fig. 35. Continuous decrease of power supply voltages.

The roadmap for susceptibility measurement methods is shown in Tables XI and XII. One set of methods is close to industrial use, mainly below 3 GHz. Promising research results have been published to address the frequency band 3–10 GHz. Above 10 GHz, although mode-stirred chambers or anechoic chambers may be used, conducted immunity methods do not yet exist.

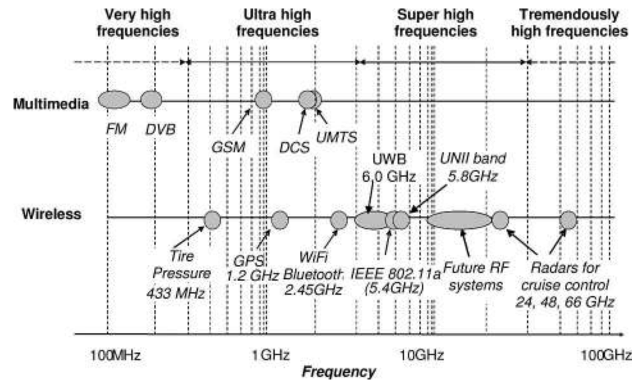

Fig. 36. Multimedia and wireless systems in the frequency spectrum.

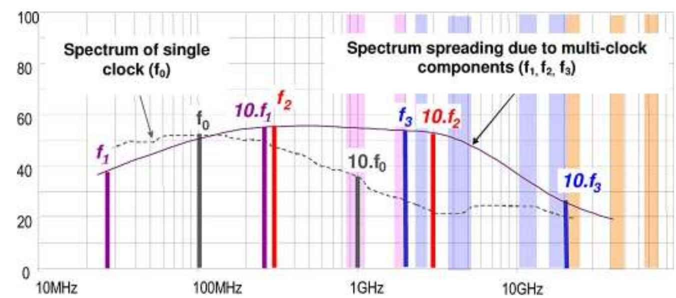

Fig. 37. Emission spectrum spreading for new generation components.

Table XII illustrates the availability of impulse immunity methods that could be applicable for industrial use in the near future.

C. *Roadmap for EMC Models*

The exponential increase in IC complexity associated with the increase in operational frequency is one of the difficulties with EMC modeling as it leads to higher model complexity: a higher number of electrical elements, a wider set of EM phenomenon

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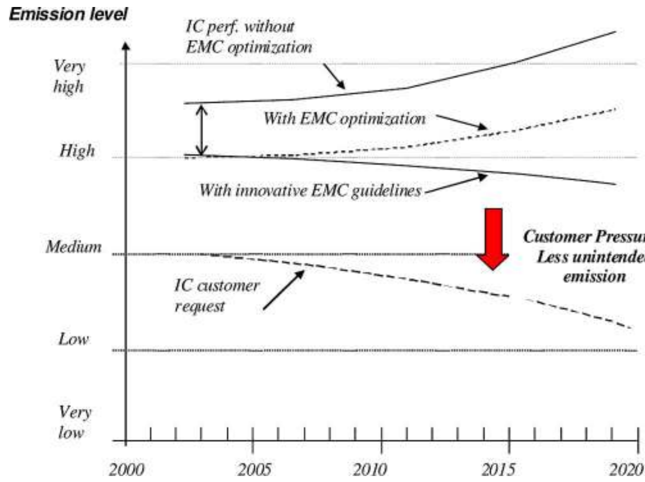

Fig. 38. Evolution of the peak emission level over the last few years and projection until 2020.

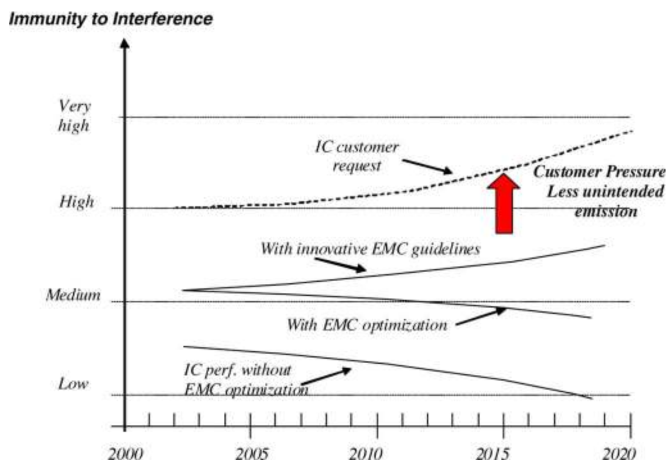

Fig. 39. Diverging trends between IC immunity requirements and increased susceptibility with technology improvements.

TABLE X
EVOLUTION OF STANDARD MEASUREMENT METHODS FOR EMISSIONS

Frequency band	Type	2005	2010	2015	2020
Below 3 GHz (IEC 61967)	Conducted	Ind. use 150Ω, Magnetic Probe			
	Radiated	Ind. use TEM, Near Field			
3 – 10 GHz	Conducted	Sol. exists	Ind. use		
	Radiated	Ind. use GTEM			
10 – 40 GHz	Conducted	NOT known	Sol. exists	Ind. use	
	Radiated	Sol. exists	Ind. use		

TABLE XI
EVOLUTION OF RF IMMUNITY STANDARD MEASUREMENT METHODS

Frequency band	Type	2005	2010	2015	2020
Below 3 GHz (IEC 62132)	Conducted	Sol. exists (e.g. BCI, DPI)	Ind. use		
	Radiated	Ind. use TEM (e.g. TEM)			
3 – 10 GHz	Conducted	Sol. exists (e.g. Extended DPI)	Ind. use		
	Radiated	Sol. exists (e.g. GTEM, NF-scan, LIHA, IC stripline)	Ind. use		
10 – 40 GHz	Conducted	NOT known	Sol. exists	Ind. use	
	Radiated	Sol. exists: (e.g. MSC Anechoic chamber)	Ind. use		

TABLE XII
EVOLUTION OF IMPULSE IMMUNITY STANDARD MEASUREMENT METHODS

Pulse	Type	2005	2010	2015	2020
Fast pulse (IEC 62215)	Conducted	Sol. exists (e.g. Synch. Trans Immunity Test)	Ind. use		
	Radiated	NOT known	Sol. exists	Ind. use	
Medium pulse		Sol. exists (e.g. Electrical Fast Transient)	Ind. use		
Slow pulse		Sol. exists	Ind. use		

TABLE XIII
EVOLUTION OF STANDARD EMISSION MODELS

Bandwidth	Type	2005	2010	2015	2020
Below 3 GHz	Conducted IEC-62433-2	Ind. use (ICEM-CE)			
	Radiated IEC-62433-3	Sol. exists (ICEM-radiated, dipole)	Ind. use		
3 – 10 GHz	Conducted	NOT known	Sol. exists	Ind. use	
	Radiated	NOT known	Sol. exists	Ind. use	
10 – 40 GHz	Conducted	NOT known	NOT known	Sol. exists	Ind. use
	Radiated	NOT known	NOT known	Sol. exists	Ind. use

TABLE XIV
EVOLUTION OF RF STANDARD IMMUNITY MODELS

Bandwidth	Type	2005	2010	2015	2020
Below 3 GHz (IEC 62433)	Conducted 62433-4	NOT known	Sol. exists	Ind. use	
	Radiated 62433-5	NOT known	Sol. exists	Ind. use	
3-10 GHz	Conducted	NOT known	NOT known	Sol. exists	Ind. use
	Radiated	NOT known	NOT known	Sol. exists	Ind. use
10 – 40 GHz	Conducted	NOT known	NOT known	Sol. exists	Ind. use
	Radiated	NOT known	NOT known	Sol. exists	Ind. use

TABLE XV
EVOLUTION OF TRANSIENT STANDARD IMMUNITY MODELS

Pulse	Type	2005	2010	2015	2020
Fast Pulse (IEC 62433)	Conducted	NOT known	Sol. exists	Ind. use	
	Radiated	NOT known	Sol. exists	Ind. use	

involved [112], which require multiple simulation approaches, electrical as well as 3-D full-*wave* EM simulations.

Simulating the IC's EM behavior before manufacture is a key factor for avoiding expensive and time-consuming redesigns. EMC models must be created to predict accurately the EM emissions of an IC and its susceptibility to external interference by keeping in mind the need to reduce simulation time. Modeling approaches up to 1 GHz have been the subject of intensive discussion, from which a draft for standardization has emerged, named ICEM [108]. However, a significant research effort is needed to provide appropriate methodologies for EMC prediction up to 10 GHz.

The roadmap for emission models at the IC level is shown in Table XIII. Ongoing developments in EMC prediction should open up new ambitions and opportunities.

The development of reliable immunity models and tools is also mandatory to supplement and reduce time-consuming testing procedures. Immunity standard proposals such as ICIM are still at the research stage. The roadmap for immunity models at IC level is shown in Tables XIV and XV.

The intention of these tables has been to keep the EMC community abreast of recent developments at the IC measurement and modeling levels, and to help guide sound decisions for future

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research that targets improved EMC characterization methods and performance prediction methodologies.

VII. Conclusion

For more than 40 years, researchers have been pursuing the development of measurement methods, prediction tools, and design techniques for improving the EMC performance of ICs. The focus of this paper was to summarize past, present, and future work with an emphasis upon measurement methods and modeling approaches. Looking to the future, there are many difficult challenges ahead, most without clear solutions. A set of issues was highlighted, regarding low-emission design techniques, high-immunity guidelines, extremely high-frequency measurement techniques, as well as efficient methodologies for reliable prediction of EMC performance prior to manufacture.

The field of EMC at the component level has grown much beyond the expectations of one or two decades ago. EMC expertise has successfully weathered and, in fact, thrived on the IC technology scale-down.

We expect component-level EMC to continue to be an active field of study in the future, as ICs become larger, denser, and operate at higher clock speeds and lower supply voltages. We hope this paper provides readers with a sense of the past and future trends in EM compliance of ICs, following the extraordinary advances of the microelectronics industry.

Acknowledgment

The authors acknowledge the many EMC engineers and IC designers, whether referenced or not, who have contributed to the improvement and understanding of this field over the years.

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