Title
THE ELECTRONICS FOR THE DONNER 600-CRYSTAL POSITRON TOMOGRAPH

Author
Cahcon, J.L.

Publication Date
1985-10-01

Lawrence Berkeley Laboratory
UNIVERSITY OF CALIFORNIA

Presented at the 1985 IEEE Nuclear Science Symposium, San Francisco, CA, October 23-28, 1985; and to be published in IEEE Transactions on Nulcear Science, Vol. NS-33, 1986

THE ELECTRONICS FOR THE DONNER 600-CRYSTAL POSITRON TOMOGRAPH

J.L. Cahoon, R.H. Huesman, S.E. Derenzo, A.B. Geyer, D.C. Uber, B.T. Turko, and T.F. Budinger

October 1985

Donner

Biology & Medicine Division

Prepared for the U.S. Department of Energy under Contract DE-AC03-76SF00098

DISCLAIMER

THE ELECTRONICS FOR THE DONNER 600-CRYSTAL POSITRON TOMOGRAPH

J.L. Cahoon, R.H. Huesman, S.E. Derenzo,
A.B. Geyer, D.C. Uber, B.T. Turko, and T.F. Budinger

Donner Laboratory and Lawrence Berkeley Laboratory
University of California
Berkeley, CA 94720

Abstract

The data acquisition system, designed for the Donner 600-Crystal Positron Tomograph, is described. Coincidence timing resolution of less than five nanoseconds full width at half maximum and data rates in excess of one million events per second are achieved by using high-speed emitter coupled logic circuits, first-in first-out memory to derandomize data flow, and parallel architecture to increase throughput. These data rates allow the acquisition of adequate transmission data in a reasonable amount of time. Good timing resolution minimizes accidental coincidences and permits data rates greater than 100,000 image-forming events per second for high-speed dynamic emission tomography. Additional scatter and accidental rejection are accomplished for transmission data by using an orbiting source and a look-up table for valid events. Calibration of this complex electronic system is performed automatically under computer control.

Introduction

This paper describes the electronics for the Donner 600-Crystal Positron Tomograph. Primary design objectives for the tomograph were:

- to achieve spatial resolution of less than three millimeters full width at half maximum (FWHM),
- to obtain emission data rates greater than 100,000 image-forming events per second for dynamic studies,
- to obtain transmission data rates greater than one million events per second for short data acquisition times, and
- to perform the calibration of this complex electronic system automatically under computer control.

High resolution is achieved by using 600 bismuth germanate (BGO) crystals, each with its own photomultiplier tube (PMT), arranged as a close packed, single layer ring.[1] The detector ring diameter is 60 centimeters, and the patient port diameter is 30 centimeters. The BGO crystals are 3 millimeters in the azimuthal direction by 10 millimeters in the axial direction by 25 millimeters in the radial direction. Clamshell motion of the gantry[2] has been implemented to double the spatial sampling.

High data rates are achieved by using high-speed emitter coupled logic (ECL) circuits in most of the electronics. First-in first-out (FIFO) memory is used extensively to derandomize data flow and therefore reduce dead time while acquiring and processing data. Parallel architecture is also used to increase data throughput. Minimization of accidental coincidences is achieved by using a coincidence timing window of 5 nanoseconds or less. This maximizes the useful event rate for emission data. In addition, transmission data are acquired with an orbiting source,[3] which allows the rejection of nearly all scattered and accidental events in this mode. All energy threshold and timing adjustments are performed by the host computer.

Description

Figure 1 shows a block diagram of the electronics for the Donner 600-Crystal Positron Tomograph. The design is modular, and the constituent modules are described in the following sections.

Front-End Electronics

There are 600 front-end electronic circuits on 75 printed circuit cards (Fig. 2). Each circuit serves one phototube by amplifying its signal, integrating the charge, and starting a timing cycle from the first photoelectron liberated from the photocathode.[4]

A timing cycle is started when the timing amplifier receives a signal equivalent to one or more photoelectrons. If the signal consists of an isolated photoelectron, the signal will have returned to the baseline after 50 nanoseconds and the timing cycle is reset. If the signal is still present after 50 nanoseconds, the output of the charge amplifier is accumulated on the charge

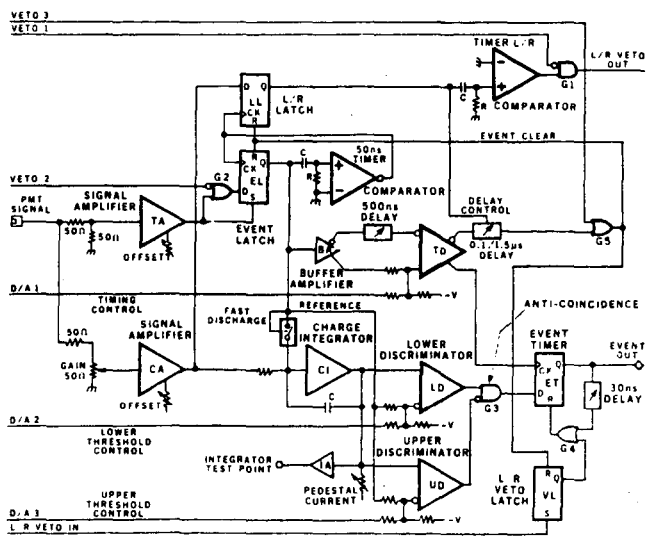

Figure 2: Front-end block diagram

TO BE PRINTED IN IEEE
Transactions on Nuclear Science
Vol. NS-33, 1986

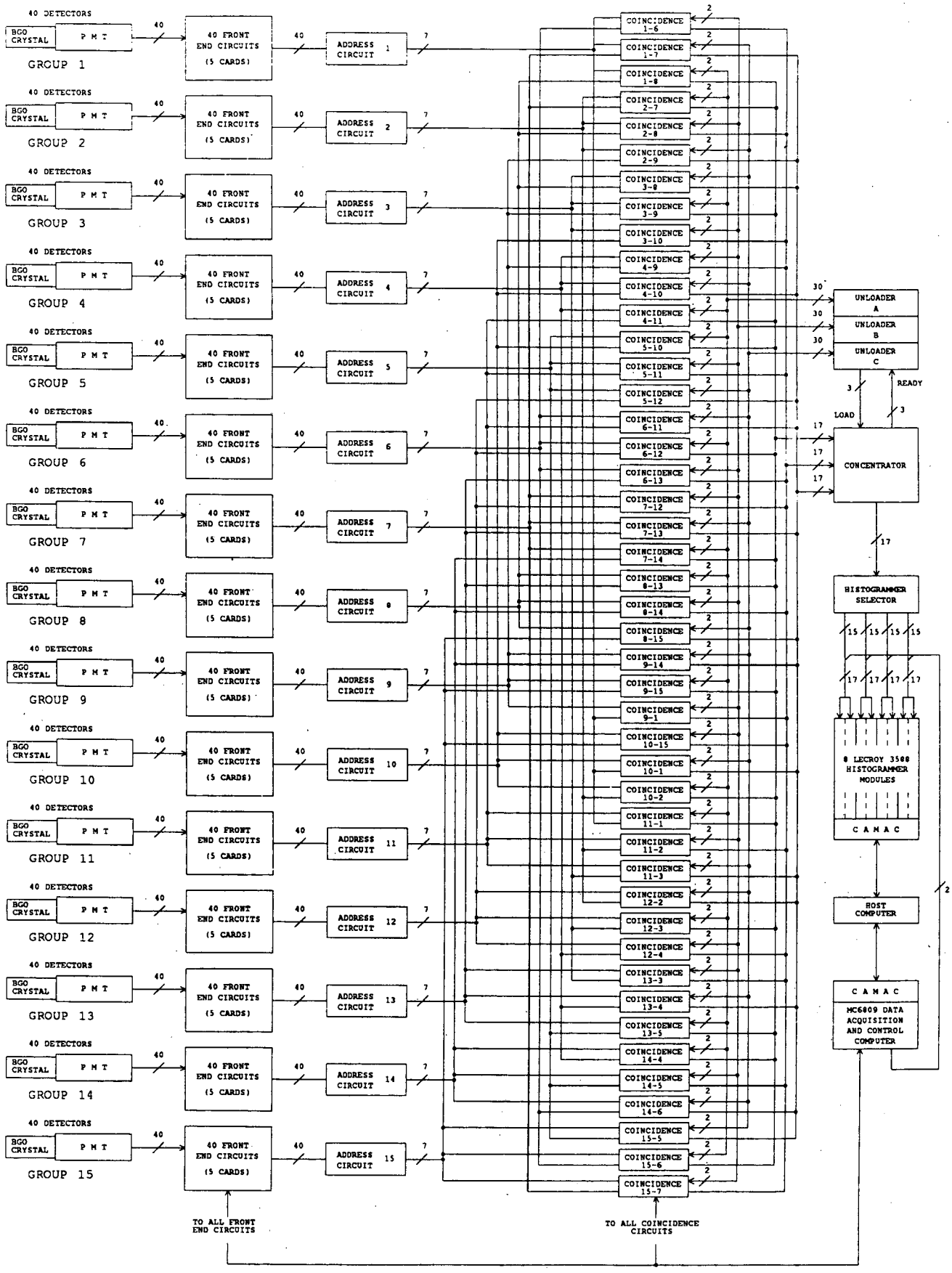

Figure 1: System block diagram

integrator for a period of about 500 nanoseconds. If the output of the integrator corresponds to an energy loss less than 100 keV, the timing cycle is reset. If the output corresponds to more than 100 keV, a veto pulse is sent to the front-end circuits of the nearest neighbor crystals. If this threshold is lowered, X-rays produced in the BGO crystal after a photoelectric interaction are often detected in a neighboring crystal. These give rise to veto pulses and cause the original good event to be discarded. If the output of the charge integrator is in the pulse height window (between the lower and upper thresholds) and no veto pulses have been received from the nearest neighbor crystals, a 23 nanosecond wide timing pulse is generated and sent to an address circuit (see below). In addition, the circuit is disabled for an additional 1.5 microseconds to prevent retriggering by photons in the tail of the scintillator light pulse. The timing pulse is derived from the first photoelectron, and delayed during the pulse height and nearest neighbor veto tests.

The length of this pulse delay and the two pulse height thresholds are established by three 8-bit digital to analog converters (DACs). The DACs have internal digital registers that are addressed and loaded by the host computer.

Address Circuits

There are 15 address circuits on 15 printed circuit cards (Fig. 3). Each circuit accepts the timing pulses from a group of 40 front-end circuits and encodes the 6-bit crystal address. The crystal address and the group timing pulse from each address circuit are sent to six independent coincidence circuits. Each of these coincidence circuits also receives the address and group timing pulse that originate from one of six other address circuits that serve the six opposing groups.

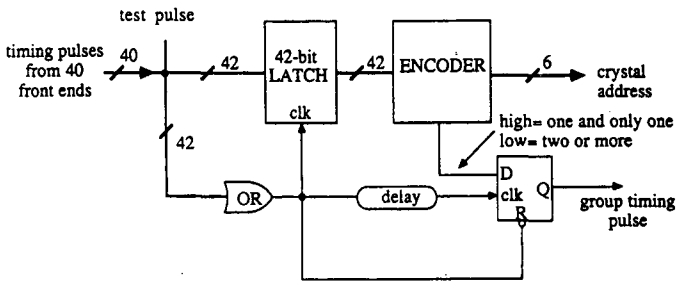

Figure 3: Address circuit block diagram

The address circuits have two types of dead time. If two timing pulses arrive within about 8 nanosecond both are lost, and if they arrive within about 25 nanoseconds the second is lost.

An additional crystal input is provided on each address circuit. A dynamic measure of the system deadtime can be made by simultaneously applying pulses to these inputs, and comparing the number of events histogrammed to the number of pulses injected. However, this does not measure the deadtime contributed by the front-end circuits.

Coincidence Circuits

There are 90 coincidence circuits on 45 printed circuit cards (Fig. 4). Each coincidence card accepts the group timing pulses and encoded crystal addresses from two address circuits. The two coincidence circuits on each card determine whenever the two group timing pulses occur within the coincidence window width. One coincidence circuit determines the on-time coincidences and the other has one group timing pulse delayed by a time much larger than the coincidence window, so that it responds only to accidental (random and unrelated) coincidences. Since the coincidence timing windows of both circuits are the same, the number of off-time events acquired is an estimate of the number of accidental events contained in the acquired on-time data.

When an on-time coincidence occurs, the two 6-bit crystal addresses are stored in a 12-bit by 3-word deep, ECL, FIFO memory, which can accept events at 17 nanosecond intervals. The off-time (delayed) coincidences are similarly stored in a second FIFO. The outputs of the two high-speed FIFOs are then sent to a 13-bit by 16-word FIFO, which can accept events at 120 nanosecond intervals, and the 12-bit crystal address plus an on-time/off-time coincidence status bit is stored.

Coincidences are detected using an ECL D-type flip-flop. The clock of the flip-flop is connected to the slightly delayed group timing pulse of one of the address circuits. (This is a timing adjustment delay different from the off-time delay.) The D-input is connected to a constant width pulse derived from the group timing pulse of the other address circuit. The delay of the clock pulse and the width of the D-input pulse are established by two 8-bit DACs. These DACs have internal registers that are addressed and loaded by the host computer.

A read-only-memory (ROM) is used to convert the pair of crystal addresses, sent from the 13-bit FIFO, into a unique 16-bit histogram address. The resulting histogram addresses are ordered by lateral-position and angle of the line between the two crystals, so that the data are stored in parallel-ray (sinogram) format in the histogram memory. The ROM is partitioned into two sections; one section generates a set of histogram addresses for the clamshell closed condition, while the other section provides histogram addresses when the clamshell is open.

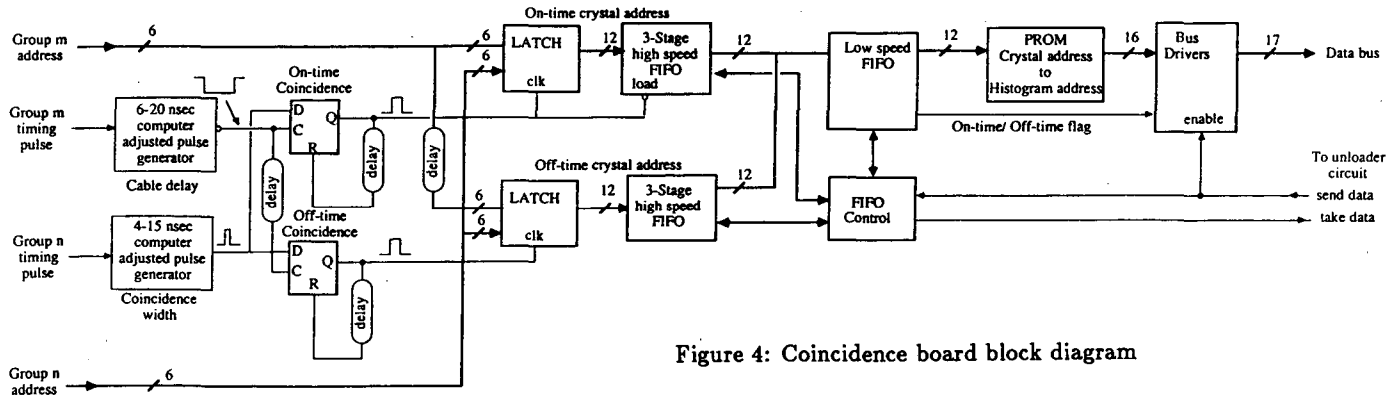

Figure 4: Coincidence board block diagram

Unloader Circuits

There are three unloader circuits on three circuit boards (Fig. 5). The unloader circuits control and prioritize data flow from the coincidence circuits to the concentrator circuit (see below). Each unloader circuit accepts control signals from 15 coincidence circuits.

In order to maintain high data acquisition rates, three identical unloader circuits operate independently and in parallel. The three groups of coincidence circuits have been chosen so that, for physically realizable distributions of positron emitter, data rates in the unloader circuits are similar.

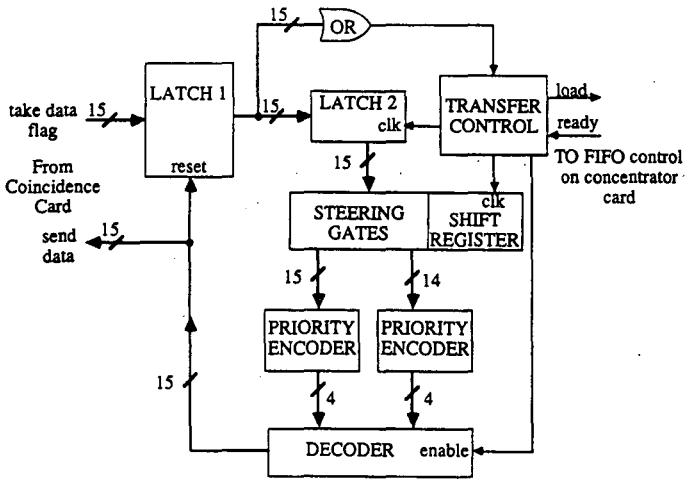

Figure 5: Unloader circuit block diagram

When a coincidence circuit has data (a histogram address) ready to be transferred, it signals its unloader circuit. More than one coincidence circuit may have data ready, and the unloader selects one card, on a rotating priority basis. The selected coincidence circuit puts its data on a data bus, which is connected to the 15 coincidence circuits and the concentrator circuit. On command from the unloader circuit, the concentrator accepts data from the data bus.

After data have been transferred, the priority of the coincidence circuits is rotated. The highest priority becomes the lowest, while the rest move up one step to the next higher level. This scheme prevents one coincidence circuit from dominating the data bus. If, at very high rates, events occur faster than they can be processed, data loss from each coincidence circuit will be distributed in proportion to the event rate of that circuit.

Concentrator Circuit

The concentrator circuit accepts data from the coincidence circuits and passes data to the histogram selector circuit. It contains three separate, 17-bit by 16-word deep, FIFO memories, each connected by a data bus to 15 coincidence cards. The FIFO filling operation is controlled by the unloader circuits, as described above. Data extraction from these FIFO memories is a separate, independent operation from data filling. Data to be passed to the histogram selector are taken from the FIFOs, on a rotating priority basis, similar to the operation of the unloader circuit as described above.

For emission data, the data from the FIFO memory are sent directly to the histogram selector. For transmission data, the data from the FIFO memory, along with additional data that indicates the position of the orbiting source, are combined to address mask-bits in a 256K by 1-bit ROM. If the line between two active crystals also intersects the orbiting source, the event is accepted. All other events are prompt scatters or accidentals and are rejected. The mask-bits contained in the ROM are generated by acquiring data with the orbiting source in one position. The resulting histogram data are thresholded to indicate histogram addresses which result from true unscattered positron-electron annihilations.

Histogram Selector Circuit

The histogram selector circuit receives data (histogram addresses) from the concentrator circuit as described above. The histogram selector is physically located near the host computer and histogram memory (see below) which are about 50 feet from the tomograph and the electronics described thus far.

The histogram selector circuit contains four 15-bit by 16-word deep FIFO memories. The 15^{th} and 16^{th} data bits sent from the concentrator are used to steer the remaining 15 data bits to one of these four FIFOs. Each FIFO subsequently sends data to a histogram memory module.

Histogram Memory

Data are acquired on eight, LeCroy 3588 Histogramming Memory modules that have been modified to allow histogram memory to be incremented for on-time events and decremented for off-time events, thus subtracting the accidental coincidences during data acquisition. Each histogram module has 32K 12-bit words. The histogram memories operate in a double buffered mode, so that four of the eight modules acquire data concurrently. Since each clamshell position requires 60K words of memory, data can be acquired from alternate clamshell positions before data transfer. The limiting speed on each module is about 1 MHz, so that by using four modules in parallel, the histogramming limit is nearly 4 MHz.

The low-order 14 data bits correspond to the low-order 14 address bits of each module; the 15^{th} and 16^{th} data bits have been used by the histogram selector to select one of the set of four histogram modules. The high-order data bit (on-time/off-time) determines whether to increment or decrement the memory. The high-order address bit of each module corresponds to clamshell position.

The histogrammers communicate with the host computer through a CAMAC interface. Data are transferred directly from the histogrammer modules to disk without passing through host computer memory. About 120K words of data from four modules (both clamshell positions) are transferred in about 2 seconds.

Data Acquisition Control System

The data acquisition control module is a microcomputer based system, attached to the CAMAC dataway, that accepts input parameters from the host computer concerning how data are to be acquired. When started, it automatically performs all of the timing and data routing for the study. Input parameters include whether the data are from a transmission or emission source, whether the study is to be gated and when the clamshell position is to be changed. For sequential studies the number of frames and the length of time for each frame in the sequence are also required. Gating information consists of a start time (after the R-wave of an EKG signal) and the time duration of the gate.

Signals from this module also control data routing to one of the two sets of four histogram modules. (Data routing between two sections of each of the four active histogram modules corresponding to clamshell position is also performed by this control system.) Data acquisition is alternately switched between the two sets of histogram modules, and the host computer is signaled by the control module, over the CAMAC dataway, to transfer data from the inactive set to disk. In this way data acquisition and data transfer occur concurrently, and data acquisition is uninterrupted.

The data acquisition control module contains a Motorola MC6809 microprocessor. Program development is done using a cross-assembler on the host computer, and the resulting object code is downloaded to the module through a serial link for debugging. The final code is transferred to a ROM which is inserted into and becomes part of the control module.

Summary

The data acquisition system for the Donner 600-Crystal Positron Tomograph uses state of the art electronics and parallel architecture to maximize the amount of medically useful data acquired from research and clinical studies. Transmission data are acquired quickly (over one million events per second) by using fast electronics and a orbiting source to reduce accidental and scattered coincidences. Dynamic emission studies with high useful event rates (over 100,000 image-forming events per second) are possible because of low dead time and a narrow coincidence window. In order to accomplish calibration of such a complex electronic system, computer adjustment of pulse height thresholds, coincidence timing, and coincidence window width is employed.

References

1. Derenzo SE, Huesman RH, Budinger TF, Cahoon JL, and Vuletich T: High resolution positron emission tomography using 3 mm wide bismuth germanate crystals. *J Nucl Med* **25**: P46, 1984.

2. Huesman RH, Derenzo SE and Budinger TF: A two-position sampling scheme for positron emission tomography. In *Nuclear Medicine and Biology,* Raynaud C, ed., Pergammon Press, New York, Vol I, pp 542-545, 1983.

3. Carroll LR, Kretz P, and Orcut G: The orbiting rod source: improving performance in PET transmission correction scans. In *Emission computed tomography—current trends.* Esser PD, ed. New York: Society of Nuclear Medicine, 1983.

4. Lynch FJ: Basic Limitation of scintillation counters in time measurements. *IEEE Trans Nucl Sci* **NS-22**: 58-64, 1975.

Acknowledgements

This work was supported in part by the Director, Office of Energy Research, Office of Health and Environmental Research of the U.S. Department of Energy, under Contract No. DE-AC03-76SF00098, and in part by the National Institutes of Health, National Heart, Lung, and Blood Institute under grant No. P01 HL25840.

LAWRENCE BERKELEY LABORATORY
TECHNICAL INFORMATION DEPARTMENT
UNIVERSITY OF CALIFORNIA
BERKELEY, CALIFORNIA 94720