The emergence of spin electronics in data storage

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Electrons have a charge and a spin, but until recently both were considered separately. In classical electronics, charges are moved by electric fields to transmit information and are stored in a capacitor to save it. In magnetic recording, magnetic fields were used to read or write the information stored on the magnetization, which "measures" the local orientation of spins in ferromagnets. The picture started to change in 1988, when the discovery of Giant Magneto-Resistance (GMR) opened the way to efficient control of charge transport through a magnetization. The recent expansion of hard disk recording owes much to this development. And new scientific breakthroughs open a new paradigm where magnetization dynamics and charge currents act on each other in nanostructured artificial materials. Ultimately, "spin currents" could even replace charge currents for the transfer and treatment of information, allowing faster, low energy operations: "Spin electronics" is on its way.

The interdependence between magnetization and charge transport is not a new story. For instance, the anisotropic magnetoresistance (AMR), which links the value of the resistance to the respective orientation of magnetization and current, was first observed in 1856 by W. Thomson but its amplitude is weak (up to a few %). Even though, the introduction by IBM in 1991 of a magnetoresistive read head based on AMR was a major technological step forward [1]. In hard disk drives (HDD), the head flies at constant height above the magnetic domains that define the "bits" in the recording medium, and senses the spatial variations of the stray magnetic field of these domains. The old "ring head", invented in 1933 by E. Schuller (AEG) for tape recording, measured a magnetic flux, and so was approaching its sensitivity limit with the reduction of the head dimensions. In the new head (Figure 1), the AMR sensor, associated to a "ring" element still used for writing, directly senses the magnetic field through its influence on the magnetization orientation in the head. The AMR head had a relative "magnetoresistance" (hereafter referred to as $\Delta R/R=(R_{max}-R_{min})/R_{min}$) of the order of only 1%,

but this was enough to immediately increase the growth rate of HDD storage areal density from 25% per year, its value since nearly the introduction of HDD in 1957, up to 60% per year.

Fundamentals of spin electronics.

The physics background behind today's fast expansion of spin electronics has also been known for a long time. A cornerstone is the "two currents" conduction concept proposed by N. Mott [2] and used by Fert and Campbell [3-4] to explain specific behaviours in the conductivity of usual ferromagnetic metals Fe, Ni, Co, and their alloys. In such "itinerant ferromagnets" both the 4s and 3d electron bands participate to the Fermi level E_F. Because of the strong exchange interaction favouring parallel orientation of electron spins, the "spin up" and "spin down" 3d bands are shifted in energy. This band splitting creates the imbalance between numbers n_{up} and n_{down} of 3d electrons at the origin of the ferromagnetic moment ($\mu \sim -(n_{up}-n_{down})\mu_B$/atom, where μ_B is the Bohr magneton), while the conduction is dominated by the unsplit 4s band, the 4s electrons having a much higher mobility. However, the spin conserving s-to-d transitions are the main source of s electron scattering. This has two major consequences on transport: the spin imbalanced density of states for 3d electrons at E_F results in strongly spin dependent scattering probabilities (Fermi "Golden rule"), and between two spin flip scattering events an electron can undergo many scattering events while keeping the same spin direction. Thus at the limit where spin-flip scattering events are negligible, conduction happens in parallel through two spin channels that have very different conductivities. Important length scales can be discussed in the diffusive transport model. The spin dependent scattering probability results in very different mean free paths λ_{up} and λ_{down}, or equivalently relaxation times τ_{up} and τ_{down}. In usual thin metallic layers they scale from a few nm to a few tens of nm, with highly variable $\lambda_{down}/\lambda_{up}$ ratios: some impurities have strongly spin-dependent cross-sections, so that, in Ni for example, the ratio $\lambda_{down}/\lambda_{up}$ can reach 20 for Co impurities or decrease to 0.3 with Cr doping [4]. Another important length scale is the spin conserving drift length projected along one direction, called the spin diffusion length L_{sf}. It is generally much larger than the mean free path [5].

Giant magnetoresistance and the spin valve head

The founding step of spin electronics, which triggered the discovery of the giant magnetoresistance [6, 7], was actually to build magnetic multilayers with individual

thicknesses comparable to the mean free paths, thus able to evidence the spin dependent electron transport. The principle is schematized in Figure 2A for the simplest case of a tri-layer film of two identical ferromagnetic layers F1 and F2 sandwiching a non magnetic metal spacer layer M, when the current circulates “in plane” (cf Figure 2B). We assume a ferromagnetic film thickness t_F comprised between $\lambda_{up}^{(F)}$ and $\lambda_{down}^{(F)}$, with $\lambda_{up}^{(F)} >> \lambda_{down}^{(F)}$, and a spacer layer thickness $t_M << \lambda^{(M)}$. When the two magnetic layers are magnetized parallel (P), the spin up electrons can travel through the sandwich nearly unscattered, providing a conductivity shortcut and a low resistance. On the contrary, in the antiparallel (AP) case both spin up and spin down electrons undergo collisions in one or the other F layer, giving rise to a high resistance. The relative magnetoresistance $\Delta R/R=(R_{AP}-R_P)/R_P$ can reach 100% or more in multilayers with a high number of F/M periods. It was already 80% in the Fe/Cr multilayer of the original discovery [6], hence the name of “giant magnetoresistance” (GMR). Elaborate theories must of course take into account other effects such as interfacial scattering, quantum confinement of the electrons in the layers, etc. [8, 9].The GMR is an outstanding example of how nanostructuring materials at the nanoscale can bring to light fundamental effects, providing new functionalities to applications. And indeed the amplitude of the GMR immediately triggered intense research, soon achieving the definition of the “spin valve” sensor [10, 11, 12]. In its simplest form, the “spin valve” (SV) is only a trilayer film of the kind displayed in Figure 2A, in which one layer (e.g. F2) has its magnetization pinned along one orientation. The rotation of the “free” F1 layer magnetization then “opens” (in P configuration) or “closes” (in AP configuration) the flow of electrons, acting somehow as a valve.

The standard SV shows magnetoresistance values of about 5 to 6%. More complex SV stacks, with layer thicknesses controlled at the atomic scale and ultra low surface roughness, are optimized to favour specular reflection of electrons towards the active part so that the magnetoresistance reaches about 20%. Following the introduction in 1997 by IBM of the SV sensor (Figure 2B) to replace the AMR sensor in magnetoresistive HDD read heads, the storage areal density growth rate immediately increased up to 100% per year. As a whole, the sequential introduction of the magnetoresistance and spin valve head, by providing a sensitive and scalable read technique, contributed to increase the raw HDD areal recording density by 3 orders of magnitude (from ~0.1 to ~100Gbit/in^2) between 1991 and 2003. This outstanding jump forward opened the way to both smaller HDD form factors (down to 0.85” disk diameter!) for mobile appliances such as ultra laptops or portable multimedia players, and to

record high drive capacities (up to 1 TByte!) for video recording or backup. HDD are now replacing tape in at least the first tiers of data archival strategies, for which they provide faster "random" access and higher data rates. However, the areal density growth rate started to slow down after 2003, when other problems joined the now limiting SV head.

Attempts were also made to develop solid state magnetic storage. Provided that the "free" layer magnetization of the SV is constrained to take only the two opposite orientations of an easy magnetization axis, arrays of patterned spin valve elements can be used to store binary information with resistive read-out. Spin-valve solid state memories were indeed developed [13]. However, the planar geometry of the spin valve sensor intrinsically limit the integration into high density nanoelectronics, while the low metallic resistance and a $\Delta R/R$ value around 10% are not well adapted to CMOS electronics. For read heads also, the "current in plane" SV geometry is a limitation to the downscaling. First, it's easy to see that the integration of the planar element of Figure 2B between the magnetic shields of the read head of Figure 1 strongly limits the minimum dimension of the "read" gap between the P1 and P2 poles, a crucial requirement for reducing the bit length: indeed, two thick insulating layers are needed on either part of the sensor. The "current perpendicular to plane" (CPP) geometry of Figure 2C is much more favourable for this purpose, as the SV sensor can be directly connected to the magnetic shields. This configuration is also more favourable for reducing the track width. And the GMR in CPP geometry presents other more fundamental interests.

But simple geometrical arguments based on the average electron propagation direction also lead to expect higher magnetoresistance values for a spin valve in the CPP configuration. The fundamental study of CPP GMR was indeed extremely productive in terms of the new concepts of spin injection and spin accumulation [14]. The basic principle is displayed in Figure 3. In Drude's model for diffusive transport in 3d ferromagnetic metals, the total current density is the sum of j_{up} and j_{down} current densities proportional to the respective relaxation times τ_{up} and τ_{down}. Again we assume that $\tau_{up} >> \tau_{down}$. So when a current flows from a ferromagnetic layer F to a non magnetic layer M, away from the interface j_{up} and j_{down} must be very different on the ferromagnetic side, and equal on the non magnetic side. The necessary adjustment requires that, in the area near the interfaces, more electrons from the spin up channel flip their spins. This occurs through an "accumulation" of spin up electrons, i.e. a splitting of the E_{Fup} and E_{Fdown} Fermi energies, which induces spin-flips and adjusts the incoming and outgoing spin fluxes. The spin accumulation decays exponentially on each side of the interface on the scale of the respective spin diffusion lengths $L_{sf}^{(F)}$ and $L_{sf.}^{(M)}$. In this spin accumulation zone, the spin polarization of the current decreases progressively as one

goes from the magnetic conductor to the nonmagnetic one, so that a spin polarized current is "injected" into the non magnetic metal on a distance that can reach a few hundreds of nm, well beyond the ballistic range. This concept has been extended to more complex interfaces between metals and semiconductors [15] (Figure 3C). Likewise, the concept applies when an interfacial resistance such a Shottky or insulating barrier exists [16]. The spin injection effect was also demonstrated for planar geometries [17], and proposed to realize 3-terminal devices such as the spin transistor [18]. We will come back on this point later.

If the magnetoresistance ratio is larger in the CPP geometry, exceeding 20%, CPP-GMR samples are much more difficult to fabricate [19]. In particular, quantitative measurements require either superconducting contacts [20] or long multilayered wires [21] to ensure current lines perpendicular to the layers. And the resistance and magnetoresistance still remain too small for optimal application to read heads [22]. Strong industrial research is going on (cf for instance [23]) .

Magnetic tunnel junction

Another major breakthrough came from replacing the non magnetic metallic spacer layer M of the spin valve by a thin (~1-2nm) non magnetic insulating layer, thus realizing a "magnetic tunnel junction" (MTJ). In that configuration the electrons travel from one ferromagnetic layer to the other by a tunnel effect which conserves the spin (Figure4A). This again is not a new story, as it was proposed by Jullière in 1975 [24], but the practical realization with a high magnetoresistance (up to 30% at 4.2K) waited until 1995 with drastic progress in deposition and nanopatterning techniques [25, 26]. The first MTJs used an amorphous Al_2O_3 insulating layer between ferromagnetic metal layers: the tunnel magnetoresistance (TMR) of such stacks reached a limit around 70% at room temperature. Much higher effects were later obtained with a single crystal MgO barrier [27, 28]. Within such a barrier, the tunnelling current is carried by evanescent waves of several well defined symmetries which, at least for high quality interfaces, have an interfacial connection in the metals only to Bloch waves of the same symmetry at the Fermi level [29, 30]. In the typical case of MgO(001) between Co electrodes for instance, the decay is much slower and the transmission higher for the evanescent waves of symmetry Δ_1, so that the TMR comes from the specific high spin polarization of the states of symmetry Δ_1 in a zone of the Fermi surface of Co near [001]. The MgO barrier is thus "active" in selecting asymmetry of high spin polarization, driving to latest record values of $\Delta R/R$=1010% at 5K, 500% at room temperature (Figure 4B) [31]. There is

no sharp symmetry selection in amorphous barriers such as Al_2O_3, which explains the much lower TMR ratios achieved.

The magnetic tunnel junction is clearly a CPP “vertical” device, with a magnetic behaviour similar to a spin valve but up to two orders of magnitude higher magnetoresistance values. It is stable up to reasonable breakdown voltages (above 1V), and the equipment suppliers rapidly developed reliable techniques to scale down its dimensions well below 100nm. So its development had an immediate impact on storage applications. Indeed, a TMR read head was commercialized by Seagate in 2005 [32] (Figure 4C), providing a higher sensitivity. This may however prove to be a short lived option: MTJs have an intrinsic high resistance (with resistance.area (RA) products above one $\Omega.cm^2$), and with further downscaling it will become difficult to maintain a high signal to noise ratio with an increasing sensor resistance. Then CPP spin valves or degenerate MTJs could become more favourable [22].

Magnetic Random Access Memory

The “high” MTJ resistance is actually more adapted to nanoelectronics. The 1995 publications started a race to develop the magnetic random access memory, or MRAM [13]. Figure 5A displays the principle of this magnetic solid state memory, in the basic “cross point” architecture. The binary information “0” and “1” is recorded on the two opposite orientations of the magnetization of the free layer along its easy magnetization axis. The MTJs are connected to the crossing points of two perpendicular arrays of parallel conducting lines. For writing, current pulses are sent through one line of each array, and only at the crossing point of these lines the resulting magnetic field is high enough to orient the magnetization of the free layer. For reading, one measures the resistance between the two lines connecting the addressed cell. In principle, this cross point architecture promises very high densities. In practice, the amplitude of magnetoresistance remains too low for fast, reliable reading because of the unwanted current paths besides the direct one through the addressed cell. So realistic cells add one transistor per cell, resulting in more complex 1T/1MTJ cell architectures such as the one represented in Figure 5B. Several demonstrator circuits were rapidly presented by most leading semiconductor companies, culminating with the first MRAM product, a 4 Mbit standalone memory [33] commercialized by Freescale in 2006, and soon voted “Product of the Year” by "Electronics Products Magazine" (Jan. 2007) (Figure 5C).

The MRAM potentially combines key advantages such as non volatility, infinite endurance, and fast random access (down to 5ns read/write demonstrated, cf [34]), that make it a likely

candidate for becoming the “universal memory”, one of the “Holy Grails” of nanoelectronics. Such a memory is able to provide data/code (Flash, ROM) and execution (DRAM, SRAM) storage using a single memory technology on the same die. Moreover, Freescale introduced in June 2007 a new version able to work in the enhanced -40°C to 105°C temperature range, i.e. qualifying for military and space applications where the MRAM will also benefit from the intrinsic radiation hardness of magnetic storage.

Nanomagnetism

Progress in “spin electronics” is not separable from the development of “nanomagnetism”. In particular, the engineering of magnetic properties at atom level in multilayers was developed in parallel with the GMR and enabled it. The role of interface effects, and the use of the layer thickness as a parameter, enabled the development of artificial magnetic materials with finely tuned new properties. This had a direct impact on “spin storage”.

The magnetic storage of binary information requires engineering an energy barrier between two opposite orientations of the magnetization, able to stop thermally excited reversals [35]. This “magnetic anisotropy” has several competing origins. The strongest one is usually the shape anisotropy due to the dipole-dipole magnetic interaction, which induces the well known in plane easy magnetization of thin films. But the main effect used in recording is the magnetocrystalline anisotropy, an atomic effect correlated to the symmetry of the immediate atomic environment. The interface anisotropy, initially proposed by Néel [36], takes advantage of the drastic break of translational symmetry at an interface to generate giant magnetic anisotropies, able to overcome the shape anisotropy and induce a stable perpendicular magnetization axis (PMA) in ultra thin films and multilayers. This PMA was first observed in 1967 on single atomic layer films [37], and achieved in 1985 in Co/Pd multilayer [38] and Au/Co/Au films [39] with more practical thicknesses. New materials could even be predicted from ab initio calculations [40]. It is now used for recording media in the “perpendicular” HDD introduced by Seagate, Hitachi and Toshiba in 2005-2006, which contributed to restore the present 40% growth rate after the slow down experienced in 2003-2004.

Exchange bias is another crucial effect linked to an interface, here between a ferromagnetic and antiferromagnetic layer: the antiferromagnetic layer has no net magnetic moment that could be sensitive to an applied field, but may retain a large magnetic anisotropy which, transferred to the ferromagnetic layer through interfacial exchange interaction, contributes to stabilize the orientation of its magnetization. This is also an old story [41], but with progress

in interface control [42] it gained wide application in the spin valve and magnetic tunnel junctions to pin the magnetization of the reference magnetic layer. And it can also be used in a new kind of MRAM [43], or to fight thermal excitations of magnetic nanoparticles [44] for future storage.

The growing structural quality of interfaces enabled the realization of the spin dependent quantum confinement of the electrons in metallic ultrathin layers. Together with interfacial band hybridization this now enables to control the exchange interaction between ferromagnetic layers separated by a non magnetic layer [45, 46, 47, 48, 49]. This for instance allows building synthetic antiferromagnets (SAF, trilayers where two ferromagnetic layers are kept magnetized antiparallel by exchange through a non magnetic spacer). Depending on their exact structure and properties, such SAF can provide either enhanced non volatility for constant writing field [50], or a more reliable writing in solid state devices [51], or simply a weak sensitivity to applied field and minimal stray field when the net magnetic moment is brought to zero. They are thus used now respectively as recording media for longitudinal HDD products [1] as well as in Freescale's MRAM product. And they are ubiquitous in all pinned layers of spin valve sensors and MRAM cells where they help the exchange bias and minimize the interlayer dipole-dipole interaction.

So at the beginning of this century outstanding progress had been made both in designing the magnetic properties through atomic engineering, and in understanding and controlling the spin dependent electron transport. And materials exist that allow building thermally stable magnetic particles down to sizes of a few nm [52], seemingly opening a bright future for a high density "spin storage".

Writing is the problem

But the old use of a magnetic field to write the information still remained a major limitation. This can be understood easily. Let's assume that information is stored on the magnetization orientation of a nanoparticle of volume V. The energy barrier fighting the thermal excitations is given by KV, where K is the anisotropy constant per unit volume. Non volatility — usually defined by a maximum error rate, e.g. 10^{-9}, on a 10 years period — is obtained when KV > 50-60 $k_B T$, where k_B is the Boltzmann constant and T the temperature. So reducing V requires increasing K accordingly, but then the writing field increases proportionally with K while the power available to create it decreases with downscaling the dimensions.

The problem is well known in HDD, where it was recently postponed by first introducing the SAF longitudinal media and then changing to perpendicular recording. The future also

promises heat assisted magnetic recording (HAMR) [1], where the magnetic field is helped by local heating of the media temporarily reducing the energy barrier, as in magneto-optical recording. But the fundamental limit is still there, together with other problems linked to the rotating nature of HDD storage such as mechanical tracking, slow access time (hardly reduced in several decades and still a few ms) and energy consumption. The future markets of HDD, in particular through the competition with Flash storage, will depend on how such problems will be solved. For instance, HDD currently maintains a roughly 40% areal density growth rate, in line with Moore's law defining the minimum cell size of Flash. But meanwhile multilevel Flash cells were introduced (2 bits/cell), and huge efforts succeeded in reducing their cost.

In MRAM the writing problem was immediately worse than in HDD, as the conducting lines have much smaller dimensions, with a strong limitation in current density around 10^7 A/cm^2 due to electromigration. Also, it is not possible in a VLSI circuit to include an optimized "ring-like" ferromagnetic circuit to "channel" the magnetic induction to the magnetic media. A magnetic channelling was developed for MRAM [53], but the effect is limited (to a factor of about 2) and requires costly fabrication steps. Finally, when approaching the downscaling limits the unavoidable distribution of writing parameters, coupled to the large stray fields in such densely packed arrays, leads to spreading program errors. This reliability problem was elegantly solved by Freescale researchers by replacing the standard ferromagnetic free layer by a SAF layer, written using a spin-flop process [33, 51, 54], and this opened the way to the first MRAM product. But this is at the expense of higher writing currents (circa 10mA), and clearly limits the achievable densities and the downscaling. As for HDD, one solution could be heat assisted recording (TAS-RAM) [43, 55]. It was also proposed to assist writing by microwave excitation at the ferromagnetic resonance frequency of the free layer [56, 57, 58], a technique that could also be useful for hard disk. But such promising techniques do not completely suppress the need for a magnetic field.

Spin transfer: a new route for writing magnetic information

The well hoped for breakthrough for spin storage was provided by the prediction in 1996 [59, 60] that the orientation of the magnetization of a "free" magnetic layer can be controlled by direct transfer of spin angular momentum from a spin-polarized current. The first experimental demonstration that a Co/Cu/Co CPP spin-valve nanopillar can be reversibly switched by such "spin transfer effect" between its low (parallel) and high (antiparallel) magnetoresistance states was presented in 2000 [61]. The concept of "spin transfer" actually

dates back to the seventies, with the prediction [62] and observations (cf [63]) of domain wall dragging by currents. Spin transfer effects had also been predicted for MTJs as early as 1989 [64]. Somehow, those predictions did not immediately trigger the intense research work that followed the 1996 and 2000 publications, maybe because the required fabrication technologies were not mature enough.

The principle of the so-called *"spin transfer torque"* (STT) writing in nanopillars is schematized in Figure 6a for the usual case of 3d ferromagnetic metals (e.g. Co) in a SV structure with a non magnetic metal spacer (e.g. Cu). Let's consider a "thick" ferromagnetic layer F1, while the ferromagnetic layer F2 and the spacer M are "thin" (compared to the length scales of spin polarized transport, cf [65]). F1 and F2 are initially magnetized along different directions. A current of s electrons flowing from F1 to F2 will acquire through F1, acting as a "spin polarizer", an average spin moment approximately along the magnetization of F1. When the electrons reach F2, the s-d exchange interaction quickly aligns the average spin moment along the magnetization of F2. In the process, the s electrons have lost a transverse spin angular momentum which, because of the total angular momentum conservation law, is "transferred" to the magnetization of F2. This results in a torque tending to align F2 magnetization towards the spin moment of the incoming electrons, hence towards the magnetization of F1. Because the loss of transverse spin momentum happens on a very sort distance (circa 1nm), the torque is an interfacial effect, more efficient on a thin layer. But a more important result is that the amplitude of the torque per unit area is proportional to the injected current density, so that the writing current decreases proportionally to the cross section area of the structure. With today's advances in nanotechnologies and the easy access to sizes below 100 nm, this represents an important advantage of spin transfer on field induced writing.

A realistic treatment of the effect [65] includes both quantum effects at the interfaces (spin dependent transmission of Bloch states) and diffusive transport theory (spin accumulation effects), while the dynamical behaviour can be studied through a modified Landau-Lifshitz-Gilbert equation describing the damped precession of magnetization in the presence of spin transfer torque and thermal excitations [65, 66]. The principle of STT writing of a MRAM cell is shown in Figure 6b. Electrons flowing from the thick "polarizing" layer to the thin "free" layer favour a parallel orientation of the magnetizations: if the initial state is antiparallel, then beyond a threshold current density j_{C+} the free layer will switch. When the electrons flow from the free to the polarising layer, one can show that the effective spin

moment “injected” in the free layer is opposed to the magnetization of the polarizing layer, writing an antiparallel configuration beyond a threshold current density j_{C-}.

Since the first observation on Co/Cu/Co trilayers, STT writing was observed on many different stacks, including exchange bias pinned layers and SAF layers [67]. It works also with tunnel junctions [68], and in particular with MgO tunnel barriers [69]. Moreover, the threshold current densities are becoming nearly compatible with NMOS transistor output as predicted by ITRS roadmap. And in a near future, TAS and STT writing modes could be associated, for an even smaller switching current.

Companies have already presented several demonstrators of the so-called “Spin-RAM” [70, 71]. As shown in Figure 7, the cell structure has now become extremely simple, which opens the way to high densities. Is it enough to compete with NAND Flash on mass data storage in standalone memories? In terms of areal density, Flash still offers a smaller multi-bits cell, and announces “3D” stacking [72]). However, MRAM has other advantages such as potentially infinite endurance (against ~10^5 cycles for a Flash) and potential for sub-ns operation [66, 73, 74], that makes it competitive as “universal” memory.

Perspectives

One major limitation to ultrahigh density Spin-MRAM is the requirement of one transistor per cell (1T/1MTJ). The cross-point memory architecture provides a way of reaching very high densities ($4F^2$ cell area) [75], lower fabrication costs, and a potential for 3D stacking of several recording layers. Intermediate cell structures such as 1T/4MTJ [76] have also been proposed. Multi-level cell operation was also recently achieved in TAS-RAM [77]. But in all cases increased density is obtained at the expense of smaller signal amplitude and thus much slower read.

One step to at least partially fight these limitations would be to gain at least one order of magnitude on the amplitude of the magnetoresistance, towards a true “current switch” with $\Delta R/R$ values for comparable, for example, to those of phase change P-RAM. This could be achieved by replacing metallic ferromagnetic layers by 100% spin polarized conductors such as half metallic oxides [78] or Heussler alloys [79, 80], or diluted magnetic semiconductors (DMS) [81, 82]. DMS furthermore open the way to new effects such as tunnelling anisotropic magnetoresistance [83, 84], and for the long term to quantum dot storage devices [85].

Another promising concept is that of the “spin filter” [86] where tunnelling happens through a ferromagnetic barrier: the transmission varies exponentially with the square root of the barrier

height, which itself depends on electron spin direction versus barrier magnetization. Such developments would of course benefit also to HDD.

Another approach is to build a 3-terminals device that can provide for transistor effect and magnetoresistance in a single magnetic device [87, 88, 89].

All these ideas show promising results at low temperature, but depend on materials issues such as obtaining Curie temperatures well above room temperature, mastering a complex stoechiometry (oxides, Heussler alloys) at an interface, or maintaining the fabrication thermal budget compatible with CMOS process when these new materials usually require specific high temperature growth. Moreover, 3-terminal devices can so far provide only very small currents, in the µA range at most, below CMOS compatibility levels, while independent writing of one or two magnetic layers may prove quite difficult to scale down even using spin transfer.

Future magnetic mass storage could rather come from domain wall (DW) devices, in an approach conceptually very near that of the former “bubble” magnetic memories [90]. File architecture for mass storage does not require random access to single bit or word as proposed in Spin-RAM, but can accommodate random access only to large sectors in which binary information is written or read sequentially, such as in HDD. A chain of DWs in a magnetic stripe can indeed represent such a sector storing binary information, but a simple application of a uniform magnetic field would immediately destroy it by annihilating the reverse domain. It was first proposed [91, 92] to use an oscillating magnetic field, uniform over the whole chip, acting on a specific DW circuit behaving as a shift register: the global character of the applied field makes downscaling and 3D stacking achievable [93]. Even more promising for very high density solid-state integration, a current injected in the magnetic stripe applies the same pressure to all domain walls along the direction of electrons travel, propagating the walls simultaneously at the same speed, without loosing information. This mimics the fast passing of bits in front of the head in HDD recording, but here there is no moving part (hence increased ruggedness) and addressing a sector would be done by CMOS electronics at µs access times. The scheme thus opens the way to very compact “storage track memory devices” [94], and could also be used in a new kind of MRAM [95] (Figure 8). However many crucial advances are needed before its practical implementation.

The theory mixes spin transfer torque (electrons crossing a domain wall transfer spin angular momentum to the non uniform magnetization in the wall) and mechanical momentum transfer (electrons are reflected on narrow walls), leading to a DW propagation controlled with a current density beyond a threshold [96, 97]. The effect was indeed observed in metals

magnetized in plane [98, 99] and perpendicular to plane [100], or in DMS [101] (with orders of magnitude lower currents but much higher resistance and other problems). However, even qualitative agreement between experience and theory is not straightforward [102, 103].

On the experimental aspect, crucial progress has to be made to reliably control domain wall propagation with low current densities. One must first provide non volatile reliable trapping of the domain walls at dedicated positions in the "data sector". Most works use simple notches [104, 105], while more elaborate pinning profiles have also been proposed [106, 107]. But not much has been published on the evolution of the thermal stability of the pinning when downscaling the dimensions. Besides, already in a parallel stripe and even more at artificial notches with distribution of patterning defects, domain walls can take different structures of nearby energy and may even change structure under a current pulse [105, 108, 109, 110]. This is a potential problem for reliable operation, because the parameters of current induced propagation should depend on the wall structure. Last but not least, the threshold current density necessary to depin a DW from a trap, or even to start motion in a parallel stripe, is still too high for applications (above a few 10^6 A/cm^2). Drastic progress has been done recently by using the natural radiofrequency dynamics of a domain wall pinned in a potential well [111, 112, 113]. Note however that, if the current density is still too high, the cross section of a thin film stripe is intrinsically small so the threshold current is already much smaller than what is available from the smallest CMOS transistors, a key asset for developing low power data storage devices (Figure 8B). Finally, the achievable DW speed is also a crucial issue for fast data rates [114, 115, 116, 117]. For instance, with maximum DW speed around 100 m/s and an on-track linear density of one DW every 200 nm, already very demanding values, the data rate would be around 0.5 Gbit/s. This would be in line with today's HDD data rates, but is far from being demonstrated.

On the long term, even higher densities could be reached by replacing domain walls by smaller magnetization vortices [118], in a trend similar to that from bubble to Bloch line memories, cf [90].

We have tried in this paper to share our amazement at the outstanding progress undergone by spin electronics in the last 2 decades, under the convergence of a chain of scientific breakthroughs and technology advances. From a fundamental point of view, if in 1988 the giant magnetoresistance opened the way to control transport through magnetization, "spin transfer" now allows to control magnetization by transport, closing the loop for **a new paradigm,** from magnetic recording to spin storage. Traditional hard disk recording has gained orders of magnitude in storage capacity, thus entering the consumer electronics

markets. And the MRAM magnetic solid state memory is now in production, although yet only for niche markets.

But the intrinsic speed and endurance of magnetic recording, together with the potential of the Spin-RAM to work with CMOS compatible electrical parameters, can open the way to applications where data storage would not be the primary objective while non volatility would still be a key asset. Along this line, it has been proposed for instance to perform logic calculations through magnetic interactions, in magnetic Quantum Cellular Automatas [119, 120], or in domain wall logic [92], for low power massively parallel logic operations under a uniform cyclical magnetic field. MTJs can also be used for logic calculation, either directly [121] (a nice idea but its practical realization is uncertain), or by a dense integration of MTJs into CMOS logic circuits [122, 123] where they bring instant on/off, run time re-programmability, and overall enhanced operation safety. Magnetism would thus enter the realm of the CPU. But a major step forward would be to realize three terminal spin electronic devices that would allow packing a complete programmable logic function into a single nanodevice. Let's assume a source-gate-drain 3-terminal device where one could independently control the magnetization of magnetic source and drain, injecting spin polarized electrons into a channel of spin dependent transmission that could also be controlled by a gate voltage. Such a device has multiple inputs to control a multilevel output, realizing a logic function that can be programmed through the non volatile magnetic configurations. The first proposition of this kind [18], despites recent progress in injecting spin polarization into semiconductors [124], has not yet achieved any practical realization. New concepts are being proposed [125, 126, 127], and more could be realized for instance with molecules [128, 129, 130, 131, 132]. On a more long term, the use of spin injection and spin currents [21, 133] may lead to the development "spin logic" devices [134].

Ultimately, "magnetic" writing will again become a drastic problem in much smaller and more complex device, and new routes have to be found. As in nanoelectronics, zero current gate voltage controlled writing would be ideal. Preliminary results have recently been obtained by using interfacial coupling with piezoelectric or even multiferroic materials [135, 136, 137], or through electric field control of ferromagnetism in DMS [138, 139]. In an even more futuristic approach, switching by spin currents only (no charge currents) has been announced [140], in a pioneering step towards spin currents only nanoelectronics. As a whole, finding solutions to the magnetic writing problem may prove to be a key issue on the way to future spin electronics, as it has been one for passed evolution of magnetic recording.

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Competing financial interests

The authors declare no competing financial interests.

Figure legends

Figure 1: **The magnetoresistive head for hard disk recording.** Schematic structure of the magnetoresistive head introduced by IBM for its hard disk drives in 1991, adapted from reference [1]. A magnetic sensor based on anisotropic magnetoresistance (left) is added to the inductive "ring type" head (right) still used for writing. The distances P1-P1' and P1-P2 between the pole pieces of the magnetic shields S1 and S2 define respectively the "write" and "read" gaps, of which depend the minimum length B of the magnetic domains. W is the track width and t is the thickness of the recording medium. Note that, in today's hard disk recording, W and B are of the order of respectively 100 nm and 30 nm, with however a different arrangement of head and domains in so called "perpendicular recording" [1].

Figure 2: **The spin valve. (A)** Schematic representation of the spin valve effect in a tri-layer film of two identical ferromagnetic layers F1 and F2 sandwiching a non magnetic metal spacer layer M, the current circulating "in plane". When the two magnetic layers are magnetized parallel (P, bottom scheme), the "spin up" electrons (spin antiparallel to the magnetization) can travel through the sandwich nearly unscattered, providing a conductivity shortcut and a low resistance. On the contrary, in the antiparallel (AP, top scheme) case both "spin up" and "spin down" electrons undergo collisions in one or the other F layer, giving rise to a higher overall resistance. **(B)** Schematic arrangement of the "current in plane" (CIP) spin valve sensor in a read head. (C). Schematic arrangement of the "current perpendicular to plane" (CPP) spin valve sensor in a read head. In both configurations, the recording media travels parallel to the front face of the sensor.

Figure 3: **Spin accumulation.** Schematic representation of the spin accumulation at an interface between a ferromagnetic metal and a non magnetic layer, adapted from reference [132]. (A) Spin-up and spin-down current far from an interface between the ferromagnetic and nonmagnetic conductors (outside the spin-accumulation zone). $L_{sf}^{(F)}$ and $L_{sf}^{(M)}$ are respectively the spin diffusion length in the ferromagnetic and non magnetic layers. (B) Splitting of the Fermi levels E_{Fup} and E_{Fdown} at the interface. The dashed green arrows symbolize the transfer of current between the two channels by the unbalanced spin flips due to the out of equilibrium spin-split distribution, and which governs the depolarization of the electron current between the left and the right. With an opposite direction of the current, there is an inversion of the spin accumulation and opposite spin flips, which polarizes the current

across the spin-accumulation zone. (C) Variation of the current spin polarization when there is an approximate balance between the spin flips on both sides (metal/metal) and when the spin flips on the left side are predominant (metal/semiconductor for example). j_{up} (resp. j_{down}) are the current densities for “spin up” (resp. “spin down”) electrons.

Figure 4: **The magnetic tunnel junction. (A)** Schematic representation of the tunnel magnetoresistance in the case of two identical ferromagnetic metal layers separated by a non magnetic amorphous insulating barrier such as Al_2O_3. The tunnelling process conserves the spin. When electron states on each side of the barrier are spin polarized, then electrons will find more easily free states to tunnel to when the magnetizations are parallel (top picture) than when they are antiparallel (bottom picture). **(B)** Record high magnetoresistance TMR=(R_{max}-R_{min})/R_{min} for the magnetic stack: $(Co_{25}Fe_{75})_{80}B_{20}$(4nm)/MgO(2.1nm)/$(Co_{25}Fe_{75})_{80}B_{20}$(4.3nm) annealed at 475°C after growth, measured at room temperature (black circles) and at 5 K (open circles), taken from reference [31]. **(C)** TEM cross section of a TMR read head from Seagate, taken from reference [32]. The tunnel junction stack appears vertically at the center of the picture, with the tunnel barrier at the level of the thin white horizontal line. The thick bended lines on both sides are the insulating layers between top and bottom contacts. The two thick light gray layers on top and bottom are the magnetic pole pieces (cf Figure 1).

Figure 5: **The Magnetic Random Access Memory. (A)** Principle of the magnetic random access memory MRAM, in the basic “cross point” architecture. The binary information “0” and “1” is recorded on the two opposite orientations of the magnetization of the free layer of magnetic tunnel junctions (MTJ), which are connected to the crossing points of two perpendicular arrays of parallel conducting lines. For writing, current pulses are sent through one line of each array, and only at the crossing point of these lines the resulting magnetic field is high enough to orient the magnetization of the free layer. For reading, one measures the resistance between the two lines connecting the addressed cell. **(B)** To remove the unwanted current paths around the direct one through the MTJ cell addressed for reading, the usual MRAM cell architecture add one transistor per cell, resulting in more complex 1T/1MTJ cell architecture such as the one represented here. **(C)** Photograph of the first MRAM product, a 4 Mbit standalone memory commercialized by Freescale in 2006, taken from the reference [33].

Figure 6: **Spin transfer switching. (A)** Principle of the “spin transfer torque” (STT) effect, schematized for a typical case of a Co(F1)/Cu/Co(F2) trilayers pillar. A current of s electrons

flowing from the left to the right will acquire through F1, assumed to be thick and acting as a "spin polarizer", an average spin moment along the magnetization of F1. When the electrons reach F2, the s-d exchange interaction quickly aligns the average spin moment along the magnetization of F2. To conserve the total angular momentum, the transverse spin angular momentum lost by the electrons is transferred the magnetization of F2, which senses a resulting torque tending to align its magnetization towards F1. **(B)** Principle of STT writing of a MRAM cell: reversing the current flowing through the cell will either induce parallel or antiparallel orientation of the two ferromagnetic layers F1 and F2.

Figure 7. **The Spin-RAM. (A)** Schematic architecture of a Spin-RAM (a) Scheme of the memory cell, and (b) tentative architecture of the cell array, taken from the reference [70]. **(B)** Resistance versus current hysteresis loop of a Spin-RAM cell, taken from reference [71]. The different colours show the evolution of the loop after an increasing number (up to $1G=10^9$) of writing cycles (100ns pulses of successively positive and negative currents, cf insert). This demonstrates an excellent stability.

Figure 8: **Domain wall storage devices.** Examples of storage devices using current induced domain wall (DW) propagation. **(A)** In the concept first proposed by S.S.P. Parkin [94], the binary information is stored by a chain of DWs in a magnetic stripe. An electrical current in the stripe, by applying the same pressure to all the DWs, moves them simultaneously at the same speed for a sequential reading (or writing) at fixed read and write heads. A reverse current can move the DWs in the opposite direction for resetting, or in an alternative solution the DWs might turn on a loop. This mimics the fast passing of bits in front of the head in HDD recording, but here there is no moving part and addressing a sector would be done by CMOS electronics at µs access times. The initial scheme in reference [94] proposes to store data in vertical stripes: this would open the way to very compact high capacity "storage track memory devices". Other schemes now propose multilayers of in plane domain tracks, easier to fabricate. **(B)** Scheme of a MRAM cell using domain wall propagation from one stable position to another on either side of a magnetic tunnel junction (cf reference [95]).

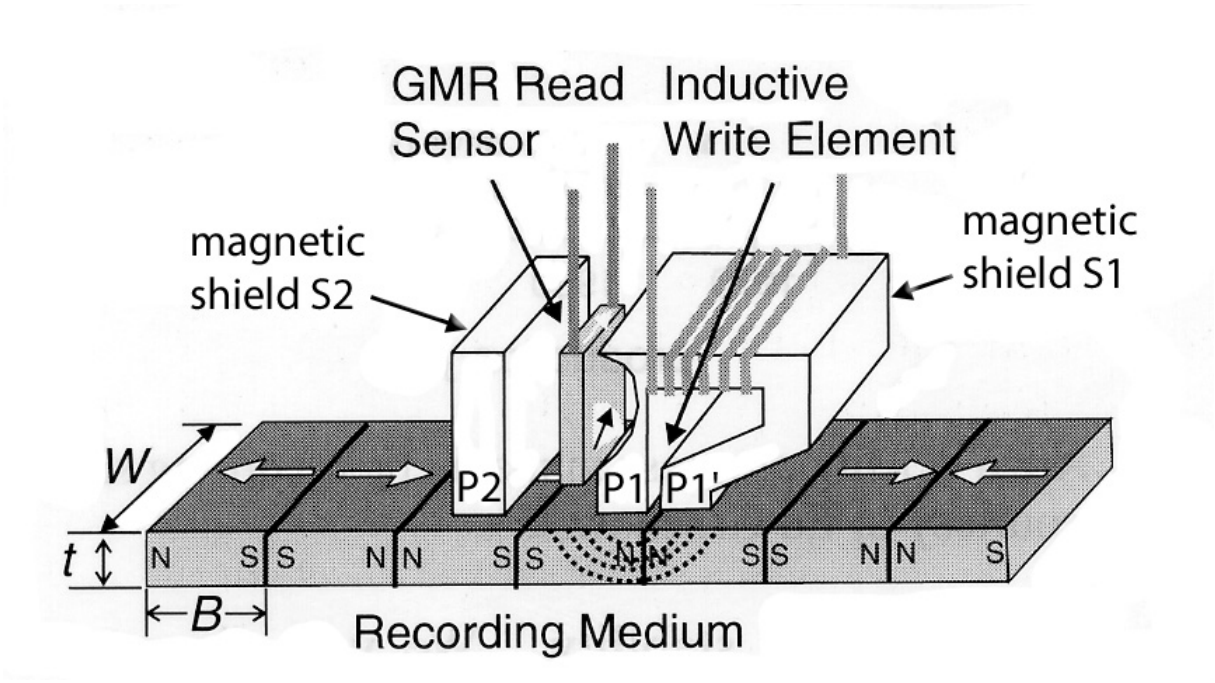

Figure 1

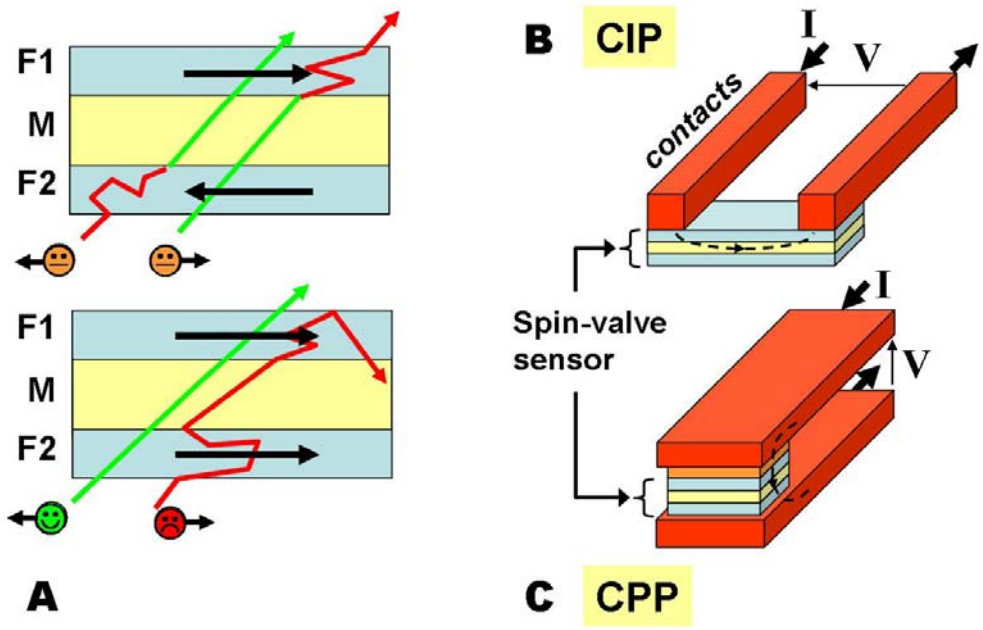

Figure 2

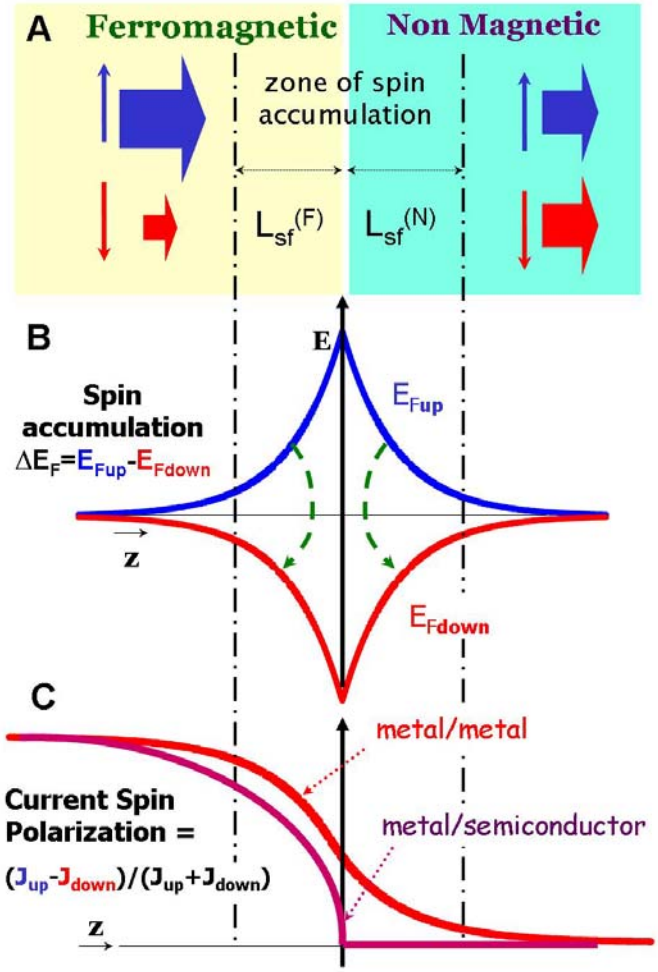
A
Ferromagnetic
Non Magnetic
zone of spin accumulation
$L_{sf}^{(F)}$
$L_{sf}^{(N)}$
B
E
Spin accumulation
$\Delta E_F = E_{Fup} - E_{Fdown}$
E_{Fup}
z
E_{Fdown}
C
metal/metal
Current Spin Polarization =
$(J_{up} - J_{down})/(J_{up} + J_{down})$
metal/semiconductor
z

Figure 3

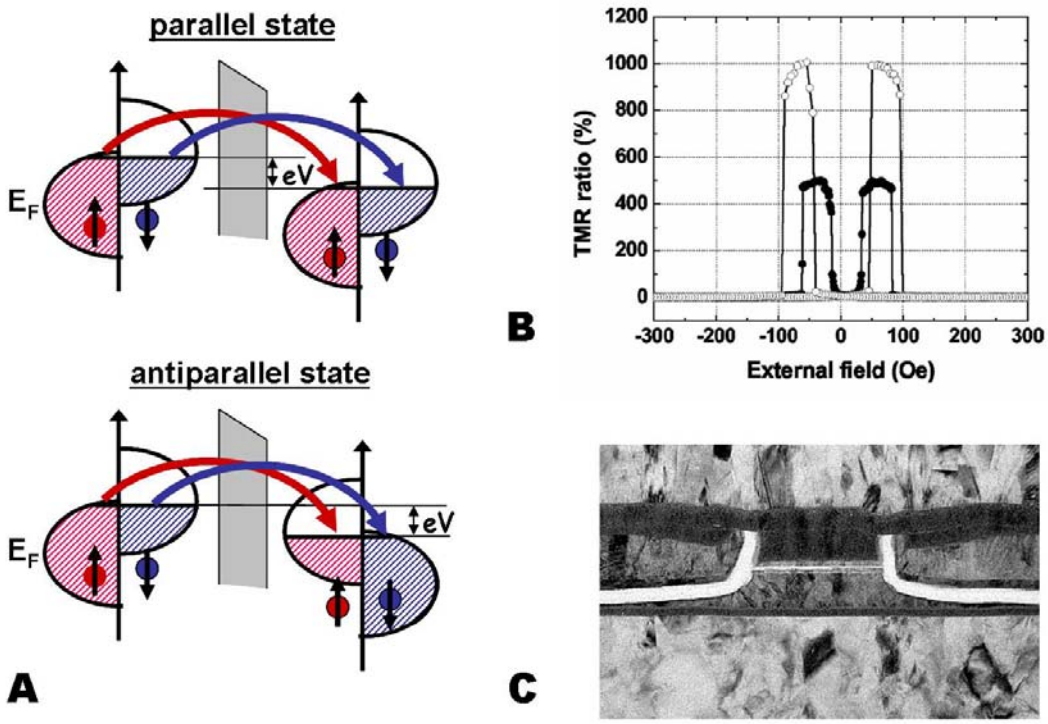

Figure 4

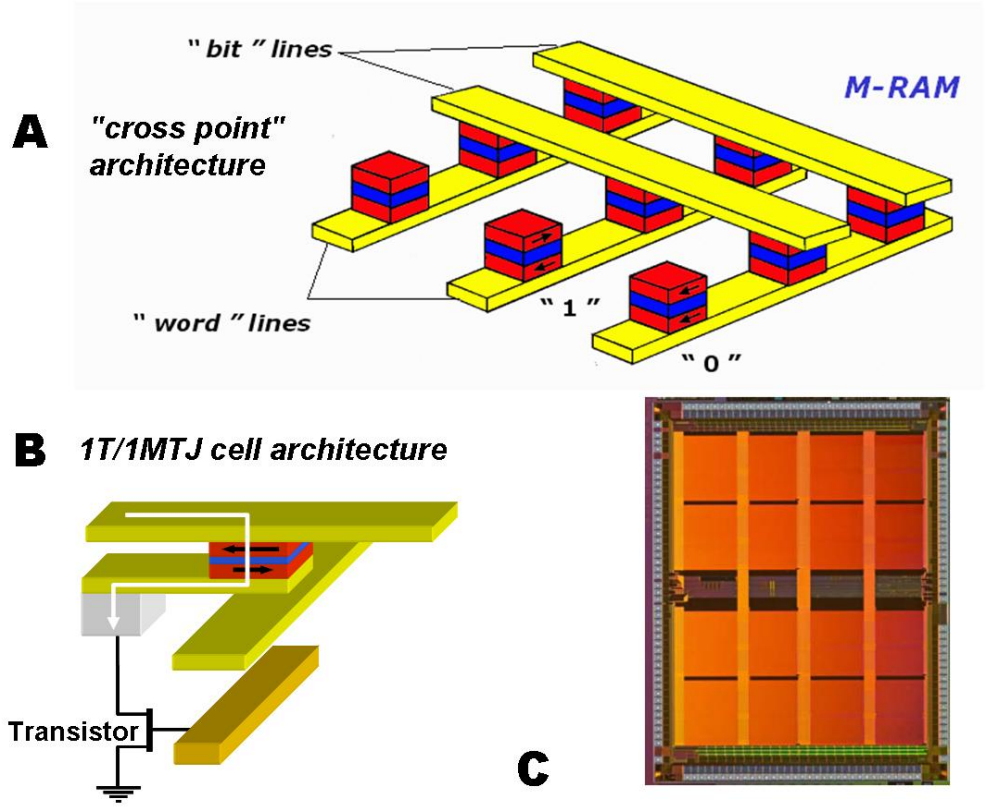

Figure 5

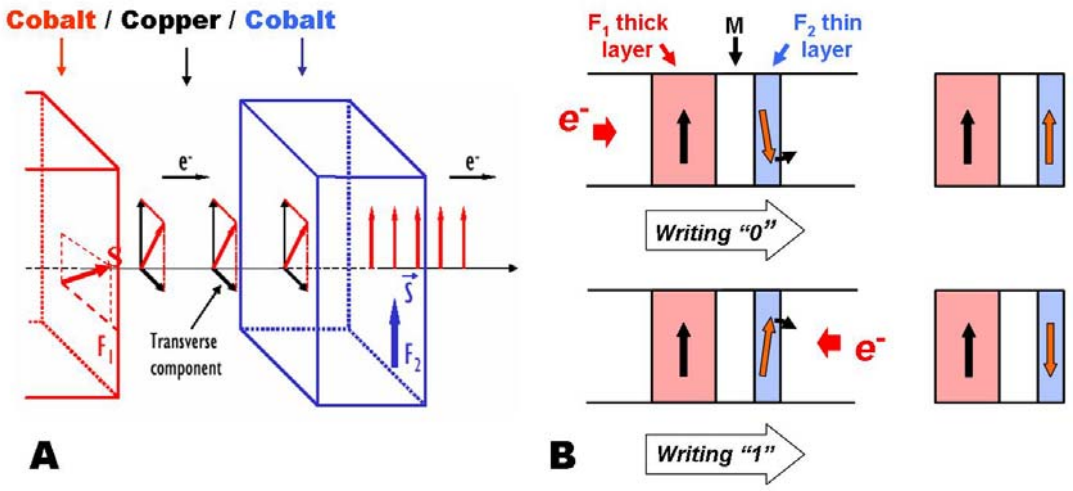

Figure 6

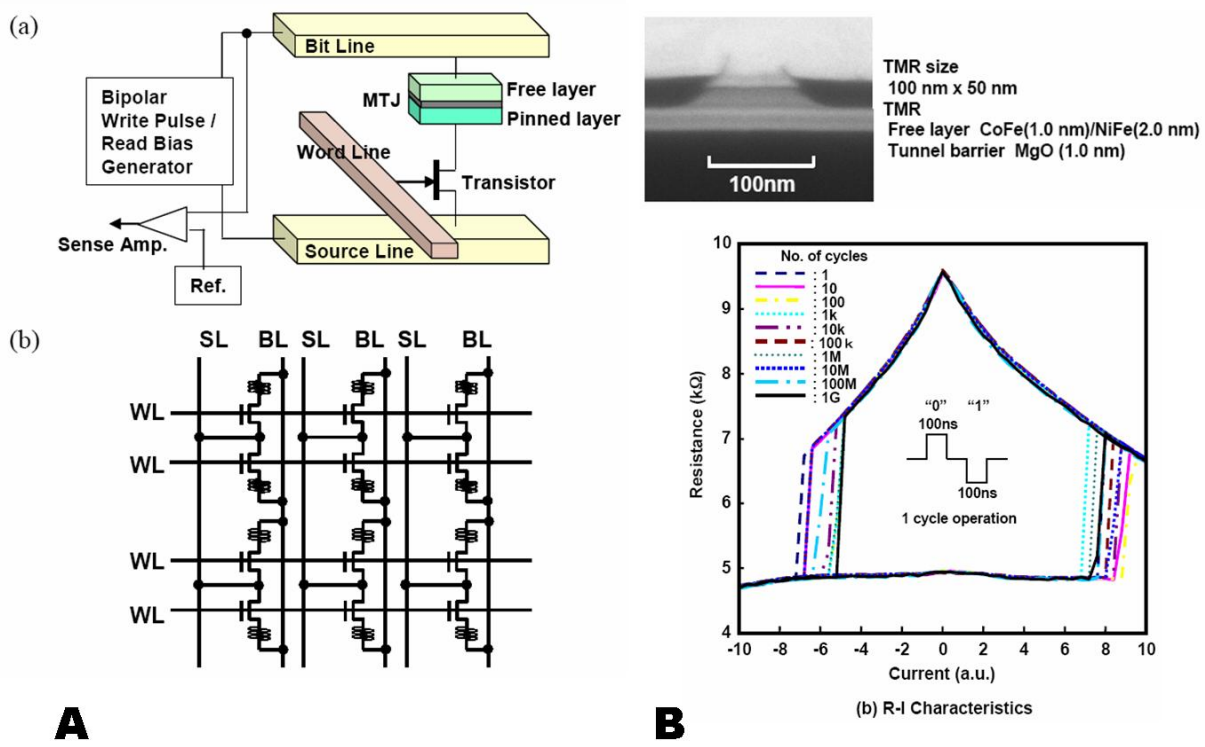

Figure 7

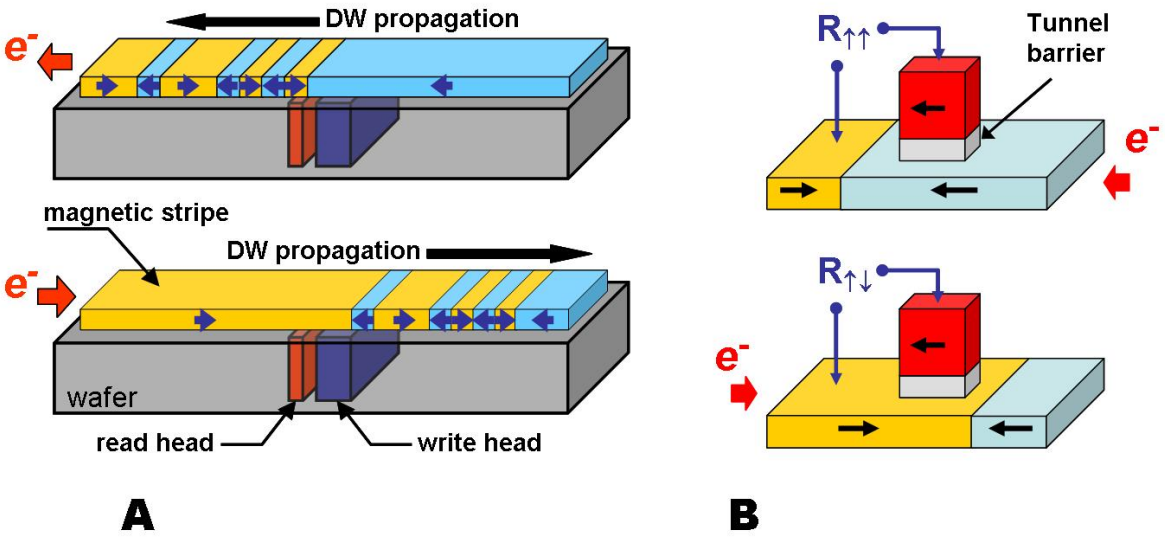
DW propagation
e-
magnetic stripe
DW propagation
e-
wafer
read head
write head
A
R↑↑
Tunnel
barrier
e-
R↑↓
e-
B

Figure 8