The Essence of the Little Box Challenge-Part B: Hardware Demonstrators & Comparative Evaluations

Dominik Neumayr, Dominik Bortis, and Johann Walter Kolar

***Abstract*—In order to expedite the development of power electronic systems towards higher power density and efficiency at a lower cost of implementation, Google and IEEE initiated the Google Little Box Challenge (GLBC) aiming for the worldwide smallest 2 kVA/450 VDC/230 VAC single-phase PV inverter with η > 95% CEC weighted efficiency and an air-cooled case temperature of less than 60 °C by using latest power semiconductor technology and innovative topological concepts. This paper, i.e. Part B of a discussion of The Essence of the Little Box Challenge, presents the hardware implementations and novel control concepts of two GaN-based inverter systems selected by the authors to counter the challenge: (i) Little Box 1.0 (LB 1.0), a H-bridge inverter with two interleaved bridge-legs both operated with Triangular Current Mode (TCM) modulation which features a power density of 8.18 kW/dm^3 (134 W/in^3) and a nominal efficiency of 96.4% and (ii) Little Box 2.0 (LB 2.0), an inverter topology with single bridge-leg DC/|AC| buck-stage operated with constant frequency PWM and a subsequent |AC|/AC H-bridge unfolder, which features a remarkable power density of 14.8 kW/dm^3 (243 W/in^3) and a nominal efficiency of 97.4%. Implemented using latest GaN power semiconductor technology, Zero Voltage Switching (ZVS) throughout the AC period and a variable switching frequency in the range of 200 kHz–1 MHz in order to shrink the size of filter passives, the LB 1.0 was ranked among the top 10 out of 100+ teams actively participating in the GLBC. The LB 2.0 is the result of further research and considers lessons learned from the GLBC and achieves despite moderate 140 kHz constant frequency PWM and hard-switching around the peak of the AC output current a higher power density ρ and a higher efficiency η. For both implemented prototypes experimental results are provided to confirm that all GLBC technical requirements are met. The experimental results include steady-state and step-response waveforms, EMI and ground current measurements, as well as efficiency and operating temperature measurements. The reason for the $\eta\rho$-performance improvement of LB 2.0 over LB 1.0 are then discussed in detail. Furthermore, the solutions of other GLBC finalists are described and then compared to the performance achieved with the hardware prototypes presented in this paper. This leads to findings of general importance and provides key guideline for the future development of ultra-compact power electronic converters.**

***Index Terms*—GaN, high power density, little box challenge, microinverter, power pulsation buffer, PV inverter, WBG, zero voltage switching.**

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I. Introduction

In Part A of the paper at hand [1], the key design challenges and the technical concepts adopted by the authors to implement an ultra-compact single-phase inverter and overcome the Google Little Box Challenge (GLBC, [2]) were described in detail and are briefly summarized in the following. In order to drastically shrink the size of the converter bridge-legs and EMI filter passives and break through the status quo in power density, GaN wide bandgap (WBG) semiconductor technology was selected by the authors to enable a high switching frequency in the range of 100 kHz–1 MHz [3]. By means of the widely accepted Triangular Current Mode (TCM) control technique [4], [5], Zero Voltage Switching of a bridge-leg can be achieved in every operating point throughout the AC period which results in low switching losses despite the high switching frequencies but requires a Zero Crossing Detection (ZCD) circuitry and sophisticated FPGA control for a robust implementation. In contrast to TCM control, conventional PWM features a constant switching frequency but suffers from high turn-on switching losses which limits the maximal feasible switching frequency. However, this drawback is mitigated by the fact that with a relatively large current ripple, i.e. a design with small filter inductance value, also for PWM the average switching losses can be considerably reduced and a switching frequency of up to a few hundreds of kHz is feasible. As GaN semiconductor technology enables both soft- and hard-switching in a totem-pole bridge-leg configuration (as opposed to Si MOSFETs), both bridge-leg control strategies were considered for the implementation of the Google Little Box inverter. Furthermore, the authors selected a 2-level implementation of the bridge-legs over a multilevel implementation because of the anticipated increase in volume introduced by the higher semiconductor count, the increased gate driving requirement (supply voltage and gate signal isolation), and because of the more involved control system to facilitate capacitor balancing under all operating conditions. In order to reduce the size of the energy storage required to cope with the 120 Hz power pulsation intrinsic to single-phase DC/AC converter system, the advantage of replacing bulky electrolytic DC-link capacitors with an additional auxiliary converter and well utilized buffer capacitors was emphasized in Part A of the paper. Among several concepts presented in literature, the buck-type Parallel Current Injector (PCI) buffer as depicted in Fig. 1(a) and (b) (cf. Fig. 3 and 11) [6]–[9], was selected by the authors to cope with the pulsating AC power since (i) it features excellent capacitor utilization and

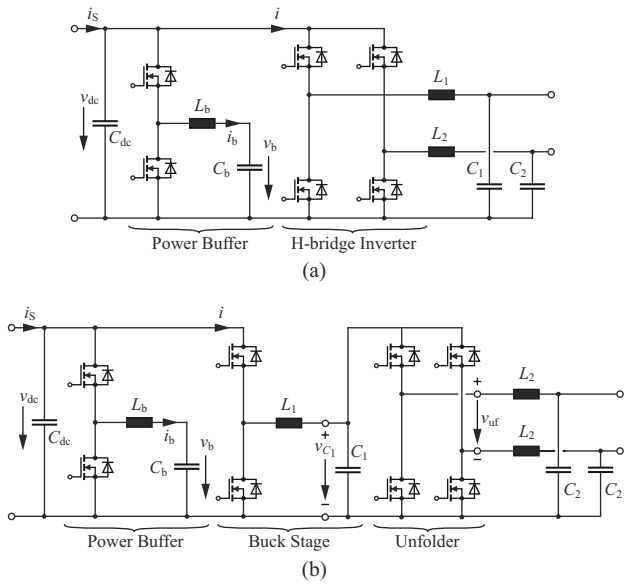

Fig. 1. (a) H-bridge inverter with DC-link referenced output filter and buck-type Parallel Current Injector (PCI) active power buffer (Little Box 1.0). (b) DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter with PCI active power buffer (Little Box 2.0).

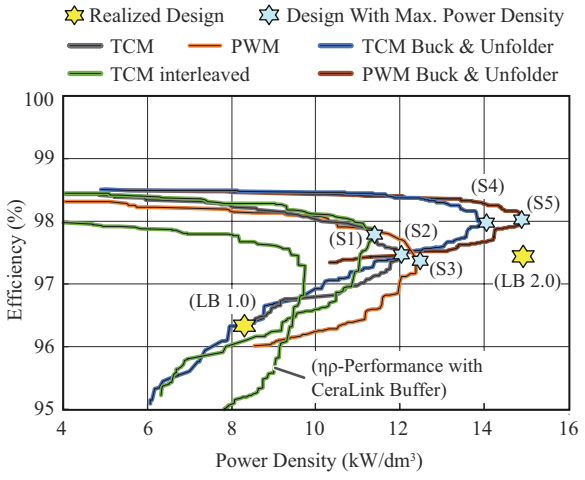

Fig. 2. Computed $\eta\rho$-performance of selected inverter concepts including the active power buffer for different operating modes (TCM/PWM) and with/without interleaving of bridge-legs. Also indicated is the actual performance achieved with the implemented hardware prototypes as presented in this paper.

(ii) allows to employ the same bridge-leg design as used in the main inverter to achieve maximal performance with minimal increase of overall complexity. As a consequence of the large feasible buffer voltage ripple, comparably small capacitance values in the range of 100–200 µF are needed, thus realizing the buffer capacitor with ceramic capacitor technology becomes a viable option. Since the effective energy density of electrolytic capacitors is reduced due to lifetime related current stress constraints, 2.2 µF/450 V class II X6S MLCC and 2 µF/500 V CeraLink capacitors were identified to be the most promising candidates for realizing an ultra-compact power buffer and are adopted for the implementation of the buffer capacitor [10]–[12]. Regarding the specified ground current requirements of 50 mA (revised from initially specified 5 mA), the difference between a 1 or 2 HF bridge-leg inverter design regarding the generation of a Low-Frequency (LF) Common-Mode (CM) output voltage component was analyzed and the merits of a DC-link referenced filter structure which allows a combined DM and CM filtering in a single stage was highlighted in Part A of the paper. Concerning the EMI requirements of the GLBC, the concept of 4D-interleaving [13] was introduced which allows to operate the interleaved bridge-legs with an optimal overlapping interval (with respect to the AC period) for maximal conversion efficiency while meeting the EMI requirements. Furthermore, to dissipate the generated power losses during operation of the inverter, a parallel-fin type heat sink with both ultra-flat blowers and conventional fans was considered by the authors for the optimal implementation of the forced-air cooling systems. It was identified that a heat sink using blowers performs best for comparably long cooling units offering a large baseplate area for direct component attachment, and a Because of the flat dimensions of the blower, a sandwich-like arrangement with two heat sinks at the top and bottom and the converter in the center is possible (cf. Fig. 4). a heat sink design using fans performs best when the total length of the cooling unit is comparably short. Thus, this configuration is well suited for a component arrangement where only the power transistors are attached to the heat sink and the filter passives are cooled by the air flow exiting the heat sink (cf. Fig. 12).

Based on these key design considerations, two inverter concepts, (i) the H-bridge inverter with DC-link referenced output filter as shown in Fig. 1(a) (denominated as Little Box 1.0, LB 1.0, in the following) and (ii) the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter topology as shown in Fig. 1(b) (denominated as Little Box 2.0, LB 2.0, in the following), both equipped with a buck-type PCI buffer to cope with the pulsating AC power, were selected for further analysis and a comparative evaluation. The results of a comprehensive multi-objective $\eta\rho$-Pareto optimization described in Part A (cf. Fig. 2 and Fig. 18(a) of Part A) indicate that, despite of higher switching losses, operation with constant switching frequency just below 150 kHz PWM achieves a higher power density compared to TCM control. This is explained by the fact that, for the given GLBC specifications and the performance of the employed GaN semiconductor technology, the loss savings of operating with Zero Voltage Switching (ZVS) throughout the AC period are less compared to the added conduction losses caused by the high RMS current and remaining ZVS switching losses resulting from the TCM control. Furthermore, it is shown that with the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter operated with PWM and a comparably large current ripple (small buck-stage filter inductance value) a power density of 14.7 kW/dm^3 (240 W/in^3) with an efficiency of up to 98 % at 2 kW output power is possible. Compared to the H-bridge inverter concept, this inverter therefore features a ≈ 15%–20% higher power density and a 1.7% higher efficiency at 2 kW rated power.

In this paper, i.e. Part B of a discussion of The Essence of

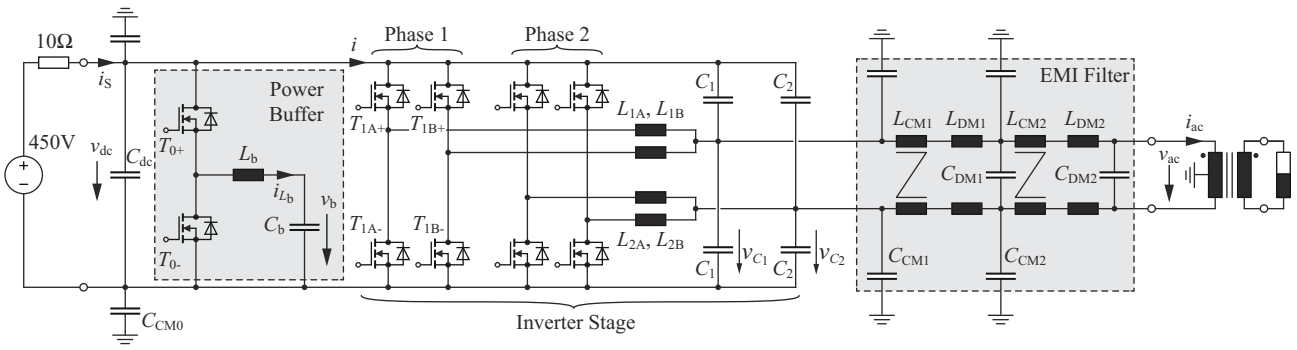

Fig. 3. Topology of the inverter denominated as Little Box 1.0 (LB 1.0) realized according to the Google Little Box Challenge (GLBC) technical specifications (cf. Table I in Part A) with the original 5 mA ground current limit. The systems consists of a H-bridge inverter with two interleaved bridge-legs per phase and a subsequent EMI output filter. The DC-side energy storage to compensate the fluctuating AC power is realized with a buck-type Parallel Current Injector (PCI) active power buffer.

the Little Box Challenge, the claimed $\eta\rho$-performance of the considered inverter concepts is confronted with the actually achieved performance figures of realized hardware prototypes (cf. LB 1.0 and LB 2.0 in Fig. 2). In Section II, the hardware prototype and results of experimental measurements on the LB 1.0, i.e. a 2-level H-bridge based inverter topology with interleaved bridge-legs, TCM operation with variable switching frequency in the range of 250−1000 kHz, and a buck-type PCI buffer employing CeraLink capacitor technology, are presented. The LB 1.0 was presented at the GLBC finals and, with a power density of 8.18 kW/dm^3 (134 W/in^3) and a nominal efficiency of 96.4%, was ranked among the top 10 out of 100+ contestants. In Section III, the hardware prototype and results of experimental measurements on the LB 2.0, i.e. a DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter which considers all findings and lessons learned from the GLBC, are presented. Compared to the LB 1.0 presented at the GLBC finals, a further volume reduction of 40% is achieved while at the same time the power losses are reduced by almost 25%. Subsequently, in Section IV the main reasons for the performance improvement of the LB 2.0 over the LB 1.0 are discussed in detail. Afterwards, the solutions of other GLBC finalist are briefly described and the claimed efficiency and power density is compared to the experimentally verified $\eta\rho$-performance of the inverter concept selected by the authors. Finally, Section V concludes this paper and summarized important findings which are providing key guidelines for the future power density improvements of industrial ultra-compact converter systems.

II. Little Box 1.0 Demonstrator

As mentioned in the introduction of this paper, a 2-level H-bridge topology was selected because ideally no low-fre-quency (LF) Common Mode (CM) voltage is generated at the output and thus the specified ground current limit can be met without the need for bulky CM chokes. As depicted in Fig. 3, each of the two output phases is implemented by means of two interleaved 2-level totem-pole bridge-legs and, to further reduce the size of the EMI filter, a DC-link referenced bridge-leg filter

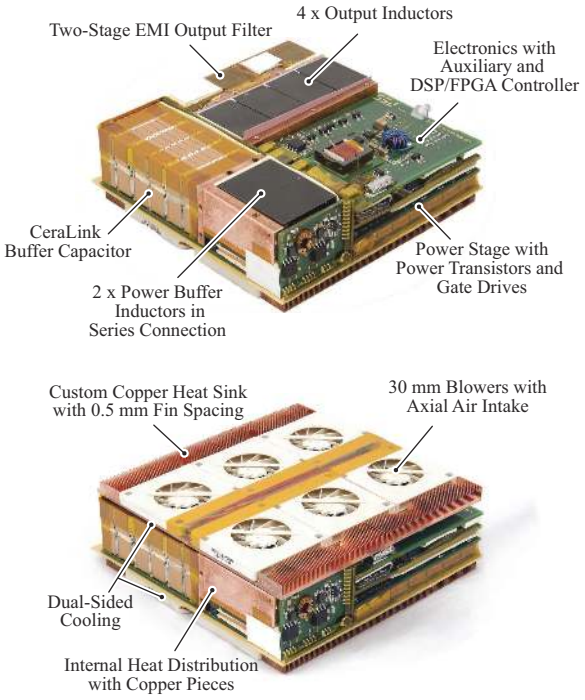

Fig. 4. Photograph of the realized LB 1.0 hardware (without housing) presented by the authors (ETH Zurich, PES), FH-IZM, and Fraza company, at the finals of the Google Little Box Challenge (8.8 cm × 8.9 cm × 3 cm, 3.46 in × 3.5 in × 1.18 in).

configuration is employed which facilitates a combined DM and CM filtering in a single stage. Furthermore, a buck-type PCI power buffer is employed to compensate the fluctuating AC power and mitigate the DC-side voltage and current ripple to meet the specified requirements. In contrast to passive DC-link buffering with electrolytic capacitors, the power buffer capacitor C_b can be cycled to a significant extent (large voltage ripple) and thus a much smaller capacitance value is required which translates into a reduced volume of the energy storage even though additional semiconductors, an additional filter inductor L_b, and auxiliary circuits are needed. In Fig. 4, a photograph of the built LB 1.0 hardware prototype with a nominal efficiency of 96.4% and an overall volume of 240 cm^3

resulting in a power density of 8.18 kW/dm^3 (134 W/in^3) is shown. In the following, details of the implementation will be described along with the presentation of experimental results.

A. Bridge-Leg Implementation

For the implementation of the bridge-legs of the system, 600 V/70 mΩ normally-off Gallium Nitride (GaN) Gate Injection Transistors (CoolGaN, Samples from Infineon, [14]) are used in combination with a novel high-performance gate drive circuit [3], [15]. In order to reduce reverse conduction losses of the GaN transistors during the dead times, 600 V SiC Schottky diodes from Wolfspeed are mounted in parallel to the power transistors. Each of the bridge-legs is operated with a TCM modulation scheme that enables zero voltage switching (ZVS) transitions in all operating points throughout an AC period [4], [5]. Since ZVS results in lower switching losses, the selected high (variable) switching frequency in the range of 200 kHz–1 MHz results in a small volume of the passive components, e.g. of the power stage filter inductors L_{1A}-L_{2B}. Furthermore, the high switching frequency in combination with the interleaving of two bridge-legs per output phase decreases the current ripple in the bridge-leg filter capacitors $C_{1/2}$ and doubles the effective switching frequency. Thus a higher cut-off frequency of the output filter is possible which in turn results in a reduced overall volume.

However, a high switching frequency also demands for suitable core materials and sophisticated inductor design in order to keep the high-frequency core and winding losses to a minimum. Addressing these challenges, the four output inductors of the inverter are realized based on a novel type of multiple-gap multiple parallel foil winding inductor [16]– [19]. Since the multiple small air gaps are evenly distributed over the full length of the inner core limb, the H-field in the winding window shows a quasi 1D distribution running in parallel to the inner limb. Consequently, a foil winding enabling a high filling factor can be used, since the H-field is aligned with the foil winding and thus ideally no eddy currents are induced. In order to counteract the skin effect at these high frequencies, the foil winding is realized with four parallel 20 µm thin copper foils which are mutually isolated with a 7 µm thin layer of Kapton. Furthermore, a sophisticated winding arrangement is used, which forces the current to flow evenly distributed in all four parallel copper layers, thus counteracting the proximity effect [16], [17]. The four output inductors of the inverter are realized based on this approach, where DMR51 MnZn Ferrite form DMEGC is used as high frequency core material. The inner limb of each output inductor has 24 air gaps surrounded by the four parallel copper foils with totally 16 turns, which gives an inductance value of around 10 µH. The inductor L_b = 20 µH of the power pulsation buffer was realized by connecting two 10 µH multi-gap inductors in series. Unfortunately, as analyzed in detail in [20] and discussed in Part A of this publication, the mechanical manufacturing and assembly of the thin ferrite plates resulted in excessive core losses in the inner limb which resulted in a relatively low quality factor of the implemented multi-gap inductors.

The capacitor of the PCI power buffer, C_b, with an effective large-signal equivalent capacitance of 150 µF, was realized by means of 108 individual 2 µF/500 V CeraLink capacitors. By the courtesy of EPCOS/TDK, a custom package with 18 capacitor chips mounted together on silver coated copper lead frames was available which drastically simplified the construction of the buffer capacitor.

B. Digital Control

For the generation of the AC output voltage v_{ac}, the two phase voltages are actively controlled to values symmetric around half of the DC-link voltage, i.e. $v_{C_1} = 1/2(v_{ac} + v_{dc})$ and $v_{C_2} = 1/2(-v_{ac} + v_{dc})$ (cf. Fig. 3). Since the sum of these phase voltages is constant, no LF CM output voltage is generated and hence LF ground currents are suppressed. The overall structure of the employed control system is shown in Fig. 5 and is composed of two subsystems dedicated to control the active power buffer and the inverter, respectively. To achieve a low THD and good transient performance, a cascaded voltage and current control feedback loop with Proportional-Resonant (PR) compensators [21] tuned at 60 Hz is used to regulate the AC output voltage. This control loop uses the AC quantities measured in the first EMI filter stage which is represented in a simplified manner by components L_3 and C_3 as shown in Fig. 5. Based on the output of the AC voltage control loop,

$$v^*_{C_{1-2}} = \bar{v}_{L_3} + v_{ac}, \tag{1}$$

wherein $\bar{v}_{L_3}$ is the local average of the inductor voltage v_{L_3}, the reference value for the capacitor voltage of the two bridge-legs,

$$v^*_{C_1} = 1/2(v^*_{C_{1-2}} + v_{dc}), \tag{2}$$

$$v^*_{C_2} = 1/2(-v^*_{C_{1-2}} + v_{dc}), \tag{3}$$

is derived. As can be seen, PI-compensators are used to control the voltages at C_1 and C_2. The reference current for L_1 and L_2 is then obtained by adding or subtracting the feed-forward term i_{L_3} to the output of the PI-compensators, respectively. Based on the measurements of the DC-link voltage v_{dc} and the bridge-leg output voltages v_{C_1} and v_{C_2}, circuit parameters such as the inductance value and the transistor output capacitances (C_{oss}), a predictive current control algorithm calculates the turn-on, turn-off and dead time interval of each bridge-leg such that the resulting inductor current features the characteristic triangular shape to achieve ZVS at both turn-on and turn-off of the bridge-leg while ensuring the correct average value $i^*_{L_{1/2}}$. To achieve a complete resonant transition at every switching instant throughout the AC period for a defined maximum dead time interval and limits imposed by the range of the variable switching frequency, a minimum constant reverse current of 5.0 A is used. The information of the inductor current Zero-Crossing (ZC) is used to update the remaining turn-on and turn-off interval to cope with measurement and parameter inaccuracies. To implement the digital control structure

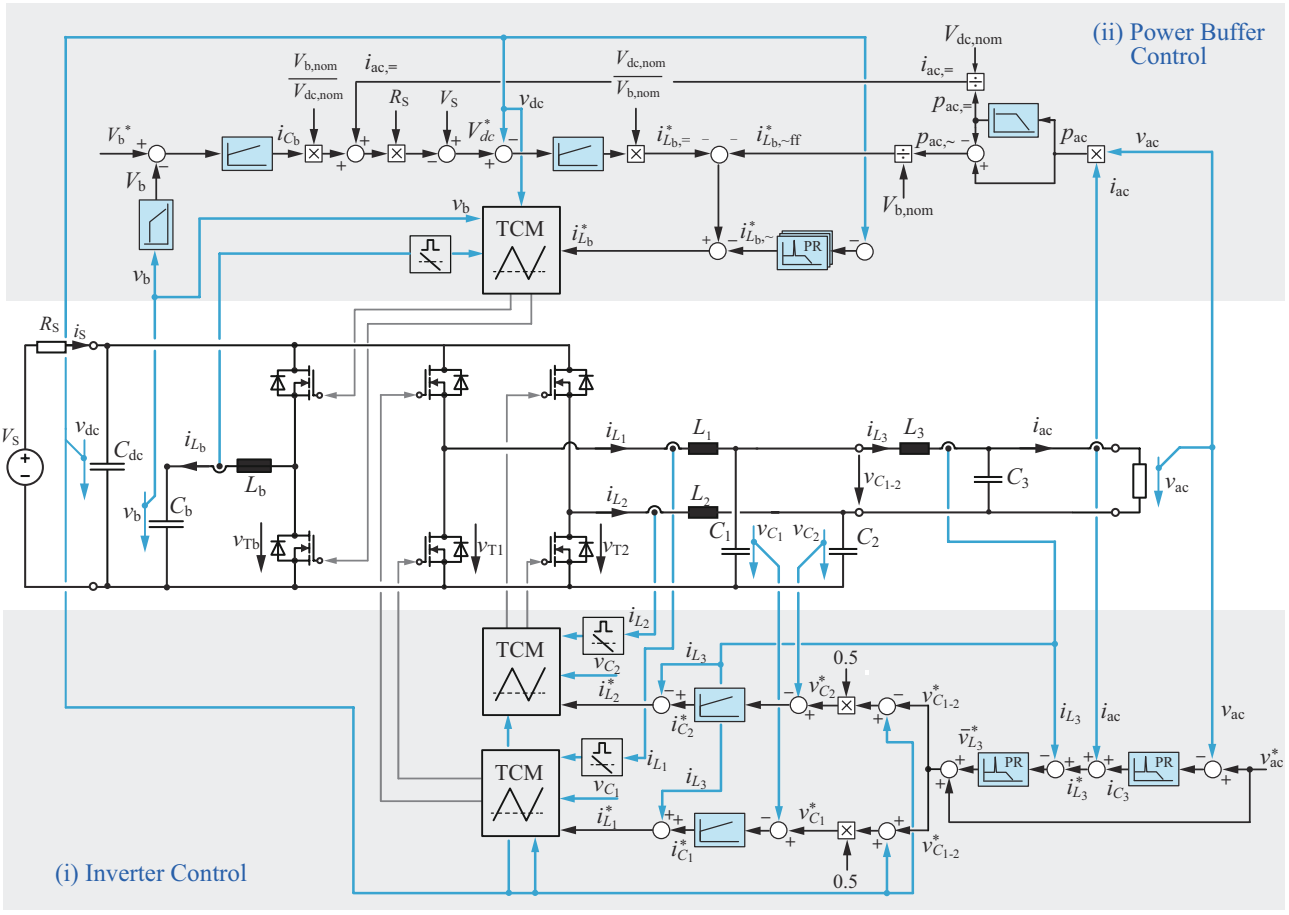

Fig. 5. Implemented digital control system of the Little Box 1.0 (LB 1.0). The inverter control structure is located below and the power buffer control structure is located above the power circuit diagram of the converter. For the sake of simplicity, the interleaved bridge-legs and the EMI filter are not included in the circuit diagram. The AC output voltage is controlled in the first DM filter stage which is represented by the components L_3 and C_3.

in hardware, a combination of a TI C2000 Delfino real-time microcontroller (TMS320F28335ZJZS) and a Lattice FPGA (LFXP2-5E-5MN132I) is used. The analog signal measurements, the feedback control system as depicted in Fig. 5, and the computation of the TCM timing intervals are implemented on the microcontroller and are executed with the fastest possible rate of 20 kHz. The timing intervals from the microcontroller and the current ZC signals are forwarded to the FPGA where the TCM modulator with a resolution of 5 ns (200 MHz) is implemented. Thus, for the given switching frequency range of 200 kHz–1 MHz, the TCM timing variables from the microcontroller are updated only every ≈ 10–50 switching cycles which justifies the twice per cycle occurring ZC feedback and adjustment of timing intervals. The TCM modulator also features the synchronization capability for the correct interleaving of the two bridge-legs for each output phase (cf. Fig. 3) in order to ensure the desired cancellation of the first harmonic in the current. The commands to activate and deactivate the individual bridge-legs depending on the position within the AC period and actual output power level (4D-interleaving, as described in Section III-C3 of Part A) are determined on the microcontroller and are then forwarded to the FPGA.

The selected magnetic saturation based Zero Crossing Detection (ZCD, cf. Fig. 5 of Part A, [22]) is implemented by means of a small toroidal core with an outer diameter of 4 mm (R4 × 2.4 mm × 1.6 mm, B64290P0036X830 from EPCOS). The selected core material is N30 which features a low saturation flux density and high permeability over a wide frequency range. The number of turns of the secondary (measurement) winding is set to $N_s = 10$. Depending on the inductor current slope (di_L/dt), with this number of turns the induced voltage reaches values from 20 V up to 160 V, which makes the ZCD circuit robust against electric disturbances. However, with the variability of the induced voltage also the time delay of the detection of the current crossings slightly changes. The induced voltage is tracked with a fast comparator circuit (TLV3501, 4.5 ns propagation delay) in order to keep the signal delay short and is then digitally filtered in the FPGA.

The control system of the buck-type PCI power buffer is also depicted in Fig. 5. The main objective of the power buffer control system is to exactly compensate the pulsating power caused by the single-phase AC load, such that only a constant power $P_S = V_S \cdot i_S$ is drawn from the DC source. First, $p_{ac,\sim}$ is calculated by means of subtracting the average power $\overline{p_{ac}} = p_{ac,=}$, from the instantaneous load power $p_{ac} = v_{ac} \cdot i_{ac}$, as shown in

the upper right corner of Fig. 5, with measured output voltage v_{ac} and current i_{ac} of the inverter. Dividing power $p_{ac,\sim}$ by the nominal average buffer capacitor voltage $V_{b,nom}$ yields the compensation current reference $i^*_{L_b,\sim ff}$ which is used as a feed-forward term. Besides neglecting the instantaneous power in L_b and the inverter's EMI filter, inaccuracies and delays in the signal acquisition and computation of the controller, the fluctuating AC power cannot be perfectly compensated by means of the feed-forward control. Therefore, in order to eliminate any possible remaining voltage ripple at the DC link, additional resonant compensators [21],

$$C_{R,m}(s) = \frac{2K_{i,m}s}{s^2 + (m\cdot\omega)^2}, \tag{4}$$

are employed, wherein parameter $m \in 2, 4, 6$ sets the resonant frequency of the compensator to the first three even multiples of the mains frequency. As long as there is a spectral component with frequency $m \cdot \omega$ in the error signal $e_m = 0 - v_{dc}$ seen by the respective resonant compensator, the amplitude of the sinusoidal controller output will increase, requesting more current of that particular frequency to be injected into the DC link.

The cascaded control loop depicted in the upper left corner in Fig. 5 is employed to keep the mean value of the buffer capacitor voltage $\overline{v}_b = V_b$ at a chosen reference. If only control aspects are considered, then the reference voltage of the buffer capacitor V^*_b would be set to a voltage level

$$V_{b,mid} = V_{dc,nom}/\sqrt{2} = 282.8\ \text{V} \tag{5}$$

corresponding to half of the maximal stored energy. Maintaining the bias of the buffer capacitor at $V_{b,mid}$ results in symmetrical energy margins, and a load step-up or step-down can be handled equally well. However, since (i) the prevailing capacitance density of the considered ceramic capacitors is strongly dependent on the DC bias and (ii) the amplitude of current i_b is inversely proportional to v_b, a compromise between transient handling capability and $\eta\rho$-performance must be made. Therefore, in case of the realized PCI buffer of the LB 1.0 with CeraLink capacitors, the reference voltage V^*_b is set to 300 V.

As a result of the current injected at the DC-link to compensate the fluctuation portion of the AC power, the buffer capacitor voltage features a distinctive voltage ripple at twice the mains frequency. In order to extract the mean buffer voltage V_b, a low-pass filter, specifically a moving-average filter with window size of one 120 Hz period, is employed. A PI-compensator is used to compute the current i_{C_b} needed to charge or discharge the buffer capacitor to meet the reference value. The inner loop of the cascaded PCI buffer control structure depicted in Fig. 5 is required to tightly regulate the average DC-link voltage under all load conditions. It should be noted that this control loop also contributes to the cancellation of any remaining low frequency voltage ripple at the DC-link. However, the resonant compensators can be tuned more aggressively and are thus more effective in eliminating the LF voltage ripple.

The input current reference of the converter is given by

$$i^*_S = i_{C_b}\frac{V_{b,nom}}{V_{dc,nom}} + \frac{p_{ac,=}}{V_{dc,nom}}, \tag{6}$$

which includes the current needed to adjust the buffer capacitor bias and the current needed to provide the real power $P_S = p_{ac,=}$ to the load. The current i_{C_b} computed by the outer PI-controller, is referred to the DC link voltage level by means of the static scaling factor $\frac{V_{b,nom}}{V_{dc,nom}}$. Since it is assumed that with ideal control there is no 120 Hz ripple present in the DC-link voltage, low-pass filtering of v_{dc} is not necessary which increases the phase-margin of the inner loop of the cascade. Given the converter input current, the DC-link voltage reference is calculated with the equation

$$V^*_{dc} = V_S - R_S \cdot i^*_S \tag{7}$$

$$= V_S - R_S \cdot \left(i_{C_b} \cdot \frac{V_{b,nom}}{V_{dc,nom}} + \frac{p_{ac,=}}{V_{dc,nom}} \right). \tag{8}$$

It should be noted that instead of computing V^*_{dc} under the assumption of a constant input resistance $R_S = 10\ \Omega$, an additional PI-compensator can be used to regulate the converter input current. The output of the PI-compensator is the required voltage across the input resistor R_s and is subtracted from the fixed source voltage $V_S = 450$ V to obtain the operating point dependent DC-link voltage reference V^*_{dc}.

The inner-loop PI-compensator then controls v_{dc} to meet the reference V^*_{dc}. Referring the output of the PI-compensator to the buffer capacitor voltage level by means of scaling with $V_{dc,nom}/V_{b,nom}$ yields the mean buffer current reference $i^*_{L_b,=}$, required to keep both V_b and v_{dc} at the desired average values. Due to the cascaded structure, controlling the DC-link voltage has always priority over the mean buffer capacitor voltage. This has significant advantages in case of abrupt load changes, since the average buffer capacitor voltage V_b can be temporarily deflected from the reference V^*_b, keeping v_{dc} tightly controlled. Assuming a strict unidirectional power flow from the DC supply (no current sinking capability), then, e.g. in case of an stepwise load drop from 1 kW to 0 kW, the energy stored in the converter system at the very moment of the load change, namely the energy stored in the passive components of the inverter stage and the PCI buffer inductor, is absorbed in the larger buffer capacitor and not in the at least a factor of 10 smaller DC-link capacitance. This prevents critical overshoots or sags in v_{DC}, even under harsh load transients. Eventually, the individual current references $i^*_{L_b,=}$, $i^*_{L_b,\sim ff}$ and $i_{L_b,\sim *}$ are combined to obtain a single reference i^*_{LB} of the PCI filter inductor current. Note the negative gain because of the imposed counting direction of i_{L_b}.

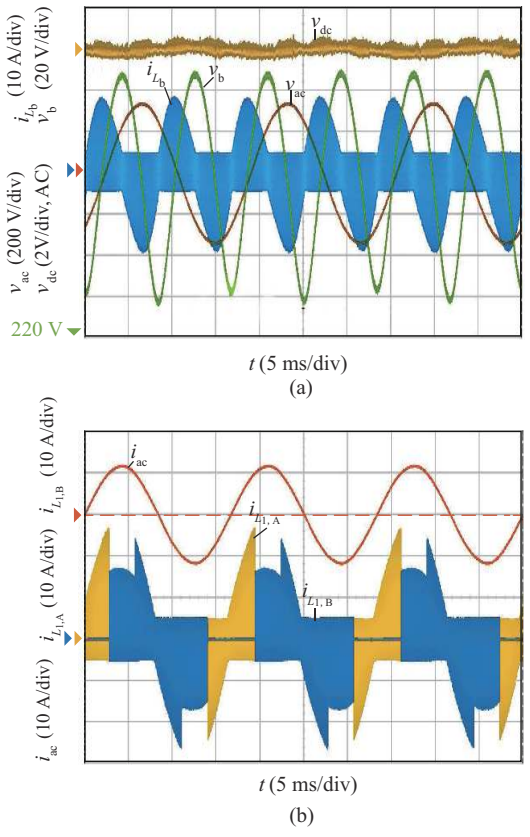

Fig. 6. Measured steady-state waveforms of the Little Box 1.0 (LB 1.0) prototype operated at the rated 2 kW output power. (a) The active power buffer eliminates the 120 Hz voltage ripple of the DC-link voltage v_{dc}. The buffer voltage swing at rated power is designed to be around 110 V. (b) Filtered output current and corresponding high-frequency Triangular Current Mode (TCM) modulated current $i_{L1,A}$ and $i_{L1,B}$ in the power stage inductors $L_{1,A}$, $L_{1,B}$ with 4D-interleaving (cf. Section III-C3 of Part A). The measurements were performed at unity power factor (cos φ_0 =1) but the waveforms depicted in (a) and (b) were not captured simultaneously which explains the phase-shift between v_{ac} and i_{ac}.

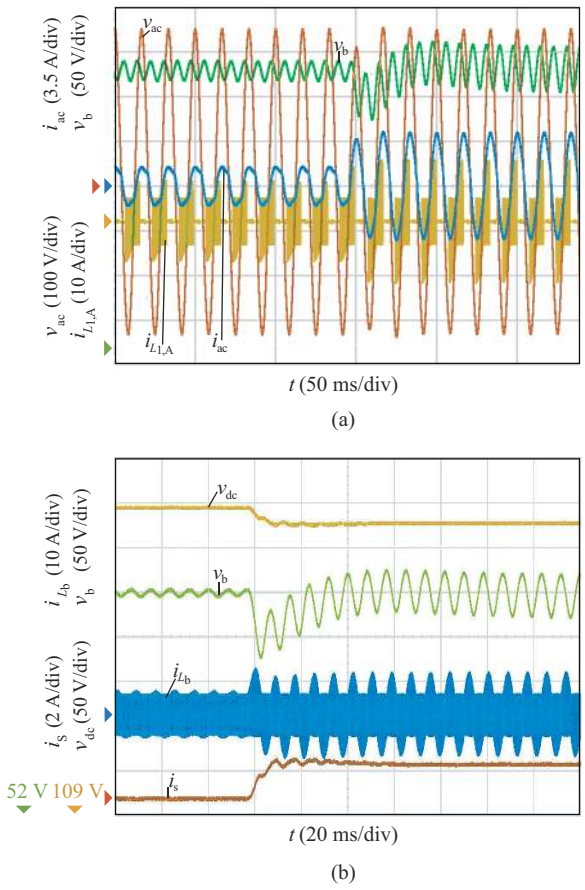

Fig. 7. Transient waveforms of the Little Box 1.0 (LB 1.0) subject to a stepwise increase in output power. (a) Measured AC output waveforms v_{ac} and i_{ac}, and filter inductor current $i_{L1,A}$ subject to a stepwise load increase from 230 W to 700 W. (b) Measured DC-side and power buffer waveforms subject to a stepwise load increase from 0 W to 700 W. The small ripple present in the buffer capacitor voltage prior to the load step despite 0 W of output power is due to the reactive power drawn by the EMI filter (DM capacitors). Note that the waveforms depicted in (a) and (b) were not captured simultaneously and exhibit a different time scale.

Likewise to the inverter, a predictive current control algorithm computes the correct timing intervals and a dedicated TCM modulator computes the high resolution bridge-leg control signals.

C. Experimental Waveforms

Fig. 6 shows the measured characteristic waveforms of the LB 1.0 prototype at steady-state and rated output power. Considering v_{dc} (yellow trace) in Fig. 6(a), it can be seen that the PCI power buffer effectively compensates the fluctuating AC power and successfully mitigates the 120 Hz voltage ripple. The resulting voltage swing present in the buffer capacitor voltage v_b, amounts to 110 V and is superimposed to the bias or offset voltage V_b = 300 V. The characteristic TCM shape of the PCI buffer inductor current is also shown in Fig. 6(a). Fig. 6(b) displays the sinusoidal AC output current and the current in the inductor $L_{1,A}$ and $L_{1,B}$ of the two interleaved bridge-legs of output phase 1. Clearly visible is the outcome of the implemented 4D-interleaving, where both bridge-legs are only operated simultaneously at high instantaneous output power, i.e. around the peak value of i_{ac} in case of ohmic loads. The total overlap duration of the interleaved bridge-legs as shown in Fig. 6(b) amounts to 158°. The actual overlap duration in every operating point was determined empirically with the objective to increase the overall conversion efficiency while complying with the specified EMI regulations. Fig. 7 shows the measured waveforms of the LB 1.0 converter during a transient caused by a stepwise increase in output power. Fig. 7(a) shows the AC output waveforms during a load step from 230 W to 700 W. It can be seen that the transient is settled in less than 50 ms which clearly complies with the specified settling time of 1 s for a maximum specified load step of 500 W. Fig. 7(b) shows the PCI buffer and DC-side related waveforms for a load step from 0 W to 700 W. Triggered by the step, the average buffer capacitor voltage drops 50 V below the 300 V at steady-state. Simultaneously, the PCI buffer controller starts to compensate the power pulsation by means of injecting an appropriate

current into the DC-link. As a consequence, a distinct 120 Hz voltage ripple develops at the buffer capacitor immediately after the load step. After a transient time of 60 ms, the average buffer capacitor voltage has recovered and the fluctuating AC power is completely compensated by the active power buffer. Take note that the PCI is achieving a smooth transition of the DC-link voltage level which settles at a lower value after the transient due to the inserted 10 Ω resistor R_s between the 450 V DC source and the DC-link (cf. Fig. 3). The reactive power drawn by the EMI filter (DM capacitors) of the inverter stage is compensated by the power buffer, thus a small ripple is present in the buffer capacitor voltage prior to the load step although no load is connected to the inverter.

D. EMI Compliance

In order to achieve a high filter attenuation while still keeping the filter components small, for the given circuit structure and selected frequency range a two-stage EMI output filter topology is employed as shown in Fig. 3. As can be noticed, although with the H-bridge topology ideally no LF CM voltage is generated at the inverter output, the CM inductors L_{CM1} and L_{CM2} as well as the CM capacitors C_{CM1} and C_{CM2} are still needed to filter the remaining HF CM components. Note, that the bridge-legs of output phases 1 and 2 cannot be synchronized because of the TCM control and thus the CM noise elimination known from the H-bridge topology with bipolar PWM does not apply. In the given filter configuration, the output capacitors C_1 and C_2 not only help to attenuate the Differential Mode (DM) noise but also the CM noise, which means that if C_1 and C_2 are increased, the needed CM inductance can be decreased. Furthermore, since $C_{1/2}$ are either connected to the positive or negative DC-rail and thus no ground currents are generated, $C_{1/2}$ can be designed in the µF-range which is much larger than the CM capacitor values of C_{CM1} and C_{CM2} which are more in the tens of nF-range. The only limiting factor for the capacitance of C_1, and also for the other DM capacitors C_{DM1} and C_{DM2}, is the additional reactive power demand that causes larger currents and higher losses in the whole system. For the built prototype each C_1 is realized with four parallel and C_{DM1} and C_{DM2} with three parallel 2.2 µF, 450 V class II/X6S Multi-Layer Ceramic Capacitors (MLCC, C5750X6S2W225M250KA from EPCOS/TDK), since ceramic capacitors feature a much higher capacitance per unit volume than the conventionally used film capacitors. On the contrary, the dielectric material of the class II/X6S MLCCs exhibits substantial power loss when excited with a large-voltage swing at low frequencies (cf. Section II-B1 and Appendix C of Part A). Based on experimental measurements, the dissipated power per volume of the class II/X6S dielectric material is in the order of 4.7 W/cm^3 for an AC excitation with $2 \times \sqrt{2} \times 240$ V = 678.8 V peak-to-peak voltage at 60 Hz

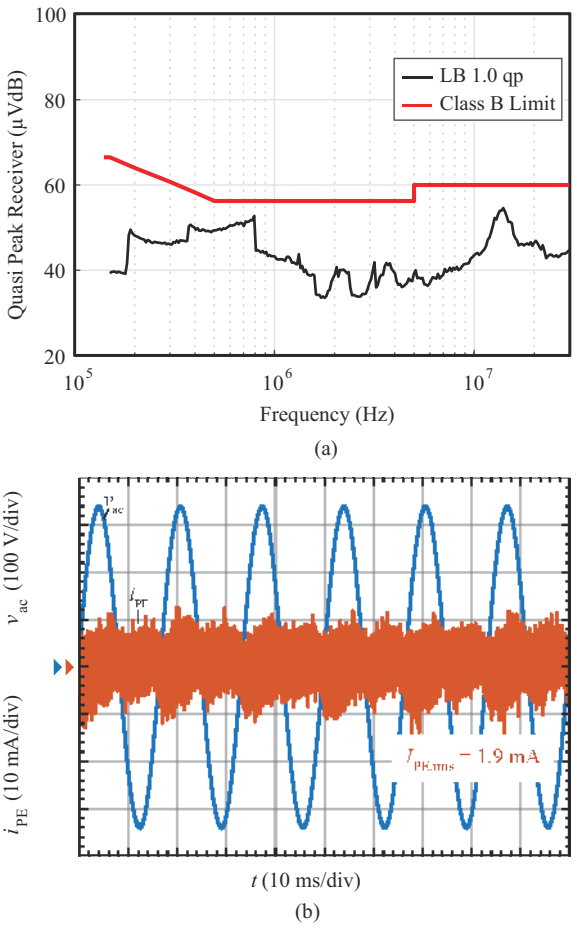

Fig. 8. (a) EMI noise spectrum of Little Box 1.0 (LB 1.0) at 2 kW output power measured with R&S ENV216 single-phase LISN and R&S ESPI7 test receiver. (b) Ground current of the LB 1.0 measured by means of inserting both AC output wires simultaneously into the clamp of a current probe (Teledyne CP030).

excitation frequency. Considering the voltage-and temperature-dependent capacitance of the selected components, the effective capacitance drops to approximately 650 nF per piece which results in an additional reactive output filter power of around 200 VAr. The CM inductors L_{CM1} and L_{CM2} are built with toroidal cores from Vacuumschmelze which are based on the core material VITROPERM 500F that offers a high permeability and high saturation flux density (core type: T60006-L2012-W498, winding: 11 turns, 1 mm-Ø). Even if the leakage inductance of the CM inductors contributes to the DM inductances, separate DM inductors, L_{DM1} and L_{DM2} are added to achieve the required DM attenuation. For all DM inductors the commercially available 10 µH-inductors from Coilcraft (XAL1010-103MED) are used. The CM capacitors C_{CM0}, C_{CM1} and C_{CM2} are implemented with 3 × 100 nF, 630 V/ X7R MLCCs from TDK (C3225X7T2J104K160AC).

The quasi-peak EMI spectrum of the LB 1.0 hardware prototype with aluminium enclosure at 2 kW output power is depicted in Fig. 8(a). The results where obtained with the R&S ESPI7 test receiver and the R&S ENV216 single-phase

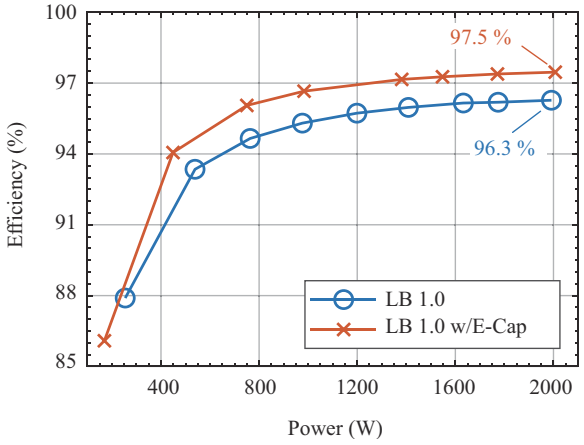

Fig. 9. Conversion efficiency of the Little Box 1.0 (LB 1.0) with respect to output power measured with a Yokogawa WT3000 precision power analyzer. The red curve with cross markers represents the measured efficiency of the inverter using passive DC-link buffering with electrolytic capacitors instead of the active power buffer.

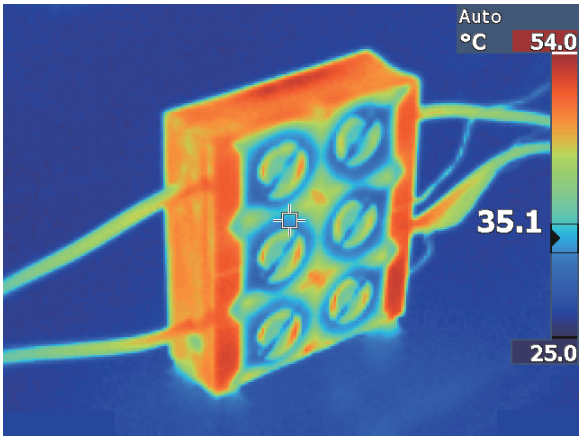

Fig. 10. Thermography image of the Little Box 1.0 (with housing) recorded with a FLUKE Ti10 infrared camera showing the steady-state temperature distribution at rated 2 kW output power.

LISN which was installed between the AC output of the converter and the resistive load bank. It can be clearly seen that the FCC Part 15 B conducted EMI limits are met. Due to the implemented TCM control with resulting variable switching frequency, the noise spectrum does not exhibit distinct peaks but instead is spread out over a wide frequency range.

In a preceding calibration test, the DC output terminals of the employed laboratory voltage source were connected directly to the resistive load bank. In a characteristic operating point, that is 450 V DC and 5A, around 7.4 mA of ground current was measured by means of inserting both wires in the clamp of a Teledyne CP030 current probe. If the chassis of the supply was, in addition to the always persistent ground connection through the AC supply cable, also connected directly to the local ground/PE terminals of the EMI test setup, approximately 30 mA of ground current were detected. For this reason, a CM choke of ≈ 2 mH @ 10 kHz of nominal inductance, implemented with 5 turns around a toroidal VITROPERM 500F core (T60006-L2045-V102), was inserted between the DC supply (Sorensen SGI 600/17) and the converter input. Keep note that because of the low-impedance path provided by the CM capacitor C_{CM0} at the input of the converter (cf. Fig. 3), a fair assessment of the ground current caused by the device under test is still possible.

The recorded ground current in the nominal operating point is depicted in Fig. 8(b) and was measured by inserting both AC output wires simultaneously into the clamp of the current probe(Teledyne CP030). The ground wire of the converter was connected to the local ground/PE terminal of the EMI test setup. The RMS value of the ground current amounts to only 1.9 mA and confirms the effectiveness of the designed CM filter and the symmetrical H-bridge inverter topology. It should be emphasized, that the LB 1.0 converter therefore complies to the original more stringent 5 mA ground current limit of the GLBC which was later relaxed to 50 mA (cf. Section II of Part A).

E. Efficiency

The measured efficiency of the LB 1.0 prototype as a function of output power is depicted in Fig. 9. As indicated by the blue line with circle markers, the efficiency of the system with active power buffer exhibits a peak efficiency of 96.3% at rated output power. The corresponding CEC weighted efficiency amounts to 95.07%, meeting the minimum efficiency requirements (95%) of the GLBC. The red line with cross markers represents the measured efficiency of only the inverter with passive DC-link buffering by means of high-density electrolytic capacitors(3 × 493 µF/450 V, B43991-X0009-A223 from EPCOS/TDK). The peak efficiency amounts to 97.5% and the resulting CEC efficiency amounts to 96.3%. The substantial reduction in efficiency by the operation of the PCI can be ascribed to the additional HF bridge-leg with multi-gap filter inductor and CeraLink buffer capacitor. In fact, as will be further discussed in Section IV, roughly 60% of the PCI power losses are caused by the CeraLink buffer capacitor.

F. Cooling and Operating Temperature

A dual-sided cooling arrangement(cf. Fig. 4) with ultra-flat custom-machined heat sink elements is used to extract the 74 W of power loss in the nominal operating point. The heat sink has a height of only 4.5 mm and employs 6 Sunon 5V DC micro blowers (30 × 30 × 3 mm) per element. The effective cooling system performance index (CSPI) amounts to 25 W/(K dm^3) and also considers the heat distribution elements (thin copper pieces within the converter) needed to conduct the heat from the lossy components, e.g. the power inductors, to the baseplate of the respective heat sink. The thermography image in Fig. 10, recorded with a FLUKE Ti10 infrared camera, shows the steady-state temperature distribution of the LB 1.0 at 2 kW output power. As it can be clearly seen, the implemented cooling system is sufficient to meet the maximum allowed

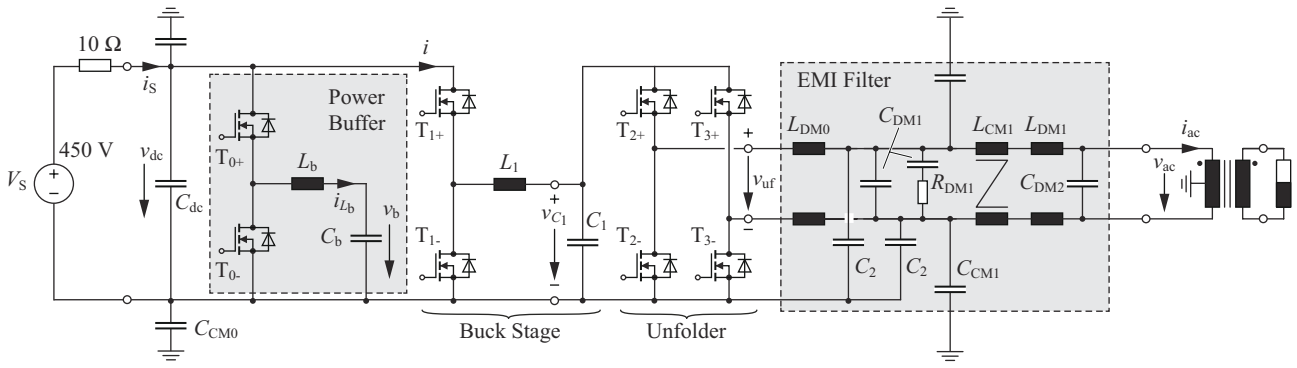

Fig. 11. Topology of the 2nd inverter realized according to the Google Little Box Challenge (GLBC) technical specifications with revised 50 mA earth current limit (Little Box 2.0, LB 2.0). The inverter is comprised of a DC/|AC| buck-stage with |AC|/AC H-bridge unfolder and a subsequent EMI output filter. The DC-side energy storage to compensate the fluctuating AC power is also implemented with a buck-type Parallel Current Injector (PCI) active power buffer.

surface temperature requirement of 60 °C.

III. Little Box 2.0 Demonstrator

The inverter topology of the Little Box 2.0 (LB 2.0) as shown in Fig. 11 is based on a conventional DC/|AC| buck converter which generates a rectified sinusoidal voltage $v_{C1} = |\hat{V}_{ac} \cdot \sin(\omega t)|$ with respect to the negative DC-link rail and a subsequent |AC|/AC H-bridge unfolder which generates the actually desired sinusoidal output voltage v_{uf} [23]. Likewise to the LB 1.0 system, the DC-side energy storage to compensate the fluctuating AC power is realized with a buck-type PCI power buffer. Compared to the H-bridge topology of the LB 1.0(cf. Fig. 3), the major advantage of this topology is that one half of the previously described inverter stage including bridge-leg filter inductors and capacitors can be completely omitted, thus volume and losses are saved and the system complexity is reduced. However, a higher ground current is to be expected since a LF CM voltage with a peak voltage equal to half the AC amplitude, i.e. $v_{CM} = \hat{V}_{ac}/2 \cdot \sin(\omega t)$, is generated at the output(cf. Fig. 10(b) of Part A). The H-bridge unfolder was selected because, unlike the half-bridge unfolder(totem-pole inverter) [1], high dv/dt transitions in the LF CM voltage are prevented and it is furthermore possible to utilize the DC-link referenced filter configuration and therefore reduce the size of the EMI filter. In this regard, the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder concept became truly viable once the specified ground current limit was relaxed from 5 mA to 50 mA because of the expected volume reduction of the CM chokes due to the comparably high permissible total CM capacitance of $\approx \frac{50\text{ mA}}{2\pi 60\text{ Hz} \cdot 1/2 \cdot 240\text{ V}} = 1.1\ \mu\text{F}$.

In Fig. 12, a picture of the built LB 2.0 hardware prototype with an overall boxed volume of 135 cm^3 (without housing) resulting in a remarkable power density of 14.8 kW/dm^3 (243 W/in^3) and a nominal efficiency of 97.4% is shown. In the following, details of the implementation will be described along with the presentation of experimental results.

A. Bridge-Leg Implementation

For the implementation of the PCI and inverter buck-stage

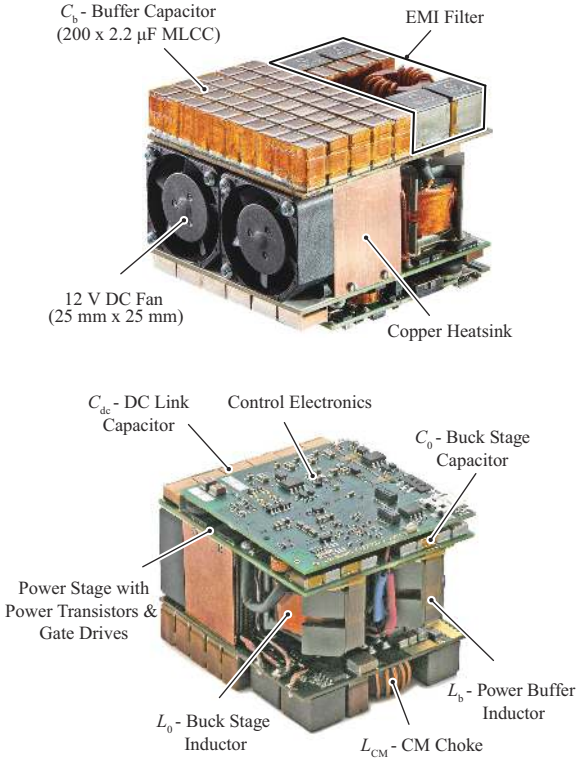

Fig. 12. Photograph of the realized Little Box 2.0 (LB 2.0) hardware (without housing) (5.9 cm × 5.0 cm × 4.5 cm, 2.32 in × 1.97 in × 1.77 in).

bridge-legs, also 600 V/70 mΩ CoolGaN technology is used with two transistors in parallel per switch. In order to reduce losses during reverse conduction of the GaN transistors, 600 V SiC Schottky diodes are used. The inductor of the buck-stage converter, L_1 = 45 µH is implemented on a RM 10 core using the MnZn ferrite material N97 from TDK. The winding is realized with 30 turns of a 180 × 71 µm HF litz wire without additional silk insulation to achieve a higher copper filling factor. The limbs of the RM 10 core were shortened with a diamond wheel precision saw to achieve a total air gap length of 6 mm (3 mm per limb) while keeping the total height of the core unchanged. The inductor of the PCI, L_b = 40 µH, is also implemented on a N97/RM 10 core. The winding is

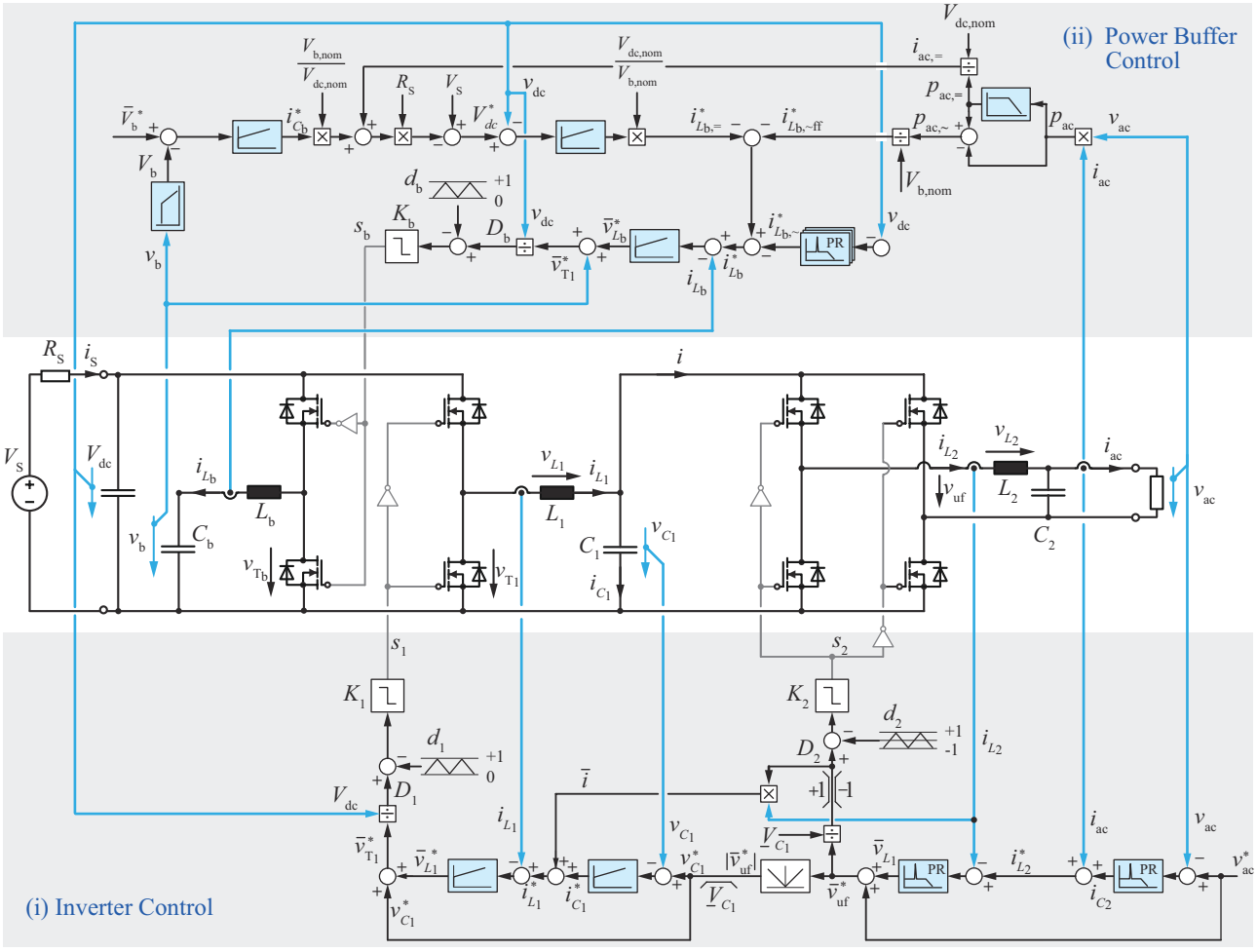

Fig. 13. Implemented digital control system of the Little Box 2.0 (LB 2.0). The inverter control structure is located below and the power buffer control structure is located above the power circuit diagram of the converter. For the sake of simplicity, the complete EMI filter is not included in the circuit diagram. The AC output voltage is controlled in the DM filter at the unfolder output, which is represented by components L_2 and C_2.

realized with 20 turns of a 225 × 71 µm HF litz wire also without additional silk insulation. The limbs of the RM 10 core were also shortened to achieve a total air gap length of 2 mm (1 mm per limb) while keeping the total height of the core unchanged. To minimize the conduction losses of the H-bridge unfolder, 650 V/25 mΩ enhancement-mode GaN transistors from GaNSystems (GS66516T) are employed as they feature best-in-class on-state resistance. Because the hardware design does not allow for a direct heat sink connection, two 25 mΩ transistors are connected in parallel per switch to further reduce the conduction losses and virtually render cooling unnecessary. The PCI and inverter buck-stage are operated with an EMI friendly constant 140 kHz switching frequency. The unfolder H-bridge is operated with 120 Hz except, as described in more detail in the next section, during temporary 140 kHz unipolar PWM operation around the ZCs of the AC voltage (cf. Fig. 11 of Part A).

The capacitor of the PCI C_b, with an effective large-signal equivalent capacitance of ≈ 120 µF, was realized by means of 200 individual 2.2 µF, 450 V class II/X6S MLCCs. As can be seen in Fig. 12, 200 of these chip capacitors were soldered together on a PCB which is on the one hand a very challenging assembly task and on the other hand bears the risk of electrical failures due to micro-cracks in the ceramic material caused by mechanical stress during assembly and/or operation.

B. Digital Control

The deployed control system of the LB 2.0 prototype is depicted in Fig. 13. The structure of the implemented PCI control system is identical to the LB 1.0 prototype(cf. Fig. 5) except that the current in inductor L_b is now regulated by a conventional PI-feedback loop and fixed frequency PWM instead of TCM control. Likewise to the LB 1.0 control scheme, the AC output voltage is tightly regulated with a cascade of outer-loop voltage and inner-loop current feedback control using PR-controllers as shown in the bottom right of Fig. 13. The output voltage of the buck-stage, v_{C_1}, is regulated with a PI-compensator to follow the rectified unfolder voltage reference $|v^*_{uf}|$ until it falls below the minimum defined value $\underline{V}_{C_1}$,

$$v^*_{C_1} = \max\left(\left| v^*_{uf} \right|, \underline{V}_{C_1} \right). \tag{9}$$

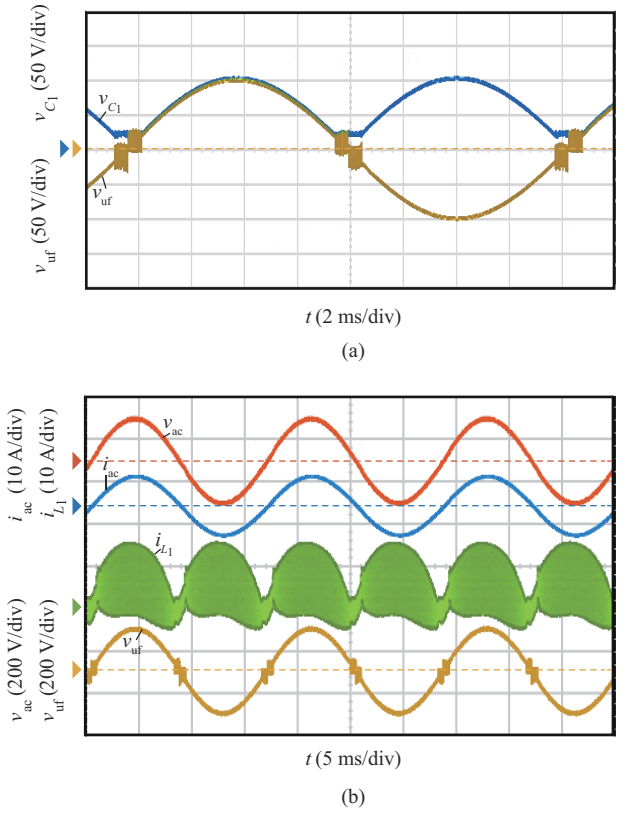

Fig. 14. Experimental measurements. (a) demonstrating the temporary PWM operation of the unfolder and the corresponding constant DC/|AC| buck-stage output voltage v_{C1} which (b) prevents distortion in the AC output current during ZCs of the output voltage.

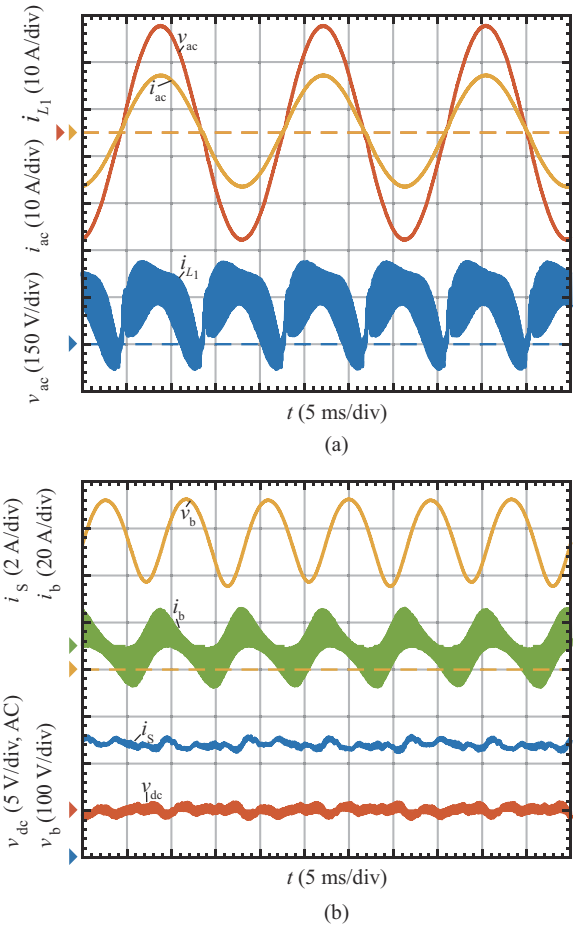

Fig. 15. Measured steady-state waveforms of the Little Box 2.0 (LB 2.0) operated at rated 2 kW output power (cos φ_0 =1). (a) shows the AC output waveforms v_{ac} and i_{ac}, and the high-frequency current in the buck-stage inductor L_1. (b) The active power buffer clearly eliminates the double-line frequency voltage ripple.

As described in Part A (cf. Fig. 11 of Part A), during the time interval when $|v^*_{uf}| < \underline{V}_{C1}$, the buck output voltage reference is kept constant at $\underline{V}_{C1}$ and the duty-cycle of the unfolder, operated with 140 kHz unipolar PWM during this interval, is adjusted such that the voltage at the output of the unfolder v_{uf} follows precisely the sinusoidal reference v^*_{uf}. Preventing v_{C1} to fall below a minimum value, prevents distortions in the output current during the ZC of the voltage, which is particularly of concern for reactive loads when the output voltage and current are not in phase, and also allows to adopt TCM modulation in the buck-stage if desired ($v_{C1} > 0$ needed at any time for $di_{L1}/dt < 0$ during turn-off interval). Since, the time interval in which the unfolder H-bridge is operated with PWM is very short compared to the AC period and because the switched voltage is also low ($= \underline{V}_{C1}$), the occurring switching losses of the unfolder H-bridge are negligible. The experimental waveforms to illustrate the described inverter control concept are shown in Fig. 14 and were recorded during commissioning of the LB 2.0 hardware. Fig. 14(a) shows how v_{C1} does not fall below the specified minimum voltage of $\underline{V}_{C1} = 25$ V and the unfolder H-bridge engages in unipolar PWM during this period. As can be seen in Fig. 14(b), this effectively prevents distortions during the ZCs of the AC output voltage typically present in PFC rectifier systems.

In order to tightly control v_{C1}, particularly at the transitions between rectified sinusoidal and constant voltage reference, a cascade of PI-controllers with outer-loop voltage and inner-loop current feedback is employed. Likewise to the PCI power buffer, conventional constant frequency PWM is employed to generate the switching signals for the DC/|AC| inverter buck-stage.

The entire digital control system of the LB 2.0 depicted in Fig. 13, is implemented on a TI C2000 Delfino real-time microcontroller (TMS320F28335ZJZS) and no additional FPGA is employed. The currents are measured with a Hall-effect current sensor from Allegro featuring 1 MHz bandwidth (ACS730).

C. Experimental Waveforms

Fig. 15 shows the measured characteristic waveforms of the LB 2.0 prototype at steady-state and rated output power. The sinusoidal output voltage and current and the HF current in the DC/|AC| buck-stage inductor L_1 are shown in Fig. 15(a).

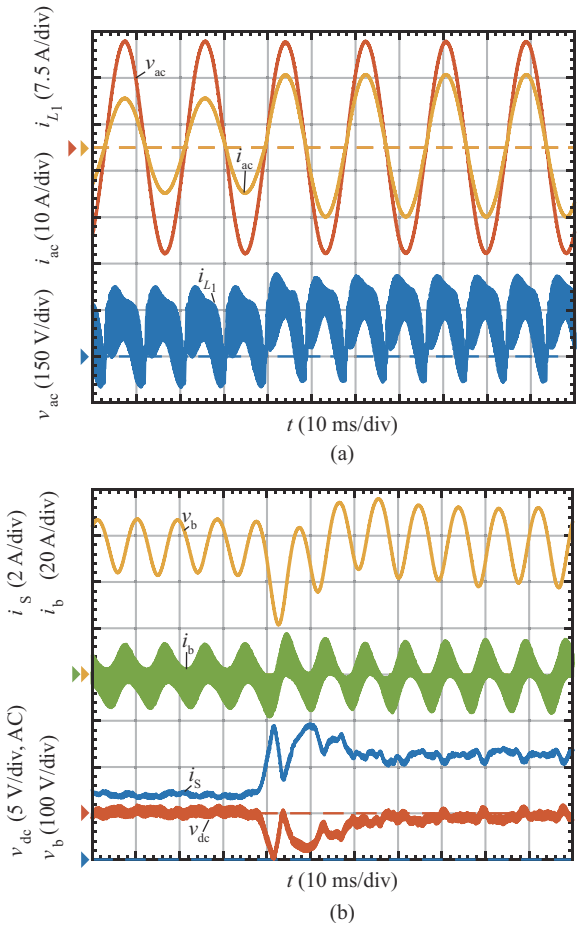

Fig. 16. Transient waveforms of the Little Box 2.0 (LB 2.0) subject to a stepwise increase in output power. (a) Measured AC output waveforms v_{ac} and i_{ac}, and filter inductor current i_{L1} and (b) measured DC-side and power buffer waveforms resulting from a stepwise load increase from 1.35 kW to 2 kW.

The waveforms of the PCI and the DC-side of the converter are depicted in Fig. 15(b). Considering v_{dc} (red trace) and converter input current i_S (blue trace), it can be seen that the PCI effectively compensates the fluctuating AC power and the specified DC-link voltage and input current ripple limits are clearly met. Note, that the measurement of v_{dc} was performed with AC coupling. The resulting peak-to-peak voltage swing present in the buffer capacitor voltage v_b amounts to 180 V and is superimposed to the bias or offset voltage V_b = 280 V. Because of the lower AC excitation losses of the class II/X6S capacitors [1], a much larger voltage swing is feasible compared to the CeraLink power buffer (cf. Section II-C, peak-to-peak voltage swing of 110 V). Fig. 16 shows the measured waveforms of the LB 2.0 converter during a transient caused by a stepwise increase in output power. Fig. 16(a) shows the AC output waveforms and Fig. 16(b) shows the corresponding PCI power buffer and DC-side related waveforms during a load step from 1.35 kW to 2 kW. The amplitude of the AC output voltage and current are settled quickly after one period which can be attributed to the high bandwidth of the underlying DC/|AC| buck-stage current control (cf. Section III-B of this paper). Triggered by the step, the average buffer capacitor voltage drops around 100 V below the 280 V at steady-state and recovers after 35 ms when the transient is settled. Naturally, the buffer capacitor voltage exhibits a larger amplitude of the 120 Hz voltage ripple once the load is increased. Note that the DC-link voltage settles at the same level after the load step because of the AC coupling of the voltage measurement. As it can be inferred from the shorter settling time and the overshoot of the input current i_S, the DC-link controller is tuned more aggressively compared to the LB 1.0 implementation (cf. Section II-C). In any case, the transient performance of the deployed control system clearly complies with the specified settling time of 1s for the maximum required step size of 500 W.

D. EMI Compliance

Because of the intermittent HF PWM operation of the unfolder, a dedicated output filter for each leg of the H-bridge is provided. Since only a low voltage, $\underline{V}_{C1}$ = 25 V, is switched with 140 kHz, a comparably small DM filter inductor L_{DM0} = 8.2 µH (Coilcraft XAL1010-822MED) is sufficient at the output of the unfolder. The filter capacitors placed between the output phases, C_{DM1}, and between the respective output phase and the negative DC-Link terminal, C_2, are implemented with 4 × 2.2 µF 450 V/X6S MLCC. In order to dampen transients possibly triggered at the beginning and end of the recurring unfolder PWM operation interval, an additional damping branch is included in the first filter stage. The damping resistor $R_{DM1} \approx 1.25\ \Omega$ is implemented with 8 parallel 10 Ω 0805 SMD resistors. It should be pointed out again, that the output capacitors C_2 help to attenuate not only DM noise but also CM noise which allows to place only a single dedicated CM inductor in the EMI filter. L_{CM1} is realized with a toroidal VITROPERM 500F core (T60006¬L2009-W914) with 10 turns using 1 mm-Ø solid copper wire. To achieve the required DM attenuation, additional DM inductors L_{DM1} are placed in the second filter stage. Likewise to L_{DM0}, the same commercially available 8.2 µH inductors from Coilcraft are used. The CM capacitors C_{CM0} and C_{CM1} are implemented with 3 × 100 nF, 630 V class II/X7R MLCCs from TDK (C3225X7T2J104K160AC).

As it became evident during the experimental EMI measurements, the implemented filter as shown in Fig. 11 was not sufficient to meet the FCC Part 15 B limits at frequencies below 1 MHz. By means of measurements with a DM/CM noise separator auxiliary equipment, inserted between the LISN RF output and the test-receiver input, CM noise was identified as the main problem. To meet the EMI requirements, an additional tiny CM choke was inserted at the DC input of the converter as shown in Fig. 17. The additional choke L_{CM0} was realized with a toroidal core with outer diameter of 13.7 mm and height of 3.6 mm using also VITROPERM 500F

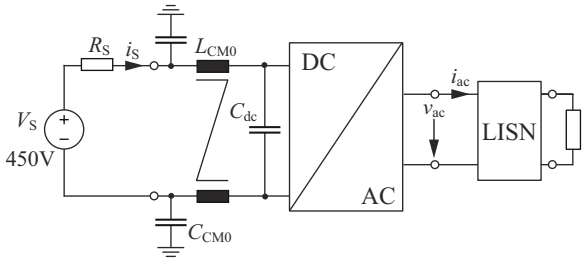

Fig. 17. Additional tiny CM choke L_{CM0} inserted at the DC input to meet the EMI limits.

(T60006-L2012-V217). The CM winding was realized with 5 turns of 0.8 mm-Ø) solid copper wire resulting in a nominal CM inductance of around 250 µH. The boxed volume of this additional CM choke is in the order of only 1.3 cm^3 (< 1.0% of the total LB 2.0 volume) and there is virtually no impact on the overall efficiency.

Since it was only intended to test the LB 2.0 hardware prototype in the laboratory, no explicit enclosure was designed. However, for the conducted EMI measurements presented next, the converter was placed on top of an aluminum baseplate which was connected to the ground/PE terminal of the EMI test setup. The ground terminal of the prototype was directly connected to the aluminum plate. The measured quasi-peak EMI spectrum of the LB 2.0 hardware prototype at 2 kW output power is depicted in Fig. 18(a). The results where again obtained with the R&S ESPI7 test receiver and the R&S ENV216 single-phase LISN which was installed between the AC output of the converter and the resistive load bank. It can be clearly seen that at low frequencies up to 20 MHz the FCC Part 15 B conducted EMI limits are met. Compared to the spectrum of the LB 1.0 prototype (shown in light grey), distinct peaks are visible at multiples of the switching frequency. As can be seen, at very high frequencies between 20–30 MHz, the measured noise just remains below the limit. Since parasitics are detrimental to the available filter attenuation at these high frequencies, it is expected that with a complete metal enclosure several dB µV of safety margin could be gained.

As described previously in Section II-D of this paper, for the ground current measurement an additional external decoupling CM choke was inserted between the DC supply (Sorensen SGI 600/17) and the input of the converter. The nominal inductance value of this decoupling CM choke is almost a factor of 9 larger compared to L_{CM0}. The measured ground current at the nominal operating point is depicted in Fig. 18(b) and its RMS value amounts to 5.7 mA which would exceed the initial strict ground current limit of 5 mA. Clearly visible are the current peaks up to 100 mA located around the zero crossings of the AC voltage which are triggered by imperfections in the transition to temporary PWM operation of the H-bridge unfolder and deviations of the DC/|AC| buck-stage output voltage v_{C1} from its reference. Without adding the additional (external) CM choke between the DC supply and the input of

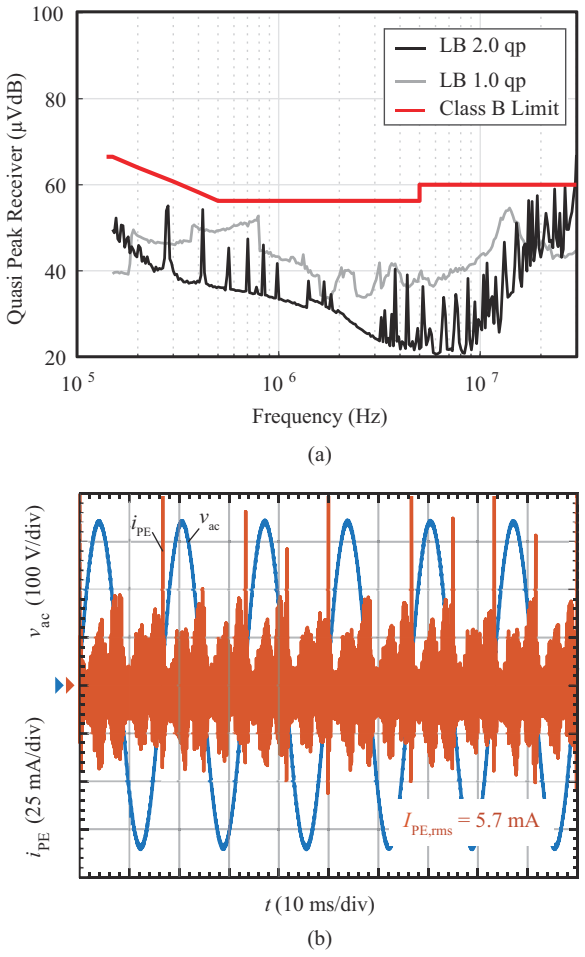

Fig. 18. (a) EMI noise spectrum of the Little Box 2.0 at 2 kW output power measured with R&S ENV216 single-phase LISN and R&S ESPI7 test receiver. (b) Ground current of the Little Box 2.0 measured by means of inserting both inverter output conductors simultaneously into the clamp of the current probe (Teledyne CP030).

the converter, the RMS value of the measured ground current amounts to 14.93 mA which is still in accordance with the revised GLBC specifications.

E. Efficiency

The measured efficiency of the LB 2.0 prototype as a function of output power is depicted in Fig. 19(a). The blue line with circle-type markers represents the efficiency of the system if two Sunon 12 V DC fans (MF25101V1-1000U-A99) are employed. The peak efficiency at 2 kW amounts to 97.4%. The red line with cross-type markers represents the measured efficiency if two 8 V high-speed fans are employed (WTF, 20 000 RPM @ 7.2 V). The total power consumption of the WTF fans amounts to ≈ 6 W which explains the drop in efficiency to 97.2% at full output power. As indicated, this is still significantly higher than the 96.3% peak efficiency achieved with the LB 1.0 converter. The CEC weighted efficiency of the LB 2.0 amounts to 96.12% with conventional fans (Sunon). Since the increased cooling performance achieved with the

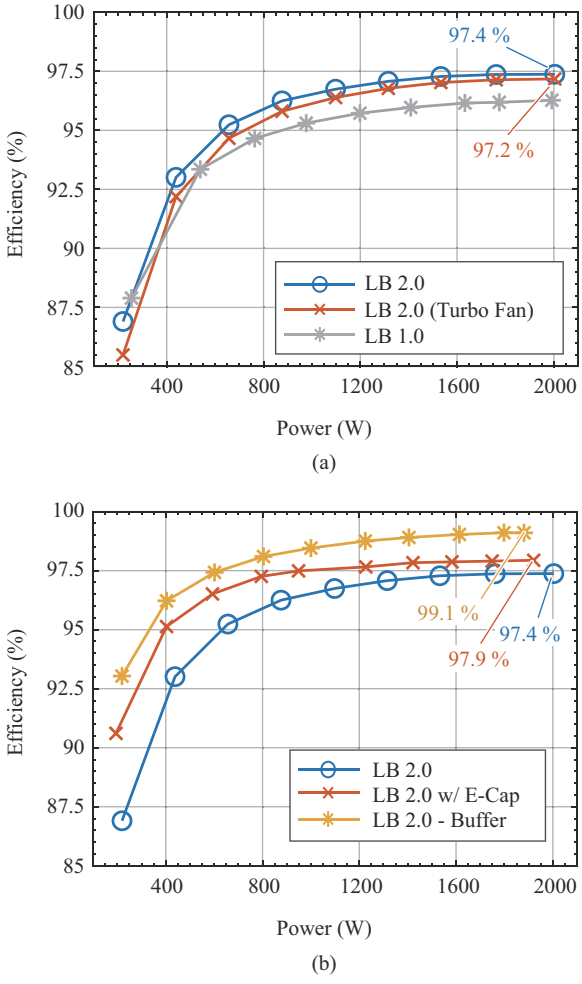

Fig. 19. Conversion efficiency of the Little Box 2.0 (LB 2.0) with respect to output power measured with a Yokogawa WT3000 precision power analyzer. (a) Efficiency with normal and high-speed DC fan and comparison with results from Little Box 1.0. (b) Efficiency with respect to output power of only the active power buffer (tested with electronic load), only the inverter equipped with electrolytic capacitors and the complete system.

high-speed fans is actually only needed at high loads above ≈ 1.7 kW and the CEC weighting coefficient at rated power is only 0.05, the lower nominal efficiency when using the high-speed fans has virtually no affect on the CEC weighted efficiency. In practice, the fan speed can be adjusted according to the output load level and/or the corresponding cooling demand (this was not considered during the experimental testing), thus it is reasonable to report a weighted efficiency of 96%. The yellow line with star-type marker depicted in Fig. 19(b) represents the efficiency of only the PCI without the inverter. For this purpose, an electronic load (Chroma 63201) was used to emulate the pulsating power caused by the inverter. It can be seen that the peak efficiency at close to rated output power exceeds 99% efficiency. Displayed in red with cross-type markers is the measured efficiency of the LB 2.0 if only the inverter is operated and the DC-link is passively buffered with high-density electrolytic capacitors (3 × 493 µF, 450 V, B43991-X0009-A223 from EPCOS/TDK). As can be seen in the plot, the peak efficiency then almost reaches 98% at full output power. Due to the high efficiency of the PCI close to rated power, replacing the electrolytic capacitors with the active power buffer only reduces the overall efficiency by roughly 0.5% In case of the LB 1.0 (cf. Section II-E), substituting the electrolytic capacitors with the more compact PCI resulted in a reduction of 1.2% in overall efficiency. The main reason for this is that compared to the CeraLink technology utilized in the LB 1.0 to realize the buffer capacitor, the X6S MLCC exhibits a much lower power loss (≈ 1.5 W instead of ≈ 17.3 W at 2 kW).

F. Cooling and Operating Temperature

As can be seen from the picture of the LB 2.0 hardware in Fig. 12, the cooling system consists of a single custom machined copper heat sink and two 25 mm × 25 mm × 10 mm DC fans. The fans are directly attached to the fins of the heat sink without an additional duct. The 4 mm thick base-plate extracts the losses from the power transistors (cooling through the PCB). The air stream exiting the heat sink, is then cooling the power inductors L_1 and L_b which are located directly after the heat sink. The fin dimensions are 20 mm × 18 mm × 0.5 mm and the channel width (distance between fins) amounts to 0.8 mm. Since manufacturing from a single copper block was not possible due to mechanical limitations, all fins were first cut from a thin 0.5 mm copper sheet and then inserted into machined channels in the baseplate and afterwards soldered for permanent fixation. Considering Sunon 12 V DC fans (MF25101V1-1000U-A99), the calculated cooling system performance index (CSPI, cf. Section III-D of Part A) is in the order of 53 W/(K dm^3). Treating the free space around the power inductors as air duct (cf. Fig. 12), the performance reduces to 37.5 W/(K dm^3).

In order to further increase the airflow passing by the power inductors and/or to limit the maximal winding temperature of the power inductors, the Sunon fans were replaced with more powerful ultra-high speed fans from WTF (20 000 RPM, re-purposed from RC model car applications) to provide better cooling in the nominal operating point as discussed previously.

The thermography image in Fig. 20 was recorded with a FLIR A655sc HD infrared camera and shows the steady-state temperature distribution of the LB 2.0 at 2 kW output power from two perspectives. The average temperature of the power stage (power transistor, gate drives, etc.) is approximately 80 °C. The power inductor of the inverter generates more losses and therefore, exhibits a higher steady-state operating temperature. The temperature of the winding reaches approximately 84 °C. However, it should be noted that surfaces exposed to the outside which would directly touch the metallic enclosure, such as the core of the power inductors, the buffer capacitor, the EMI filter, the heat or the control PCB, exhibit operating temperatures of only 50–65 °C.

IV. Discussion & Performance Benchmark

Based on the experimental results for the two hardware demonstrators provided in the previous sections, it can be

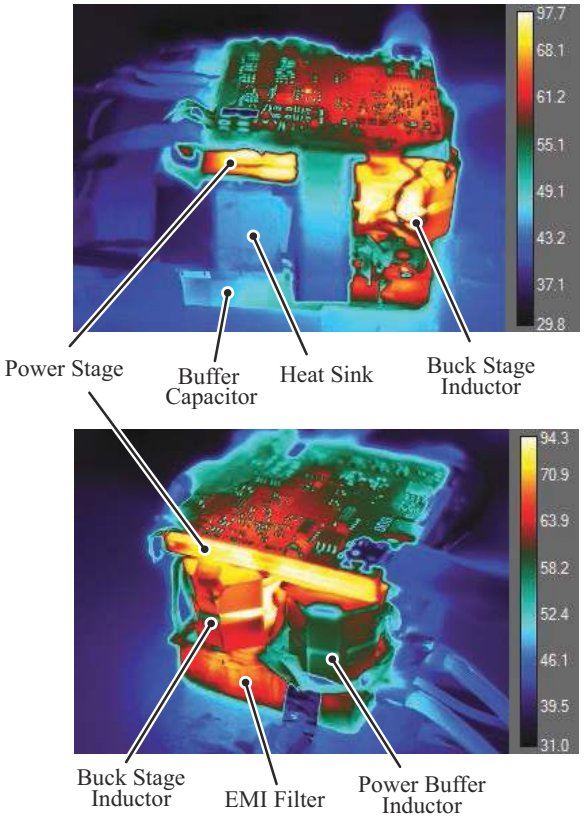

Fig. 20. Thermography images of the Little Box 2.0 (without enclosure) recorded with a FLIR A655sc infrared camera showing the steady-state temperature distribution at rated 2 kW output power.

concluded that both systems meet the technical specifications of the GLBC. Fig. 21 shows the calculated loss and measured volume distribution at 2 kW output power of the realized prototypes. As the total volume and loss figures indicate, 18 W of losses and about 103 cm^3 of volume are saved in case of the improved LB 2.0 compared to the LB 1.0. Because of the reduced power loss of the components and the higher cooling system performance, the cooling volume of the LB 2.0 was reduced from 95 cm^3 (39.6%) to 46.5 cm^3 (33.7%). Due to the installed ultra-high speed fans for improved cooling of the LB 2.0, the power consumption of the auxiliary electronics has almost doubled.

A. Main Reasons for the Higher Performance of the LB 2.0

As can be noticed by comparing Fig. 21(a) and (b), the power loss of the buffer capacitor (shown in dark blue) was significantly reduced. As described in Section II of this paper, the buffer capacitor of the LB 1.0 was implemented with 120 x 2 µF, 600 V CeraLink capacitors from EPCOS/TDK. These ceramic capacitors can be operated with a large current ripple and feature a high capacitance density which, in contrast to class II ceramics, even increases with applied bias voltage and/or temperature [11]. Furthermore, the capacitors are available in compact 20 µF or even custom-made packages making the system assembly much easier and more reliable. From this perspective, the CeraLink technology seemed to be the right choice to implement the PCI buffer in the course of the GLBC, however, it turned out that these capacitors unfortunately generate high losses when subjected to a LF AC voltage with large amplitude such as present across the PCI buffer capacitor. For this reason, in the PCI buffer of the LB 2.0 system, class II/X6S MLCCs were utilized resulting in a reduction of the buffer capacitor losses by 15.8 W. Because of the lower loss density it is also possible to operate the buffer capacitor with a larger LF AC voltage amplitude of the voltage ripple which results in a slightly lower volume despite the fact that the capacitance density of the X6S MLCCs is slightly lower compared to CeraLink capacitors.

The LB 1.0 H-bridge inverter with 4D-interleaving was implemented with a total of 4 bridge-legs each with a dedicated HF inductor. In contrast, the LB 2.0 inverter DC/|AC|buck-stage was realized with a single bridge-leg and a single HF inductor. Therefore, despite the much lower switching frequency of the LB 2.0, 140 kHz as opposed to 250 kHz–1 MHz of the LB 1.0, the total volume of the inverter's power stage – mainly determined by the power transistors and filter inductors – was reduced by roughly 50% from 40 cm^3 to 19.3 cm^3. Interestingly, despite ZVS throughout the AC period and 4D-interleaving in case of the LB 1.0, the total losses in the power transistor are considerable due to the much higher switching frequency. As analyzed in [24] and discussed in Part A of this publication, for the employed 600 V/70 mΩ GaN Gate Injection Transistor (GIT), soft-switching of 10 A at 400 V causes 2 µJ of energy dissipation per transistor and switching cycle. To exemplify, for a switching frequency of 1 MHz, this translates into 4 W of losses per bridge-leg and thus ZVS losses cannot be neglected at very high switching frequencies even if the latest GaN semiconductor technology is employed. It has been identified [24], that the lossy charging and discharging of the transistors' output capacitance (C_{oss}) during the resonant transition is the origin of the experienced ZVS losses and that the dissipated energy is a function of applied dv_{ds}/dt rather than switched current. For this reason, practically lossless class I/C0G MLCC capacitors C_{ext} = 600 pF, were added in parallel to the high-side and low-side GITs (charge equivalent parasitic output capacitance $C_{oss,Qeq}$ = 114 pF), which allowed to reduce the turn-off losses by around 30% [3]. However, due to the higher effective output capacitance $C_{oss,eff}$, now for the ZVS transient a higher amount of charge $Q_{oss,eff}$ is needed to charge/discharge the effective output capacitances $C_{oss,eff}$. This means that for a defined maximum dead time interval of $T_{dt} \approx 125$ ns (for two transitions this corresponds to 25% of a 1 MHz switching cycle), a large current of 5A is required to charge $C_{oss,eff}$ from 0V to 400 V and vice versa. This increases the peak-to-peak amplitude of the TCM current and therefore the RMS value and the associated conduction losses. Moreover, because of the remaining ZVS losses, a permanently interleaved operation of the bridge-legs at low power turned out to be no more beneficial in terms of efficiency. For this reason, the 4D-interleaving scheme as introduced in Part A with simultaneous operation of both bridge-legs only around the peak of the instantaneous output power was adopted.

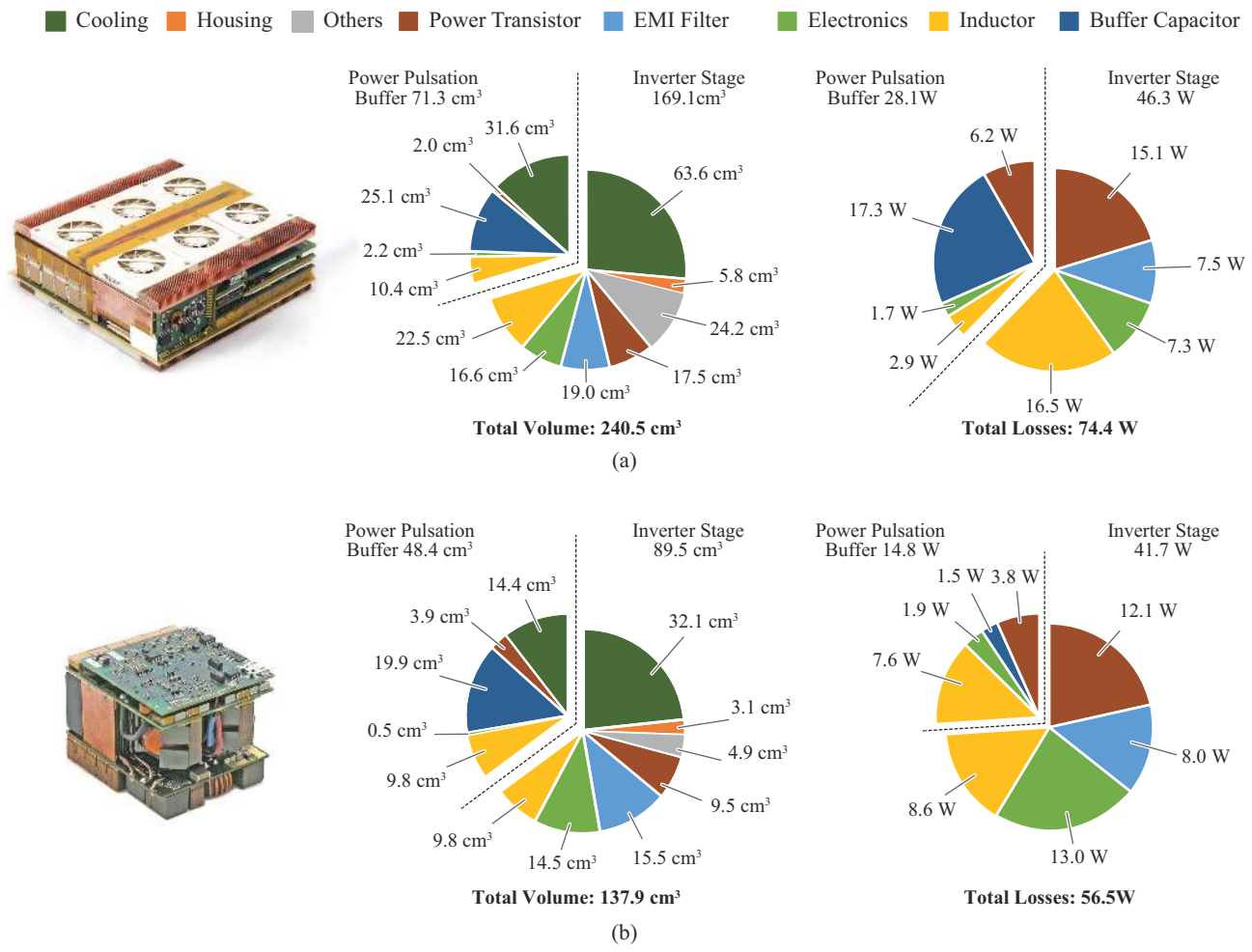

Fig. 21. Volume and power loss balance at 2 kW output power of the realized hardware prototypes. (a) Little Box 1.0 (LB 1.0). (b) Little Box 2.0 (LB 2.0).

In contrast, the inverter of the LB 2.0 with just a single bridge-leg and conventional PWM exhibits similar power transistor losses. This can be explained by the lower RMS value of the inductor current as opposed to the TCM modulation which results in lower conduction losses and the moderate 140 kHz switching frequency also limits the occurring hard-switching losses.

B. Benchmark With Google Little Box Challenge Finalists

Out of 100+ teams worldwide which submitted detailed descriptions of their technical approach, 18 teams were selected to submit their converter to Google for final testing at the National Renewable Energy Laboratory (NREL) in Golden, Colorado back in October 2015. The 1st price of the GLBC was awarded in February 2016 to the team of the Belgium company CE+T Power. Their converter achieved a power density of 8.72 kW/dm^3 (142.9 W/in^3) which is –not surprisingly –only slightly higher than the power density of the LB 1.0 converter system presented in Section II of this paper, 8.18 kW/dm^3 (134 W/in^3), since both teams were following the same technical approach (interleaved, H-bridge TCM inverter and buck-type PCI buffer). Among the 18 finalists, there were three categories: 7 teams were affiliated with technical consulting firms, 7 teams were affiliated with electrical engineering companies and only 4 teams were affiliated with universities. Moreover, 3 out of the 18 finalists did not show up at the final event. Most of the teams used either a H-bridge or a DC/|AC| buck-stage and |AC|/AC H-bridge unfolder topology to implement the inverter but overall no fundamentally new approach was presented. One of several innovative approaches worth mentioning, is the topology presented by the University of Illinois at Urbana-Champaign (UIUC), where the DC/|AC| buck-stage was realized with a 7-level flying capacitor topology using 100 V GaN transistors [25], [26]. Overall, 11 teams employed GaN power transistors, 2 teams used SiC and 2 teams relied on Si power transistors. Both, TCM modulation with ZVS throughout the AC period and variable switching frequency as well as conventional PWM with ZVS only around the ZC of the AC current and constant switching frequency were adopted by the finalists. Moreover, the majority of finalists used an active power buffer to cope with the fluctuating power at the AC side. The buck-type PCI buffer presented herein was employed by many finalists but also the partial-power stacked and series-connected active power buffer concepts were adopted [27], [28]. The majority of contestants

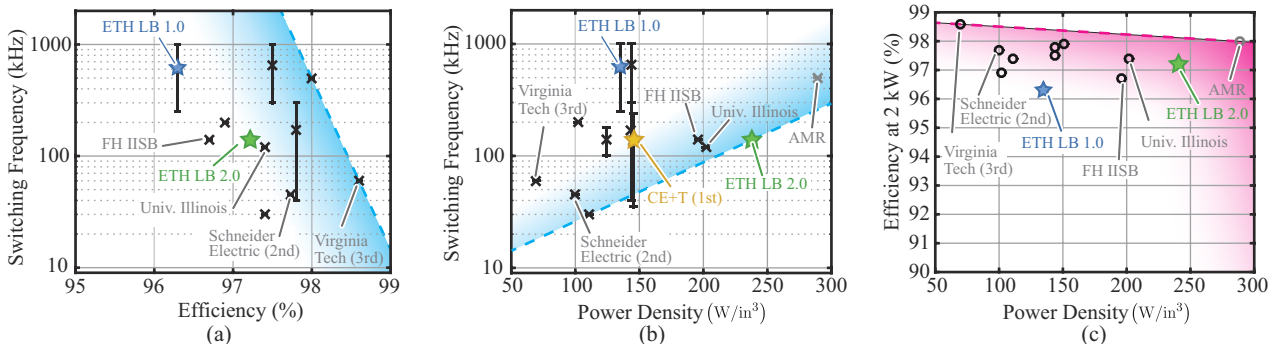

Fig. 22. Performance benchmark of the Google Little Box Challenge (GLBC) finalists concepts. The data was gathered from the technical approach documents of the finalists published by Google. Claimed performance (a) Switching frequency with respect to efficiency at 2 kW. (b) Switching frequency with respect to power density. (c) Efficiency at 2 kW with respect to power density. Note that the nominal efficiency at 2 kW of the inverter from CE+T Power is not known.

selected the 2.2 µF, 450 V, class II/X6S MLCC technology for the implementation of the buffer capacitor, in the bridge-leg output filters and for the DM capacitors in the EMI filter. To implement the HF filter inductors, a conventional approach using HF litz wire and MnZn ferrite core material was adopted by most of the finalists. Only two teams, including the authors employed a multi-gap inductor design.

Likely due to the short competition time-frame of just 15 months, none of the presented prototypes relied on advanced 3D-integration techniques such as PCB-embedding of active and/or passive components [29]. Instead, the presented hardware prototypes were altogether hand crafted engineering jewels with stacked, multi-board SMD-technology-based PCB designs with careful 3D CAD mechanical arrangement of components and a sophisticated heat management. More technical details of the individual concepts of the finalists are presented in the survey in [30].

The data for the benchmark shown in Fig. 22 was gathered from the publicly available technical approach documents of the GLBC finalists. Note, that some teams did not publish the achieved peak efficiency values are therefore not included in Figs. 22(a) and (c). Figs. 22(a) and (b) show the switching frequency with respect to the efficiency at 2 kW and with respect to the achieved power density, respectively. The interval marker indicates the variable switching frequency resulting from TCM modulation. Several teams selected a design with comparably high switching frequency in the range of 250 kHz–1 MHz, others with a much lower switching frequency in the range of 35–300 kHz. Irrespective of the frequency range, as can be seen in Fig. 22(b), the systems employing TCM reached similar power densities around 8.54 kW/dm^3 (140 W/in^3). Interestingly, two teams, i.e. Fraunhofer Institute for Integrated Systems and Device Technology (FH IISB) and the UIUC, achieved a remarkable power density around 200 W/in^3 with a comparably low switching frequency between 120–140 kHz. In case of the 7-level flying-capacitor converter, 120 kHz represents the switching frequency of a single converter cell and the effective switching frequency is actually 720 kHz. The data in Figs. 22(a) and (b) agrees with the well known tendency that increasing the switching frequency results in higher power density at the cost of a lower efficiency. The achieved efficiency with respect to power density is depicted in Fig. 22(c) and shows a clear trade-off between efficiency η and power density ρ. The majority of the teams achieved a nominal efficiency in the range of 97%–98%. Indicated with a blue and green star-type marker is the performance of the LB 1.0, described in Section II, and the improved LB 2.0, described in Section III, respectively. The yellow star marker indicates the $\eta\rho$-performance of the GLBC winners (CE+T Power). It can be seen that by means of the DC/|AC| buck-stage based inverter topology and several improvements discussed previously, the LB 2.0 converter clearly outperforms the winning team from CE+T Power in terms of power density. Interestingly, several teams including AMR (cf. Fig. 22(c)), OKE-Services and Cambridge Active Magnetics [30], claimed even higher power densities in the range of 300 W/in^3, however, no rigorous experimental evidence was published to support these claims.

C. A Critique of Little Box Challenge Inverter Designs-Revisited

In [31] a well written and comprehensive analysis of the GLBC inverter designs is provided. However, especially considering the latest progress achieved with the LB 2.0 hardware prototype presented herein, certain statements are questioned in the following. Fig. 23 shows the CEC weighted efficiency with respect to power density of the GLBC participants. The empirical trend-line of the observed trade-off between efficiency and power density of the GLBC inverter designs proposed in [31],

$$\eta = 100 - (0.04 \times \rho), \tag{10}$$

whereby ρ is the power density in W/in^3 and η is in %, is indicated by the dashed red line in Fig. 23. Although the proposed η-ρ trend-line is valid for many of the implemented designs, it fails to characterize the inverter designs with maximal power density and does not distinguish between the H-bridge based and DC/|AC| buck-stage based inverter topologies. Therefore, based on the insights gained from the conducted Pareto optimization (cf. Section IV-A of Part A), two additional η-ρ trend-lines (11) and (12) are proposed, which better describe the inverter designs of the GLBC finalists with highest power

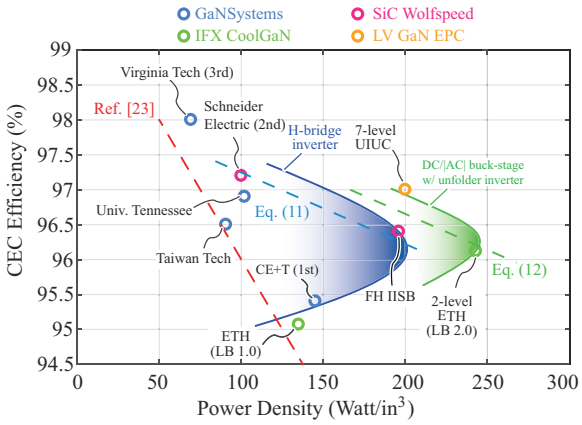

Fig. 23. CEC efficiency with respect to power density of selected Google Little Box Challenge (GLBC) participants. The efficiency and power density trade-off trend-line proposed in [31] is indicated by the dashed red line. Based on the insights gained from the Pareto optimization as presented in Part A of the paper, two additional hypothetical trend-lines for the H-bridge (dashed blue line) and the DC/|AC| buck-stage (dashed green line) based inverter concepts, more characteristic for the designs of the GLBC finalists with highest power density are proposed. Note, that only the inverter of the GLBC participants with known CEC efficiency figures are shown.

density, i.e. FH IISB for the H-bridge based inverter and UIUC for the DC/|AC| buck-stage based inverter concept, as indicated with the dashed blue and green lines in Fig. 23, respectively.

$$\eta = 98.3 - (0.0105 \times \rho), \tag{11}$$

$$\eta = 98.75 - (0.0105 \times \rho), \tag{12}$$

It should be noted that this trend-lines are just hypothetical and have yet to be confirmed.

It is therefore important to underline, that the 7-level flying capacitor inverter design should not be considered as an outlier with respect to the H-bridge based designs as stated in [31] but rather as a design which follows the η-ρ trade-off characteristic of the DC/|AC| buck-stage based inverter topologies.

Furthermore, the statement in [31] that employing Infineon CoolGaN devices in the inverter results, in low efficiency and just slightly higher power density compared to other GaN-based H-bridge designs is clearly challenged. It can be seen from Fig. 23, that in case of the LB 2.0 inverter which employs the same CoolGaN devices as the LB 1.0 prototype, both η and ρ was increased. In this respect, it is important to emphasize that a holistic consideration of the employed topology and of all power electronic constituents is necessary to get a complete picture and thus understand the main driver of system performance. The consideration of only the power semiconductors is not sufficient. This is also exemplified by the $\eta\rho$-Pareto front simulation study depicted in Fig. 24 carried out for the H-bridge TCM inverter. In this study, scaling factors $k_c \in [0, 1]$ and $k_s \in [0, 1]$ of the transistor conduction and switching losses, respectively, are introduced to gradually idealize the power semiconductor properties. (k_c =1, k_s =1) represents the real GaN transistors (Infineon CoolGaN) and (k_c =0, k_s =0) represents idealized switches without any

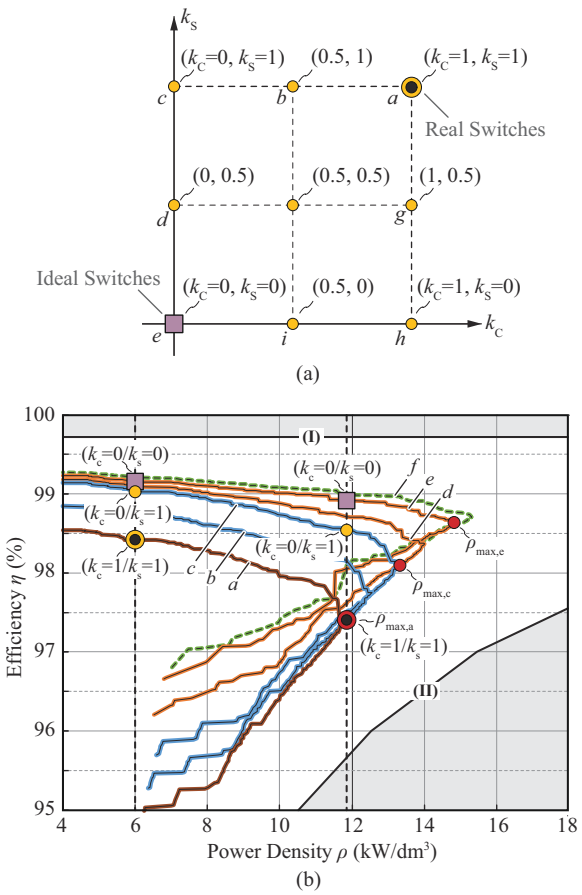

Fig. 24. (a) Scaling factors $k_c \in [0, 1]$ and $k_s \in [0, 1]$ of the conduction and switching losses, respectively, used to gradually idealize the power transistor properties; (k_c =1, k_s =1) represents the real GaN transistors (Infineon CoolGaN), (k_c =0, k_s =0) represents idealized switches without any conduction and switching losses. (b) The $\eta\rho$-Pareto fronts associated with the inscribed coordinates (k_c, k_s) for the H-bridge inverter with Triangular Current Mode (TCM) operation (cf. Fig. 3 of this paper).

conduction and switching losses. It can be seen in Fig. 24(b) how idealizing the GaN transistors gradually improves both η and ρ. Once conduction, switching and gate drive losses of the power semiconductors are completely excluded (ideal switches), the $\eta\rho$-Pareto front is exclusively determined by the filter passives, heat sink and auxiliary electronics. Naturally, if these components are implemented poorly, the resulting $\eta\rho$-performance is moderate even if ideal semiconductors would be at one's disposal.

D. Concerning an Industrial Implementation

The components of the realized hardware prototypes presented in this paper are all operated within their safe operating area recommended by the manufacturers. The electrical distances in the PCB layouts satisfy laboratory requirements but do not comply with industrial creepage distance requirements. However, this can be addressed with a higher level of integration and advanced packaging. Although the employed high energy density ceramic capacitors significantly improve power density, they are by no means an option for a cost-

sensitive application. To exemplify, the active power buffer of the LB 2.0 uses 200 pieces of the 2.2 µF class II/X6S MLCC which amounts to $290 of component cost for the buffer capacitor (Digikey, order quantities above 1000 pieces). In contrast, using electrolytic capacitors for passive buffering of the DC-link amounts to only $14.85 of component cost (3 × 470 µF from TDK's ultra-compact 450 µF B43640 series, at least 1.1 mF needed to satisfy the voltage ripple requirement). This cost consideration is likely also the reason behind Schneider Electrics' series-connected partial-power buffering approach which only relies on electrolytic capacitors [28]. In case of the LB 2.0, if electrolytic capacitors are employed instead of the active power buffer, then the power density would drop from 14.8 kW/dm^3 (243 W/in^3) to approximately 9.48 kW/dm^3 (155.4 W/in^3) considering a boxed volume of 121.5 cm^3 of the electrolytic capacitor assembly. Based on this consideration, a power density in the range of 6–9 kW/dm^3 (100–150 W/in^3) is reasonable for a cost-constraint industrial inverter implementation in accordance with the GLBC specifications.

V. Conclusion & Outlook

In this paper the experimental results of two GaN-based converter concepts in accordance with the Google Little Box challenge (GLBC) specifications were presented. The first realized inverter, a 2-level H-bridge based inverter topology with interleaved bridge-legs, Triangular Current Mode (TCM) modulation with variable switching frequency in the range of 250 kHz–1 MHz, and a buck-type Parallel Current Injector (PCI) power buffer, achieved a power density of 8.18 kW/dm^3 (134 W/in^3), a nominal efficiency of 96.4% and a California Energy Commission (CEC) weighted efficiency of 95.07%. This inverter, termed Little Box 1.0 (LB 1.0), was presented at the GLBC finals and was ranked among the top 10 out of 100+ contestants. The second realized hardware prototype (Little Box 2.0, LB 2.0) brings together all research findings and lessons learned during and after the GLBC and is composed of a 2-level DC/|AC| buck-stage operated with constant 140 kHz PWM and a subsequent |AC|/AC H-bridge unfolder. Because of the inherently generated low-frequency Common Mode (CM) voltage, this topology was not considered initially but became a truly viable option once the specified ground current limit was relaxed from 5 mA to 50 mA at a very late point during the competition. The LB 2.0, is also equipped with a buck-type PCI buffer but is realized with a more efficient buffer capacitor technology and exhibits a staggering power density of 14.8 kW/dm^3 (243 W/in^3), a nominal efficiency of 97.2% and a CEC weighted efficiency of 96.1%. Compared to the other LBC finalists as reported in [30], [31], the LB 2.0 inverter therefore sets a new experimentally supported benchmark with respect to power density for a single-phase inverter in accordance with the GLBC specifications.

Given the super-fast switching characteristics of GaN power transistors without reverse recovery, strictly ensuring ZVS throughout the entire mains period is not necessary. In fact, the resulting high RMS current due to TCM bridge-leg control causes high conduction losses which potentially outweighs hard turn-on losses typically occurring around the peak value of the AC current when operated with conventional, constant-frequency PWM but with a comparably large current ripple.

To further improve power density, low-loss ceramic capacitors which tolerate a large AC ripple and feature a very high energy density are needed. This ceramic capacitor technology also must facilitate the implementation of large capacitor blocks in the range of 100–200 µF. Equally important is the availability of high-frequency low-loss magnetic materials with high saturation flux density to implement compact, low-loss inductors.

It was demonstrated that with a 2-level bridge-leg implementation of the DC/|AC| buck-stage based inverter topology (LB 2.0) a power density of 250 W/in^3 is in reach. Based on the current available technologies, a further improvement of power density can be achieved with a flying capacitor multi-level approach to shrink the size of the bridge-leg filter inductors and the EMI filter. As it becomes evident from the work in [25], [26], [32], the volume contribution of providing voltage and signal isolation to the individual switching cells of the flying capacitor converter is, besides the performance limitation imposed by the ceramic capacitors, one of the current barriers for achieving a higher power density. With advanced packaging and a higher level of integration it would not come at a surprise to see power density values in the range of 250–300 W/in^3 for this type of converter in the very near future. Another strategy to improve the power density is to more tightly incorporate the power buffer into the operation of the inverter as presented in [33], [34], because this would allow to eliminate the bridge-leg filter inductor employed in the PCI buffer. This approach is subject of current research and would potentially allow to improve the power density of the LB 2.0 approach by up to 10%–15%.

Acknowledgement

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The list of references only includes the literature cited in part B of the paper at hand. Please see part A for further references.

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