

The Extended Overlap Alternate Arm Converter: A Voltage-Source Converter With DC Fault Ride-Through Capability and a Compact Design

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Abstract—The alternate arm converter (AAC) was one of the first modular converter topologies to feature dc-side fault ride-through capability with only a small penalty in power efficiency. However, the simple alternation of its arm conduction periods (with an additional short overlap period) resulted in 1) substantial six-pulse ripples in the dc current waveform, 2) large dc-side filter requirements, and 3) limited operating area close to an energy sweet spot. This paper presents a new mode of operation called extended overlap (EO) based on the extension of the overlap period to 60°, which facilitates a fundamental redefinition of the working principles of the AAC. The EO-AAC has its dc current path decoupled from the ac current paths, a fact allowing 1) smooth dc current waveforms, 2) elimination of dc filters, and 3) restriction lifting on the feasible operating point. Analysis of this new mode and EO-AAC design criteria are presented and subsequently verified with tests on an experimental prototype. Finally, a comparison with other modular converters demonstrates that the EO-AAC is at least as power efficient as a hybrid modular multilevel converter (MMC) (i.e., a dc fault ride-through-capable MMC), while offering a smaller converter footprint because of a reduced requirement for energy storage in the submodules and a reduced inductor volume.

Index Terms—AC–DC power conversion, active filters, capacitive energy storage, HVDC transmission, power system faults, power transmission protection.

I. INTRODUCTION

MODULAR-TYPE converters [1] have established themselves as the accepted standard approach for

voltage-source converters (VSC) because they provide an adequate solution to the growing demand for HVDC projects, such as offshore wind farms and multiterminal HVDC networks [2], [3]. The well-established modular multilevel converter (MMC) [4] offers both high power efficiency and high-quality waveforms. These improvements have been made possible, thanks to the use of many submodules (SMs) connected in series in stacks and the charged SM capacitors [5]–[7] switched in the arm current conduction path one at a time. The half-bridge SM version of the MMC is the most power efficient variant but requires large arm inductors [8] to limit di/dt and prospective fault current arising from dc-side faults. On point-to-point HVDC links, we may also require bypass thyristors in the SMs in order to protect the freewheel diodes from excessive fault currents before the ac circuit breakers open, preventing any further rectification of ac-side fault current [9], and on multiterminal schemes, dc circuit breakers [10]–[14] are needed in order to prevent the entire dc grid from being blacked out as a result of a single dc-side fault. Recent design innovations have helped the MMC to cope with these fault situations either by using hybrid stacks consisting of both full- and half-bridge SMs [15]–[20] or new SM circuits such as the double clamped submodule [21]–[24] and other designs [17], [25]–[27].

A. Alternate Arm Converter

An alternative approach opened the development of hybrid VSC topologies [27]–[36], which mix some elements of the classic VSC and the MMC. The alternate arm converter (AAC) [28], [33], [34] is a hybrid between the two-level converter [in the form of series-connected insulated-gate bipolar transistors (IGBTs), called director switches (DSs)] and the MMC (by using stacks of SMs in its arms in series with the DSs). The operating principle of the AAC consists in alternating the conduction of its top and bottom arms, in effect rectifying the ac currents into the dc current, with the SM stacks being used to maintain ac-side waveform quality. The advantage of alternate use of the arms is the reduction of the maximum voltage rating of the stacks, meaning that the AAC operates with fewer SMs than the MMC at similar power and dc voltage ratings. Furthermore, the stacks of the AAC consist of full-bridge SMs which the converter utilizes to increase the ac voltage magnitude higher than the dc terminal voltage, in order to reach the “sweet-spot” operating

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point (i.e., $\hat{V}_{AC} = \frac{2}{\pi} V_{DC}$). This also facilitates blocking dc-side faults [34], [37], as the stacks have sufficient negative voltage capability to oppose the ac-grid voltage. During such events, the AAC can also act as a STATCOM in order to support the ac grid [34], [38], [39], similar to the system described in [40].

However, the previously proposed operating mode of the AAC exhibits several shortcomings [11], [41]. First, the rectification of the ac currents leads to distortions into the dc current waveform in the form of large six-pulse ripples. This implies that this topology requires bulky and costly dc filtering capacitors in order to smooth the dc current waveform. Second, the ac current must rapidly commute from positive to negative dc terminal in the middle of a short overlap period. This overlap period is also when both the top and bottom arms balance their SM energy. The sharp transitions in the arm current waveforms, especially when reactive power is being generated, can be challenging to achieve. Third, the energy management of the AAC and, by extension, its satisfactory operation are severely limited by the short length of the overlap period (e.g., 10°) leading to an unrealistic demand for balancing currents as the converter operates away from the sweet spot.

B. Extended Overlap

A proposal [42] was made to increase the length of the overlap period of the AAC to one-sixth of a cycle (i.e., 60°) to facilitate active filtering of the dc current. In this paper, the additional degrees of freedom in the current paths created by an overlap period of 60° are exploited to create a new operating regime, which is termed the extended-overlap AAC (EO-AAC). The circuit topology of EO-AAC (see Fig. 1) remains broadly the same as the standard AAC operating with a short overlap (e.g., 10°), which is here referred to as the SO-AAC. Providing 60° of overlap ensures that there is always one (and only one) phase in the overlap mode, and this means that there is always a path for circulating dc current. Furthermore, it will be shown in Section II-B that the three ac phase currents sum to zero at a point within the converter and do not, at any time, flow via the dc link. This is similar but not identical to the feature of the MMC in which the phase currents sum to zero at the positive and negative dc poles and is advantageous in that it removes the six-pulse ripple current that was present in the SO-AAC and which resulted in the requirement for a substantial dc-bus capacitor (equivalent to two stacks of SM capacitors [7]) for filtering purposes. In the EO-AAC mode, the sweet spot that was a feature of the SO-AAC no longer exists because the dc current is independent of the flow of the rectified ac currents, and this allows the EO-AAC to operate away from its nominal operating point without a large penalty in balancing currents. The analysis of the EO-AAC to be described in Section II-C shows that there is an operating point at which the arm current waveforms are free from sharp transitions so that soft switching of the DS is readily achieved, but that operation away from the optimal point is satisfactory. The increase in the overlap period implies that a higher voltage is required from the SM stacks, and therefore, more SMs of a given voltage capability would be

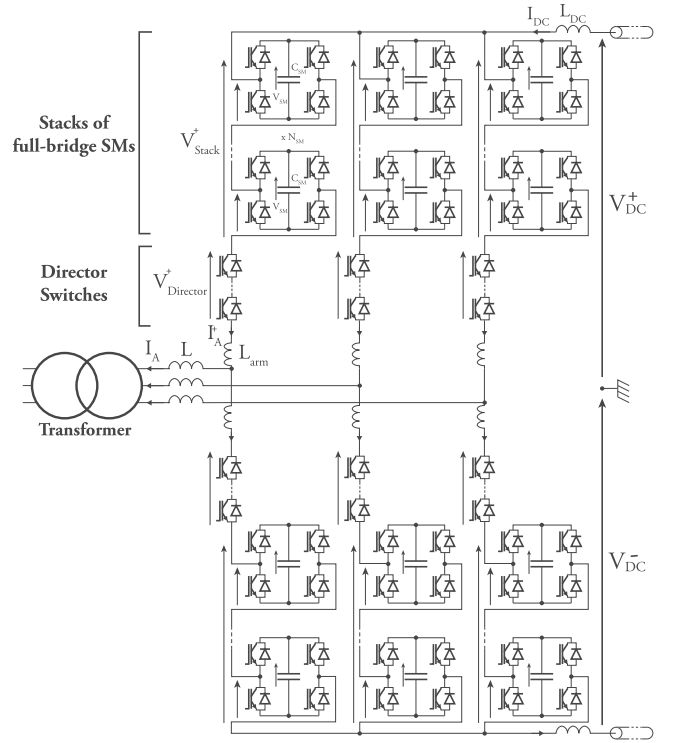


Fig. 1. Topology of the EO-AAC.

required. This has been mitigated, as described in Section II-D, by the use of a triplen harmonic voltage injection chosen not to flatten the peak of the phase voltage but to modify the zero crossing happening during the overlap periods.

Any comparison of multilevel converter topologies and operating modes must address the number of semiconductor devices, the power loss, and the volume incurred by the passive components such as SM capacitors, arm inductors, and ac- or dc-side filters. Analysis described in Sections II-E and II-F identifies the requirements for the SM capacitors and arm inductors of the EO-AAC. The EO-AAC is compared with other modular converters in Section IV, where the EO-AAC is seen to offer the good waveform quality and the wide operating range of the MMC. The efficiency is marginally better than the hybrid MMC (H-MMC) (with an equal mix of half- and full-bridge SMs). The EO-AAC retains the advantages of the SO-AAC such as dc fault ride-through, reduced number of SMs, and small total volume of SM capacitors.

C. Contribution of This Paper

This paper presents numerous new aspects about the EO-AAC with the main contributions listed as follows.

- 1) Extension of the overlap period to 60° , enabling a re-definition of the AAC operating principles, backed by experimental data from a lab-scale converter.
- 2) Removal of the sweet spot, a linear relationship between the ac and dc voltage magnitudes at which the SM capacitor voltages are stable. This permits the EO-AAC to operate over a much wider ac voltage magnitude variations compared to its short overlap version.

- 3) Explanation of the routing of the ac and dc currents through the conductive arms, changed six times per cycle; this allows smooth ac and dc current waveforms.
- 4) Optimization of the ac voltage magnitude in relation to the dc-bus voltage magnitude, leading to gapless arm current waveforms.
- 5) Introduction of a triangular zero-sequence voltage waveform to optimize the ratio of SMs to DS devices.
- 6) Quantification of the required minimal SM capacitance for a fixed voltage deviation under all normal P-Q operating conditions.
- 7) Discussion on the minimum number of inductors to ensure correct operation of the EO-AAC.
- 8) Comparison, using simulation modes at 1 MV dc, between the half-bridge MMC (HB-MMC), H-MMC, SO-AAC, and EO-AAC, including power loss estimation obtained from simulation models.

II. EXTENDED OVERLAP ALTERNATE ARM CONVERTER

A. Converter Topology

The EO-AAC has essentially the same circuit topology as the SO-AAC but with some changes, as illustrated in Fig. 1. The features in common are that the six arms each consist of a stack of full-bridge submodules (FB SMs) in series with a DS. A DS is a set of series-connected semiconductor power modules switched together at the fundamental frequency. When the DS is closed, the SM stack generates the necessary voltage to control the arm current. When the DS is open, the blocking voltage is shared between the SM stack and the DS. Thanks to their soft-switching operation, the DSs can be made of other semiconductor technologies (than IGBTs), which exhibit better conduction than switching losses, such as integrated-gate commutated thyristors.

The key difference is that the EO-AAC no longer requires a large dc-bus capacitor to keep the dc-bus voltage constant because the EO-AAC no longer generates a large six-pulse ripple in its dc current waveform. A second difference is that the principal inductances included for current control are phase reactors (normally in the form of the leakage reactance of the interface transformer) and an inductor at each dc pole. Arm inductance is still shown in Fig. 1, but this is to recognize the stray inductance inherent in the layout of the SM stacks. Thus, there are now only two explicit reactors compared to the six of the SO-AAC or MMC. The rationale for this is explained in Section II-F.

B. Conduction States

The EO-AAC has very different modes of operation compared to the SO-AAC. With an overlap period of 60° , there are six different arm conduction states, as illustrated in Fig. 2, and in each conduction state, there are exactly four arms conducting, two top arms and two bottom arms, with one top and one bottom arm in the same phase (thus being in overlap mode). The currents flowing in the six arms for each of the six conduction states are noted in (1)–(6) within Fig. 2. The fact that there is always one phase with both of its arms conducting is important because

there is, therefore, always a path for dc current (the dashed green path in Fig. 2) to circulate through a pair of arms resulting in the dc-link current being independent from the rectification of ac phase currents. Examining the three ac phase currents (the solid red, yellow, blue paths in Fig. 2) in each state, it can be seen that they meet at the midpoint of the arms of the phase that is in overlap, and therefore, at this point, they sum to zero and do not circulate through the dc link.

These two features of the 60° extended-overlap mode of operation are important. The fact that the three ac currents meet and cancel within the converter, and not in the dc link as was the case for the SO-AAC, means that the dc current waveform does not include the six-pulse ripple arising from direct rectification by the simple alternation of the arm conduction periods, which, in turn, means that there is no need for a dc-side filtering capacitor to provide a low-impedance path to the six-pulse ripple. The fact that there is always a path for dc current through a pair of arms, not just for short periods as in the SO-AAC, means that the ac- and dc-side powers can be balanced, regardless of the ac-to-dc voltage ratio. This results in the elimination of the energy-balancing sweet-spot limitation that was inherent to the SO-AAC.

C. AC Voltage Magnitude

The natural energy balance provided by the sweet spot of the SO-AAC tied the converter to operating close to one ac voltage magnitude that was a certain ratio of the dc voltage. The EO-AAC is freed from this constraint, and fresh optimization of the ac voltage magnitude can be undertaken. The changes of conduction path inherent to AAC operation (through the action of the DS) can lead to abrupt changes in the arm currents. It is possible to choose an ac voltage magnitude that reduces or eliminates sharp transitions in the arm current waveforms and thus eases the burden on the current regulators. Note that even when the arm currents have sharp transitions, the phase currents and dc current remain smooth.

The approach adopted here is that, by equating the arm current equations (1)–(6) at their respective period boundaries, a pair of alternative conditions for smooth arm currents can be obtained [see (10) and (11)]. To illustrate this, the change in the current equation of the upper arm in phase A when the transition from State (1) to State (2) is made at $\omega t = \frac{\pi}{6}$ is taken as an example:

$$\begin{cases} (1) : I_A^+ \left(\frac{\pi}{6} \right) = I_{DC} - \hat{I}_{AC} \sin \left(\frac{5\pi}{6} + \Phi_{AC} \right) \\ (2) : I_A^+ \left(\frac{\pi}{6} \right) = \hat{I}_{AC} \sin \left(\frac{\pi}{6} + \Phi_{AC} \right). \end{cases} \quad (7)$$

The current magnitudes in (7) can be substituted by the voltage magnitudes by using the definition of active power (8) so that the condition for smooth arm current waveform can be expressed as (9):

$$P = \frac{3}{2} \hat{V}_{AC} \hat{I}_{AC} \cos(\Phi_{AC}) = V_{DC} I_{DC} \quad (8)$$

$$3 \hat{V}_{AC} \cos(\Phi_{AC}) = 2 V_{DC} \cos(\Phi_{AC}). \quad (9)$$

There are two possible solutions for (9). The first solution (10) indicates that if the peak ac phase voltage is equal to two-thirds

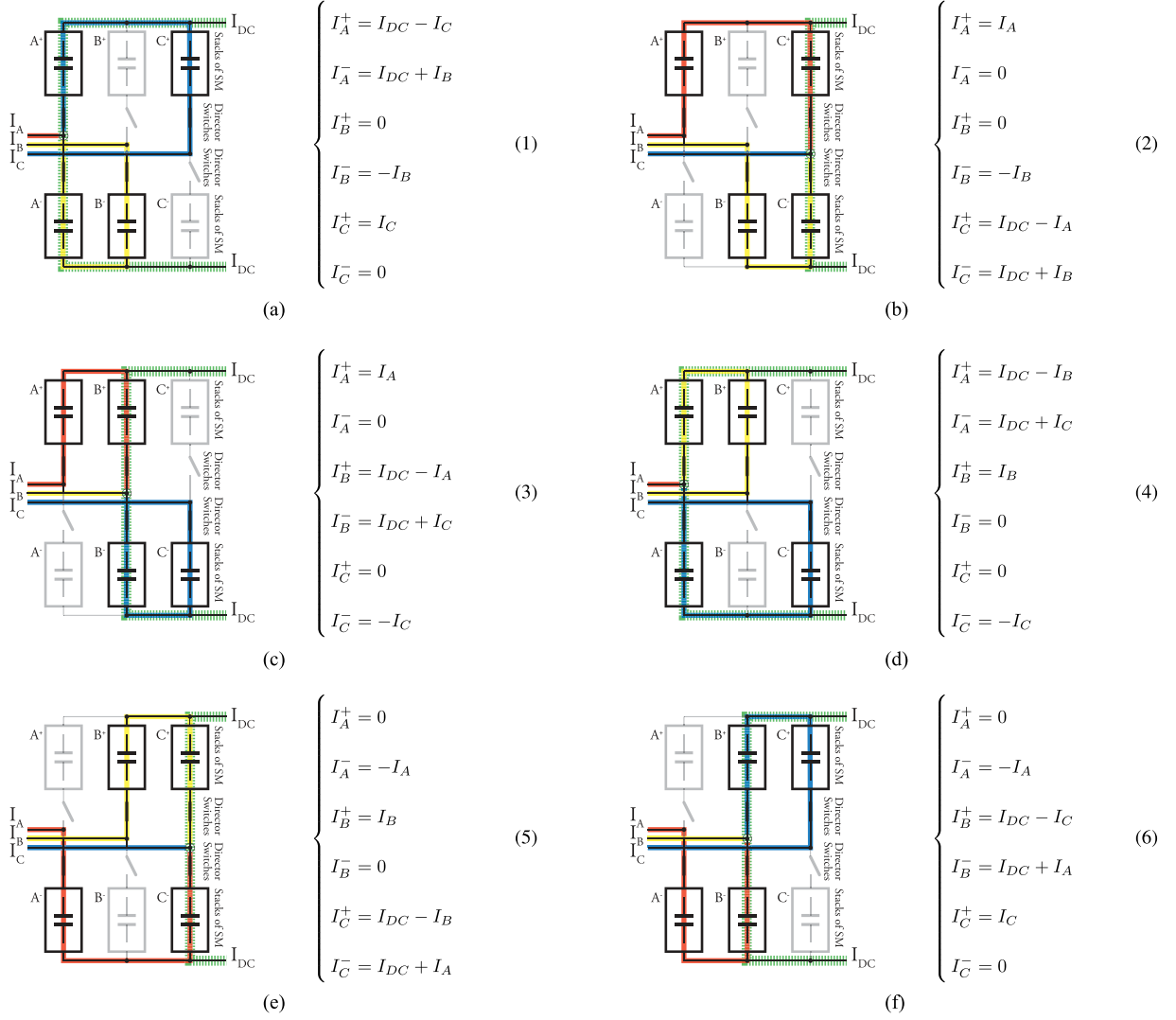


Fig. 2. Six different conduction states of the EO-AAC, showing the current paths and arm current equations. (a) $-\frac{\pi}{6} \leq \omega t \leq \frac{\pi}{6}$. (b) $\frac{\pi}{6} \leq \omega t \leq \frac{\pi}{2}$. (c) $\frac{\pi}{2} \leq \omega t \leq \frac{5\pi}{6}$. (d) $\frac{5\pi}{6} \leq \omega t \leq \frac{7\pi}{6}$. (e) $\frac{7\pi}{6} \leq \omega t \leq \frac{3\pi}{2}$. (f) $\frac{3\pi}{2} \leq \omega t \leq \frac{11\pi}{6}$.

of the dc-bus voltage magnitude, then the mix of dc and ac currents in the arm current (under constant power flow conditions) will lead to smooth transitions into or out of the overlap period. The second solution (11) states that, regardless of the ac-to-dc voltage ratio, the arm current will always be smooth if only reactive power is generated by the converter (i.e., no active power)

$$(9) \Rightarrow \hat{V}_{AC} = \frac{2}{3} V_{DC} \quad (10)$$

$$\text{or } \Rightarrow \Phi_{AC} = \frac{\pi}{2} + k\pi. \quad (11)$$

The two conditions (10) and (11) for smooth arm current waveforms are illustrated in Fig. 3, in which the expected arm current waveform (for the upper arm in phase A) is shown for six operating conditions: three choices of ac voltage and two choices of power factors. On the left-hand side are the results for real power only (unity power factor) and for an ac-grid voltage that is 120%, 100%, and 80% of the optimal ratio (10) of the dc

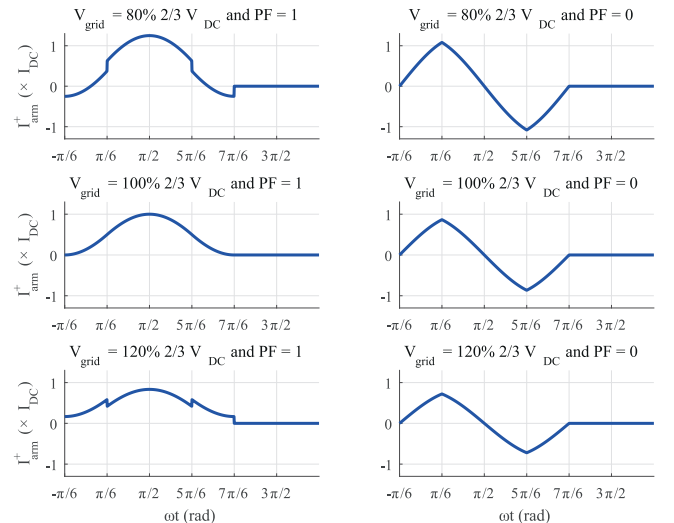


Fig. 3. Arm current waveforms for different ac-to-dc voltage ratios and power factors.

voltage. Only for the optimal case is the waveform seen to be smooth; at 80% and 120%, the waveform has discontinuities at the boundaries of the conduction states. However, even with a voltage 20% away from the optimal case, the discontinuities are not as pronounced as for the SO-AAC. On the right-hand side of Fig. 3 are the results for reactive power only (power factor zero), and here, it can be seen that the waveforms are continuous for all ac voltage magnitudes (although the slope changes abruptly). It can be expected that, in general, the arm current waveforms will be smoother when reactive power is flowing in addition to real power. A smooth current waveform at the conduction state boundaries is important in easing the burden on the current regulators but also means that the current returns to zero at the end of the arm's conduction period, and thus, soft switching of the DS can be ensured without additional control action. These are good reasons to operate at or close to the optimal voltage ratio.

D. Triplen Harmonic Voltage Injection

Extending the overlap period directly influences the required voltage rating of the SM stacks because they are required to match the ac voltage waveform for longer than half a cycle and, therefore, for a voltage swing of more than half of the peak-to-peak phase voltage. A means to mitigate this rating increase was suggested in [43] and consists in injecting a specific triplen harmonic voltage. Equation (12) describes this triplen harmonic voltage, where k_3 represents the magnitude relative to half the peak ac voltage and $\text{tri}(3t)$ is a triangle wave at three times the ac-grid frequency

$$V_3(t) = k_3 \frac{\hat{V}_{AC}}{2} \text{tri}(3t). \quad (12)$$

Equation (13) describes the voltage that appears across an arm, which is thus split between the SM stack and DS within the arm

$$\begin{cases} V_{\text{Arm}}^+(t) = \frac{V_{DC}}{2} - (V_{AC}(t) + V_3(t)) \\ V_{\text{Arm}}^-(t) = V_{\text{Stack}}^+(t) + V_{\text{Director}}^+(t). \end{cases} \quad (13)$$

Fig. 4 illustrates the voltages of the SM stacks and DSs needed to create the arm voltage for $k_3 = 0, 0.5, \text{ and } 1.0$. With no triplen harmonic, the SM stack must produce $+0.86$ and -0.27 times V_{DC} . Adding the triangle wave term reduces the peak positive voltage of the stack and increases the negative voltage (making better use of the bipolar capability of FB SMs within the stacks) until, at $k_3 = 1.0$, the use is symmetric at $\pm 0.5 V_{DC}$. Another way of looking at this is that adding the triplen voltage in this fashion has flattened the region of the zero crossing of the converter voltage and accentuated the peak voltage. This is the opposite sense and effect with which triplen harmonic injection is normally used in power converters. This use of triplen harmonic voltage has the benefits of lowering the voltage rating of the stacks, thus reducing the number of SMs required, but it also increases the voltage rating (and number of devices) of the DSs due to the increased value of the peak converter voltage.

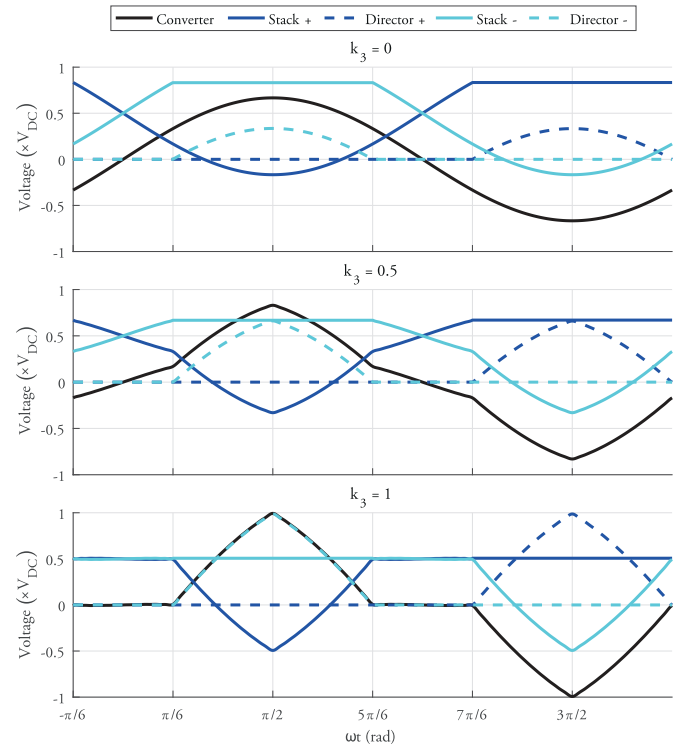


Fig. 4. Stack of SM and DS voltage waveforms for triplen harmonic injection magnitudes.

The voltage rating of the stacks of SMs and DSs is dictated by two points in the fundamental cycle. The following example considers the upper arm in phase A (A^+), but it can be reworked for the other arms, using the symmetry of the converter. First, at the end of the overlap period, i.e., the transition from State (4) to State (5) at $\omega t = \frac{7\pi}{6}$ in Fig. 2, the stack should ideally generate its maximum voltage, while the DS voltage is still zero (necessary for zero-current, zero-voltage soft-switching). Second, at the minimum point of the converter voltage waveform, i.e., at the transition from State (6) to State (6) at $\omega t = \frac{3\pi}{2}$ in Fig. 2, arm A^+ is not conducting and the DS has to support the difference between the ac- and dc-grid voltages minus the contribution from the stack which should be its maximum voltage. Implementing the above factors into (13) leads to the following voltage equations:

$$\begin{cases} \hat{V}_{\text{Stack}} = \frac{V_{DC}}{2} + \hat{V}_{AC} \left(\frac{1}{2} - \frac{k_3}{2} \right) \\ \hat{V}_{\text{Director}} = \hat{V}_{AC} \left(\frac{1}{2} + k_3 \right). \end{cases} \quad (14)$$

At $k_3 = 1$, the converter voltage waveform is flat for the entire overlap period, thus reducing the SM stack voltage rating to its lowest possible value at exactly half the dc-bus voltage. However, under this same condition ($k_3 = 1$), the SM stacks would also be rated at less than the ac peak voltage magnitude, which would mean that insufficient SM stack voltage is present to fully control the arm currents with a dc-side short-circuit fault. A better solution lies at $k_3 = 0.5$, where the converter voltage waveform is only half its usual voltage magnitude during the overlap period. Under this condition, the SM stack voltage rating is exactly equal to the ac-grid peak voltage at the end of

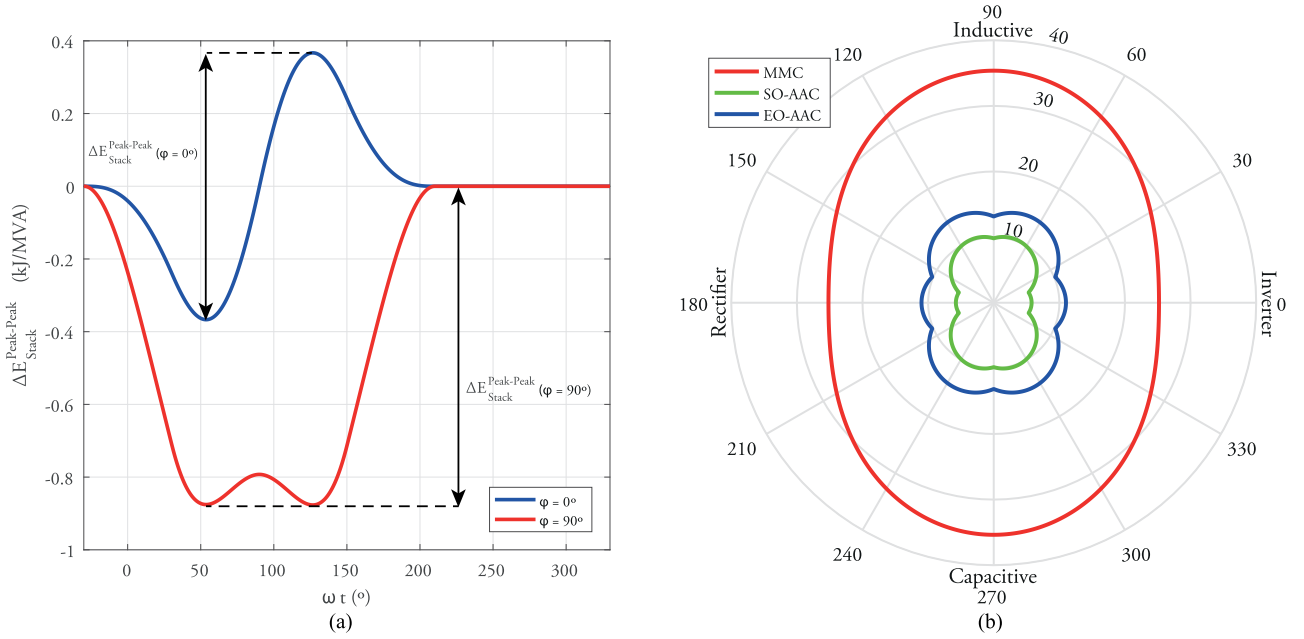


Fig. 5. Numerical analysis of the energy deviation and capacitor sizing in the AAC and MMC. (a) Energy deviation profile (in kJ/MVA) of one stack in the EO-AAC for two different ac current angles, assuming 50-Hz operation. (b) Total relative energy requirement (in kJ/MVA) in the six SM stacks of the EO-AAC and other modular converters, depending on the ac current phase angle, assuming $\Delta V = 10\%$ and 50 Hz operation.

the overlap period. Substituting $k_3 = 0.5$ in (14) and using the optimal ac voltage magnitude (10) leads to equal voltage ratings for the SM stack and DS as defined in the following:

$$\hat{V}_{\text{Stack}} = \hat{V}_{\text{Director}} = \frac{2}{3} V_{\text{DC}}. \quad (15)$$

The number of SMs in the stacks and the number of series-connected power modules in the DSs can be found from (15) based on the voltage ratings of an SM and of a single DS power module.

E. Capacitor Sizing

Like all modular converters, the EO-AAC requires sufficient voltage on the SM capacitors of each stack to maintain control of the arm currents. The SM capacitance has to be chosen large enough to ensure that the voltage deviation over a fundamental cycle caused by conduction of current is within some specified range. In the methodology developed in [7] and summarized in (16), the minimum SM capacitance is obtained by first estimating the peak-to-peak energy deviation for operation across the region of $P + jQ$ plane that is required and identifying the worst case. This highest energy deviation is then combined with the allowed SM voltage deviation (ΔV) to identify the capacitance

$$\begin{cases} \Delta E_{\text{Stack}}(t) &= \int_0^t V_{\text{Stack}}(\theta) I_{\text{Stack}}(\theta) d\theta \\ E_{\text{Stack}}^{\text{Nominal}} &\geq \frac{\Delta E_{\text{Stack}}^{\text{Peak-Peak}}}{4 \Delta V} \\ C_{\text{SM}} &= \frac{2 E_{\text{Stack}}^{\text{Nominal}}}{N_{\text{SM}} V_{\text{SM}}^{\text{Nominal}^2}}. \end{cases} \quad (16)$$

Fig. 5(b) plots the total relative energy requirement for all power factor angles, indicated in total nominal capacitive stored

energy across all six stacks (in kJ) per units of converted apparent power (in MVA). It is seen that the EO-AAC has a somewhat higher intracycle energy deviation than the SO-AAC, but both are significantly less than the MMC. Taking a simple case where there is no restriction on the power factor angle, the highest value of normalized stack energy deviation of the EO-AAC is $0.895 \frac{\|S\|}{3\omega}$ (this assumed the ac-to-dc voltage ratio defined in (10) and triangular triplen harmonic voltage injection of $k_3 = 0.5$), with $\|S\|$ being the apparent power magnitude. Using this value in (16) with $\Delta V = 0.1$ leads to a stored energy specification for the SM capacitance across all six stacks of 14.25 kJ/MVA.

The SM capacitive energy storage of the EO-AAC is greater than the SO-AAC (10.25 kJ/MVA), but it is important to note that the absence of ripples (six-pulse or otherwise) in the dc current has obviated filtering on the dc side. It was estimated in [7] that a dc-bus capacitance equivalent to two additional stacks worth of SM capacitors would be needed with the SO-AAC. Thus, it can be said that the EO-AAC requires an equivalent volume of capacitance to the SO-AAC with its dc-bus capacitance included, thus conserving the compact design, which was one of the attractive characteristics of the SO-AAC.

F. Inductive Elements

The stacks of SMs act like voltage sources because of the ability to switch charged capacitors in and out of the conduction path. It is the action of these imposed voltages over the inductors of the AAC, or MMC, that facilitates control of the currents and the size of the inductances plays an important role in control of current flow, e.g., the arm inductors in the MMC [8]. Furthermore, the number of inductors needed is no greater than the number of independent currents in the circuit. The EO-AAC

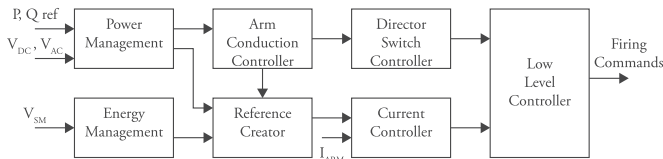


Fig. 6. Block diagram of the control architecture.

only has four arms in conduction at any time. The two phases with only one arm in conduction have that arm directly in series with the ac-side phase reactor. The phase in the overlap mode can have its dc-side current regulated by dc-side inductors. Since the ac transformer already provides the phase reactor through its leakage inductance, that leaves the EO-AAC only requiring two dc inductors for current control purposes, and these only need to be specified for current control purposes since fault ride-through capability is present. Therefore, the dc-side inductors can be small (e.g., ≤ 0.1 p.u.). A reduction in the number of explicit inductors from six in the MMC to two in the EO-AAC, in addition to the small total capacitive energy storage as explained in Section II-E, could represent a significant space saving if these are all air-cored inductors with large clearance distances from other structures.

G. Control Systems

A complex converter topology such as the EO-AAC requires the support of an extensive control system to ensure proper operation, as detailed in Sections II-B–II-D. The general architecture of the EO-AAC controller is illustrated in Fig. 6. The extensive nature of this controller would require a paper on its own, but a summary of its architecture is explained below to give a better context to the operation of the EO-AAC, especially for the experimental results presented in Section III.

Starting with the measurement of the ac and dc voltages, the “Power Management” synchronizes the converter to the grids and translates the P-Q demands into ac and dc current references. The “Energy Management” monitors the capacitors voltages of the SMs within the converter and computes appropriate actions in terms of internal voltage and current adjustments in order to keep the energy level within the stacks close to their nominal value. Its operation is closely related to the one of the MMC [44], [45] and SO-AAC [34]. The “Arm Conduction Controller” determines which four of the six arms of the EO-AAC are conducting, in synchronization with the ac phase angle. Knowing which arms are in conduction also allows the “DS Controller” to determine the conduction state of the DS, especially the ideal timing to ensure their soft switching. Using all the above information, the “Reference Creator” [46] computes the current waveforms, which should be flowing through each arm at each controller time step, using a state-space-model-based feedforward supplemented by proportional gains computed through the linear-quadratic regulator method. The “Current Controller” compares these reference waveforms with the measured arm currents and computes the optimal stack voltage, similarly to the method described in [47] and [48]. Finally, the “Low-Level Controller”

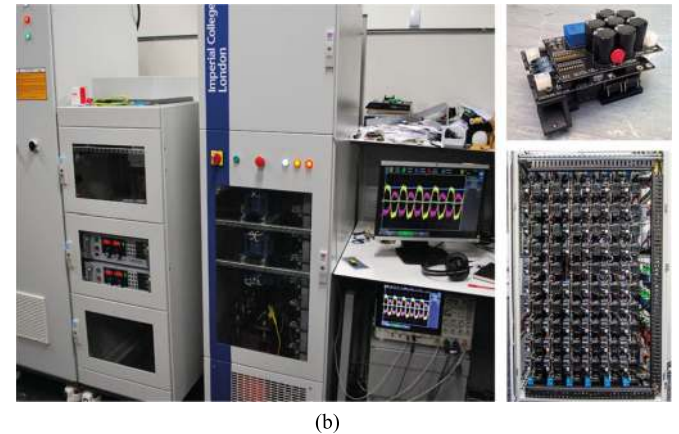
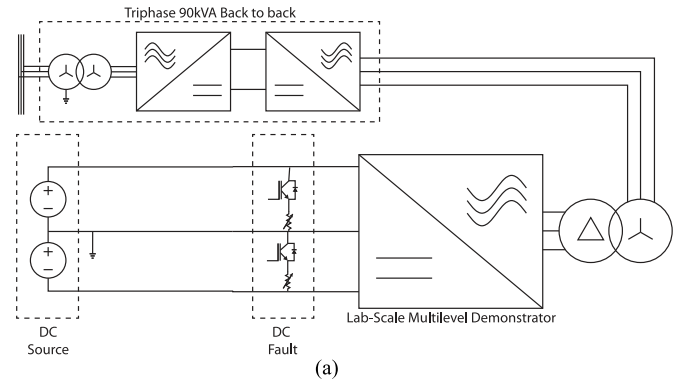


Fig. 7. Experimental rig used in this study. (a) Electrical schematic of the experimental rig. (b) Converter in its cabinet (left), one full-bridge SM (top-right), and the six stacks of series-connected SMs with the DS at the bottom (bottom-right).

converts the stack voltage commands into individual SM firing commands, taking into account the state of their respective DS and voltage deviations between the individual SMs using sorting algorithms similar to [49] and [50].

III. EXPERIMENTAL VALIDATION

A. Experimental Setup

The experimental EO-AAC is a 12-kVA ± 600 -V dc converter with ten SMs per stack. It was first presented in its prototype form in [51] and upgraded for [52]. The converter is controlled through an OPAL-RT real-time computing system running with a sampling frequency of 10 kHz. The converter is connected to a dc bus consisting of a unidirectional dc power supply, a load bank, and a dc-side fault emulator in the form of a low-resistance switched across the two dc poles, as shown in Fig. 7. The ac voltage is generated by Triphase inverters, which allows the emulation of different grid conditions. Table I lists all the parameters of the experimental setup. The IGBTs in the SMs are, however, switching at a higher frequency than the grid frequency due the fact that there are only ten SMs per arm, as opposed to hundreds in an actual HVDC converter. In all the following figures showing experimental data, the following variables have been measured directly using an oscilloscope with high-frequency bandwidth in order to capture most of the

TABLE I
CHARACTERISTICS OF THE EO-AAC EXPERIMENT

Characteristic	Symbol	Value
Power rating	$ S $	12 kVA
DC-bus voltage	V_{DC}	± 600 V
AC line voltage (RMS)	V_{line}	846 V
Nominal SM voltage	V_{SM}	90 V
Number of SMs per stack	N_{SM}	10
SM capacitor	C_{SM}	1000 μ F
Phase reactor	L	24 mH
Arm inductor	L_{Arm}	1.3 mH
DC inductor	L_{DC}	23 mH
DC fault resistor	R_{fault}	4.7 Ω
Control sampling frequency	$F_S = \frac{1}{T_S}$	10 kHz

fast transients: the arm currents, dc currents, and stack voltages. All the other variables (ac currents, ac voltage, and SM voltages) are recorded by the OPAL-RT system running at the sampling frequency of the controller, the architecture of which is detailed in Section II-G.

The dc fault apparatus consists of IGBTs in series with a low-impedance resistors (4.7 Ω) connected across the dc terminals. The firing signals for the IGBTs are generated independently of the converter control system. This implementation was motivated to ensure that the controller has no prior knowledge to the inception and clearance of a fault. During the initial instance of the fault, the controller has to cope with the fault conditions by itself before the fault detection algorithm establishes the nature of the fault and applies the predetermined fault response. The detection of the presence or removal of a dc-side fault is based on hysteresis threshold crossing by the dc-bus voltage. A fall of the dc-bus voltage magnitude below 60% of its nominal magnitude triggers the fault response by the converter, which consists, in this experiment, of moving into the STATCOM mode where the active power is dropped to zero and a constant capacitive power at 0.3 p.u. is provided to the grid. During this period, the dc power supply, which is used to provide power to the dc bus in the test rig, remains in the current limit mode set at 12 A. This results in a retained dc voltage of around 120 V (i.e., 0.1 p.u.). When the fault resistance is disconnected, the dc power supply starts recharging the dc bus. After the dc-bus voltage magnitude has remained above 80% for at least one full cycle, the controller considers that the fault is cleared and moves back into the recovery mode by ramping the power back up (at a rate of 10 p.u./s) up to its pre-fault set point. In a real system, it would be feasible for the AAC to recharge the network capacitance, if required, as shown in [52].

Sections III-B–III-C present the results from three tests, which illustrate and verify the material presented in Section II. Further experimental results from the EO-AAC were presented in [52] such as power reversal and both symmetrical and asymmetrical ac faults.

B. Normal Operation

The EO-AAC experimental rig generates the electrical waveforms as described in Section II when operated under normal conditions. Fig. 8 shows the experimental EO-AAC operating

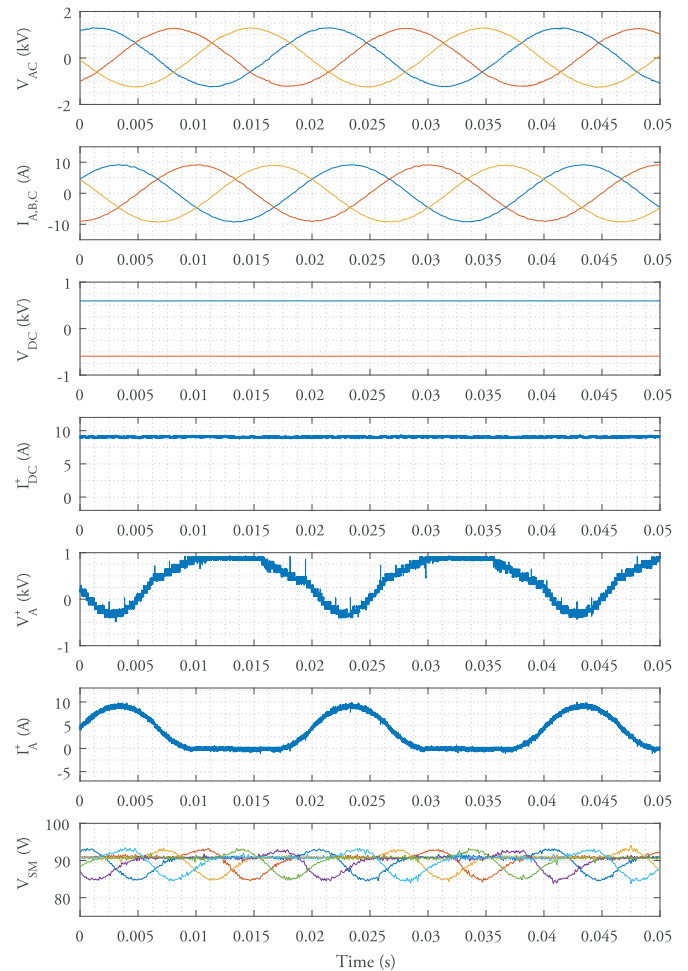


Fig. 8. Experimental results from the hardware converter operating at a set point of 1 p.u. P and 0 p.u. Q. Top-bottom: converter ac line voltages, converter phase currents, dc pole-to-ground voltages, dc current, phase A upper arm stack voltage, phase A upper arm current, and average SM voltage in each stack of SM.

under steady-state power flow of $P = 1$ p.u. (12 kW) inverting and no capacitive power. The electrical waveforms are as described in Section II in that the ac and dc current waveforms (second and fourth plots) are smooth (apart from some switching noise evident). Operation is close to $V_{AC} = \frac{2}{3} V_{DC}$ [the optimal point defined in (10)], and the arm currents (sixth plot) show the absence of discontinuities at the conduction state transitions, as discussed in Section II-C. The stack voltages (fifth plot) show the smaller rate of voltage rise during the overlap periods and the heightened voltage peak in the middle of the conducting states expected from triplen harmonic voltage injection.

C. DC-Side Fault

The EO-AAC retains the property of the SO-AAC of being able to fully control the arm currents even in the presence of a dc-side short-circuit fault to the extent that it can operate as a STATCOM [34], [38], [39]. Fig. 9 shows the main converter waveforms with a short-circuit applied to the dc side at 0.10 s and released at 0.35 s. At the instance of the fault, the controller maintains the currents close to their references despite

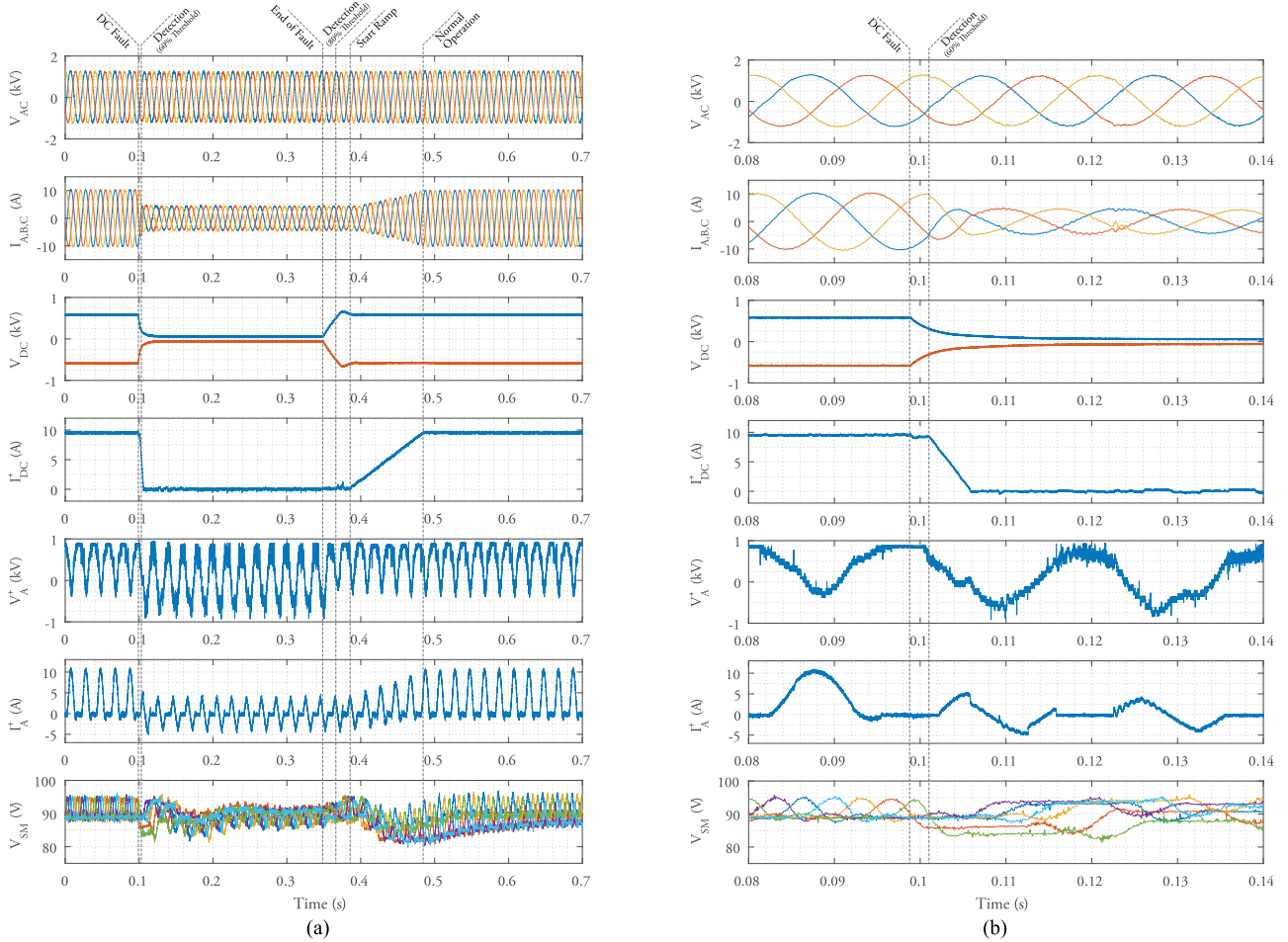


Fig. 9. Experimental results showing the dc-side fault-blocking and STATCOM capabilities of the EO-AAC, followed by the restoration of the dc-bus voltage by the converter and back to normal operation. The format is the same as in Fig. 8. (a) Global view of the event. (b) Zoom-in version.

the change in operating condition. After the fault detection declares the presence of the dc-side fault, the controller moves to a STATCOM operation by setting the real power reference to zero and a 0.3-p.u. capacitive reactive power reference. Subplots 2, 4, 6, and 7 from the top of Fig. 9 demonstrate that the arm, phase, and dc currents and SM voltages exhibit only minor deviations from their reference waveforms through the fault inception and clearance. There is a small amount of retained voltage (about 120 V) when the dc fault is active due to the dc power supply in the current-limiting mode at around 12 A still connected to the dc bus. This retained dc voltage does not impact the capability of the converter to maintain current control, as in the case of a 0-V dc-bus voltage. When the fault is cleared, the dc-bus voltage can rise under the control of the dc power supply. Once the detection algorithm concludes that the fault is cleared (i.e., dc-bus voltage above 80% nominal value for at least one full cycle), the converter resumes normal operation by transitioning through a power ramp of at a rate of 10 p.u./s.

D. AC Voltage Magnitude Variation

In order to demonstrate the ability of the EO-AAC to operate across a wider range of ac/dc voltage ratios (in other words,

freedom from the restrictions of the SO-AAC sweet spot), the experimental converter was subjected to steps in the ac voltage magnitude, generated by the triphase inverters. Each column in Fig. 10 shows a different ac voltage magnitude, with one operating point below the optimal voltage ratio and one above. The EO-AAC is seen to adapt and operates stably in each case. When operated away from the optimal point (10), the arm current waveforms (but not the phase currents) start to show discontinuities when the arms move from one conduction state to another, similar to Fig. 3. The amplitude of these discontinuities can be predicted in relation to the nominal dc current magnitude, as stated in (17), by noting the variation of the ac voltage magnitude around its optimal point (10) by the factor k_{AC} and the per unit amount of power k_S going through the converter

$$\begin{cases} \Delta I &= \frac{I_A^+(\frac{\pi}{6}^+) - I_A^+(\frac{\pi}{6}^-)}{I_{DC}^{Nom}} \\ &= k_S \left(1 - \frac{1}{k_{AC}}\right) \cos(\Phi_{AC}). \end{cases} \quad (17)$$

However, the magnitude of these discontinuities remains small, especially compared to those observed in the SO-AAC. The discontinuities are approximately 18% of the dc current magnitude in the case of an ac voltage magnitude of 0.85 p.u. and unity power factor. As noted in Section II-C and demon-

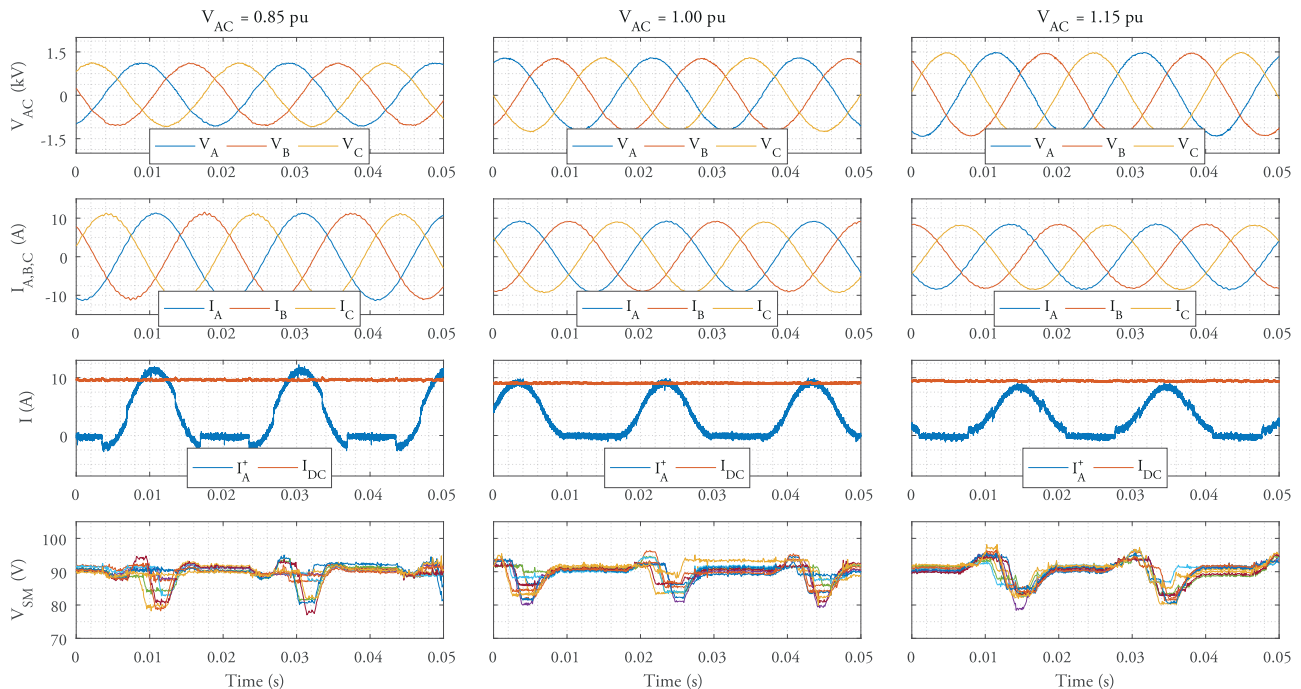


Fig. 10. Experimental results of the EO-AAC operation under a wide range ($\pm 15\%$) of ac voltage magnitude variations.

strated in (17), operation at unity power factor corresponds to the worst-case scenario, and the generation of reactive power reduces the magnitude of these arm current discontinuities.

Finally, the voltage rating of the stacks in the EO-AAC has a small dependence to the ac voltage magnitude variation. This is proven by (18) resulting from (14) with $k_3 = 0.5$, where k_{AC} measures the ac voltage magnitude's relative variation to its nominal value (10). This results in a voltage rating increase of the stacks of SMs by $\pm 2.5\%$ for an ac voltage magnitude variation of $\pm 15\%$

$$\begin{cases} \hat{V}_{AC} &= k_{AC} \frac{2}{3} V_{DC} \\ \hat{V}_{Stack} &= \frac{V_{DC}}{2} \left(\frac{1}{2} - \frac{k_{AC}}{6} \right). \end{cases} \quad (18)$$

IV. DISCUSSION

The EO-AAC should be compared against its predecessor, the SO-AAC [34], and the incumbent technology, the MMC [4]. The HB-MMC is normally the preferred format because of its low power losses, but the comparison here will also include the H-MMC because it has dc fault ride-through capability that makes it a competitor to the AAC. Here, the H-MMC is taken to have the same number of SMs as the HB-MMC but with half of them replaced by full-bridge SMs [16]. This format of the H-MMC only allows undermodulation (i.e., $\hat{V}_{AC} \leq \frac{1}{2} V_{DC}$) but does allow continued current control with a short-circuited dc link. Note that the SO- and EO-AAC are both configured to overmodulate and have higher nominal ac voltages than the MMC of the same dc voltage, as defined by the sweet spot and the optimal operating point (10), respectively.

These four converter types are compared in Table II when configured as a ± 525 -kV, 1.5-GW converter. The SMs have

been rated at 1.8 kV in order to use the 3.3–1.5-kA IGBT module (Infineon FZ1500R33HL3) at a voltage derating factor of 60% when allowing the SM voltage to fluctuate by $\pm 10\%$. For the DS, 4.5–1.5-kA Press-Pack injection-enhanced gate transistors (IEGTs) (Toshiba ST1500GXH24) are used because of their tendency to fail short circuit, a desired behavior for series-connected power devices. Applying the same derating factor (and ignoring the SM voltage deviation margin) leads to a voltage rating of 2.7 kV per IEGT. The SM capacitors were sized as described in Section II-E. The arm inductors in the HB-MMC were sized at 0.1 p.u. to limit the rate of rise of the current in the case of a dc-side fault, as detailed in [8]. In the case of the H-MMC, this current-limiting criterion no longer applies; thus, the arm inductors have been reduced to 0.02 p.u. to achieve a good balance between control margins and inductor size, also in line with other works related to the H-MMC found in the literature [8], [16], [17]. Power losses in the semiconductors were assessed by running a time-domain simulation in Simulink and, then, calculating the voltage drops across all the IGBTs, IEGTs, and internal diodes using polynomial approximations to the datasheet curves for the conduction losses and switching power losses added at each event, following the procedure detailed in [53] and [54] and also used in [16].

The total number of SMs in the AAC is less than the MMC because the SM stacks need only to generate a lower peak voltage, while the arm is conducting, with the DS supporting the additional voltage when the arm is not conducting. Overall, the number of semiconductor devices in the EO-AAC is about 8% higher than the SO-AAC, 4% higher than the H-MMC also, and 55% higher than the HB-MMC. This has implications for cost, but for size and power losses, there are other important factors to consider. Each AAC SM uses a smaller capacitor than the

TABLE II
MODULAR CONVERTER CHARACTERISTICS

Technology	MMC		AAC	
	HB-MMC	H-MMC	SO-AAC	EO-AAC
Topology				
DC-side fault tolerant	No	Yes	Yes	Yes
Power rating	1.5 GW ± 525 kW			
DC-bus voltage				
AC line voltage	617 kV	617 kV	819 kV	857 kV
Nominal voltages	SM: 1.8 kV—DS IEGT: 2.7 kV			
Number of half-bridge SM per stack	584	292	0	0
Number of full-bridge SM per stack	0	292	372	389
Total number of SM	3504	3504	2232	2334
Number of series-IEGT per DS	0	0	195	260
Total number of IGBT modules	7008	10 512	8928	9336
Total number of IEGT modules	N/A	N/A	1170	1560
SM capacitors	9.35 mF	9.35 mF	4.25 mF	5.65 mF
DC-bus capacitor	N/A	N/A	12 μ F (= 6.6 MJ)	N/A
Total capacitive energy stored	53 MJ	53 MJ	22 MJ	21 MJ
Arm inductors	6 \times 142 mH (0.1 p.u.)	6 \times 28 mH (0.02 p.u.)	6 \times 23 mH (0.02 p.u.)	(stray inductance only of 6 \times 1 mH)
DC inductors	(DC Circuit Breaker \approx 400 mH)	None	2 \times 115 mH (0.1 p.u.)	2 \times 25 mH (0.02 p.u.)
Total power losses from the semiconductor devices	Inverting only (PF=1)	0.433%	0.608%	0.532%
$P_{Base} = 1.575$ GW	Rectifying only (PF=1)	0.405%	0.592%	0.558%
	Inverting capacitive (PF=0.95)	0.464%	0.639%	0.543%
	Rectifying capacitive (PF=0.95)	0.428%	0.624%	0.574%
	Inverting inductive (PF=0.95)	0.463%	0.640%	0.578%
	Rectifying inductive (PF=0.95)	0.437%	0.635%	0.598%

MMC SM (approximately half) and the AAC uses fewer SMs (approximately two-thirds), so the stored capacitive energy and physical volume they occupy is smaller. The EO-AAC has the lowest number of explicit inductors (two) because it can use the leakage of the interface transformer and does not require arm inductors. The total size of the inductors is influenced by their number as well as stored energy because of clearance and shielding issues. The HB-MMC, being the only converter of the four unable to control arm currents during a dc-side short circuit, would need significant inductance somewhere (in the arms or dc link) to limit the rise of fault currents. The SO-AAC is the only one of the four to not provide inherently smooth dc current and, therefore, must include a large capacitance on the dc link.

The power efficiency results for six operating points are shown at the bottom of Table II. As expected, the H-MMC has higher losses than the HB-MMC because it has more semiconductor devices in the conduction paths for the same pattern of currents. The SO- and EO-AAC have broadly similar numbers of IGBTs overall, but they are put to different use. Nonetheless, the losses in the EO-AAC are similar and a little bit less than the H-MMC (by about -9%). It is important to note that these losses are for only the semiconductor devices, and other substantial losses in the transformer, inductors, and the cooling system need to be considered in a complete converter station [55].

In summary, all the dc fault ride-through converters here suffer a power loss penalty compared to the HB-MMC. The EO-AAC has solved the two major drawbacks of the SO-AAC: it is not tied to a sweet spot, and it does not need a dc-side filtering capacitor (a significant volume saving). The EO-AAC and

H-MMC are similar in terms of controllability in normal and abnormal conditions, and in terms of power loss. The EO-AAC requires approximately half the volume of SM capacitance and two rather than six explicit inductors, contributing to a more compact design of the converter station.

V. CONCLUSION

The EO-AAC is an improved version of the previously proposed AAC which was operated with a short overlap (SO-AAC). Some of the advantages of the EO-AAC stem from its operating mode, but there are also some from consequential changes in the circuit itself such as the removal of the dc-side filtering capacitor and reduction in the number of inductors. The new mode of operation employs an overlap of 60° in the conduction of top and bottom arms, whereas, previously, the SO-AAC used an overlap of about 10° as an opportunity to circulate a balancing current between the arms and the dc link. The new operating mode ensures that there is always a path to circulate current between the dc side and the converter independent of the ac-side currents. It also means that the ac currents sum to zero within the converter phase that is in overlap and do not flow via the dc link. The EO-AAC has been shown to have these benefits over the SO-AAC: 1) smooth dc current waveform thus removing the need for a bulky low-frequency dc filtering capacitor, compensated by a small increase in the total capacitive energy storage in the SM but remains smaller than that of the MMC, 2) release from the sweet-spot operating area for energy balancing reasons, thus allowing the EO-AAC to operate at any ac-to-dc voltage ratio. It has also been shown that an optimal

operating point exists at $\hat{V}_{AC} = \frac{2}{3}V_{DC}$, where there are no discontinuities in the arm current waveforms between the different conduction periods leading to a further benefit, which is 3) the easing of the current control task and soft switching of the DSs.

The EO-AAC retains the benefits of the original SO-AAC, namely 4) dc fault ride-through capability (and a subsidiary benefit of not needing to size inductors for fault current limiting), 5) STATCOM mode of operation during a dc-bus outage for additional ac-grid support, 6) the relatively small capacitive energy storage requirement (14.25 kJ/MVA), and 7) reduced number of inductors (two dc-side inductors as opposed to six-arm inductors). The EO-AAC requires more semiconductor devices than the SO-AAC (+8%) and H-MMC (+4%), but this increase has been mitigated by the use of a triangular triplen harmonic voltage injection technique. Comparing these three converter topologies (which are all capable of dc fault ride-through), the power losses in the semiconductors are broadly similar at approximately 0.6% and above the HB-MMC at 0.43%.

A comparison between the HB-MMC and EO-AAC technologies has identified two key facts. On the one hand, from a purely electrical point of view, the dc-side fault-blocking capability comes at a premium of more semiconductor devices (+55%) and higher semiconductor power losses (+30%). On the other hand, from a converter station design point of view, the AAC technology reduces the bulk of several items: fewer submodules (−33%), smaller submodule capacitors (−50%), and fewer inductors (two instead of six) when compared to the MMC. All these facts combined mean that the premium usually associated with the dc-fault blocking capability of a VSC could now be offset by the smaller footprint of the converter station, thanks to the EO-AAC technology.

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Authors' photographs and biographies not available at the time of publication.