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BRIEF REPORT AND COMMENT

This section is intended for the publication of (1) brief reports which do not require the formal structure of regular journal articles, and (2) comments on items previously published in the journal.

The fabrication of metal–oxide–semiconductor transistors using cerium dioxide as a gate oxide material

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Cerium dioxide was employed as a gate insulator for an enhancement-type *n*-channel metal–oxide–semiconductor (MOS) transistor. Cerium was evaporated in a tungsten boat and immediately oxidized for oxide uniformity. The use of CeO_2 as a gate oxide in MOS transistor yielded a low positive threshold voltage with negligible interface charge effects. This resulted in the transistor performing as an enhancement type device.

I. INTRODUCTION

Research in various elemental compounds as insulating oxides has led to their potential use in thin film devices and has marked possibilities in very large scale integrated (VLSI) material technology.[1,2] Quality thin film insulating materials are an important factor in the design and operation of monolithic and hybrid devices. They enable device size reduction and their intrinsic dielectric properties can be used to obtain the required characteristics in various microelectronic devices. Thin films of cerium dioxide (CeO_2), a rare earth oxide, have received attention in the recent years due the high dielectric constant and the potential use of these films in thin film devices. Cerium dioxide exhibits a strong dielectric breakdown field with values on the order of 10^7 V/cm. Information regarding the electrical and optical properties of CeO_2 available in the literature[3,4] has had influence on its possible use in metal–oxide–semiconductor (MOS) devices. In metal–oxide–semiconductor devices, the oxide affects parameters such as the threshold voltage (V_T) and the small signal transconductance (g_m). For devices using thin film oxides in the range 0.02–0.2 μm, it becomes necessary to realize the differences that stem from the use of different types of oxides.

The threshold voltage V_T of a MOS transistor is dependent on the type of gate oxide material used. Certain applications require not only a low value of V_T, but also a precisely controlled value to match to other devices in the circuit. Use of oxides such as Si_3N_4 and SiO_2 in devices have been reported.[5] Si_3N_4 has a relative dielectric constant of approximately 7 compared to 3.9 of SiO_2. Studies on CeO_2 show that it has a relative dielectric constant of 4.2 at room temperature, which is slightly higher than SiO_2. With higher relative dielectric constant materials the gate capacitance can be increased thereby reducing V_T. Even though Si_3N_4 has a high dielectric constant, it has the disadvantage of contributing charges at the oxide–nitride layer which affect V_T directly. This charge formation is what causes most SiO_2 MOS *n*-channel enhancement devices to operate in a depletion mode. In the devices fabricated here, CeO_2 is deposited on the Si substrate and there is no ionic formation due to SiO_2 growth.

The application of CeO_2 in Al–CeO_2–Si enhancement-type *n*-channel structures is investigated here. The fabrication techniques employed are filament evaporation and deposition of cerium metal (Ce) and subsequent oxidation to get CeO_2 as the gate oxide. The quality of this oxide is analyzed and directly related to the study of how it will influence the device characteristics and operation. In this paper, the

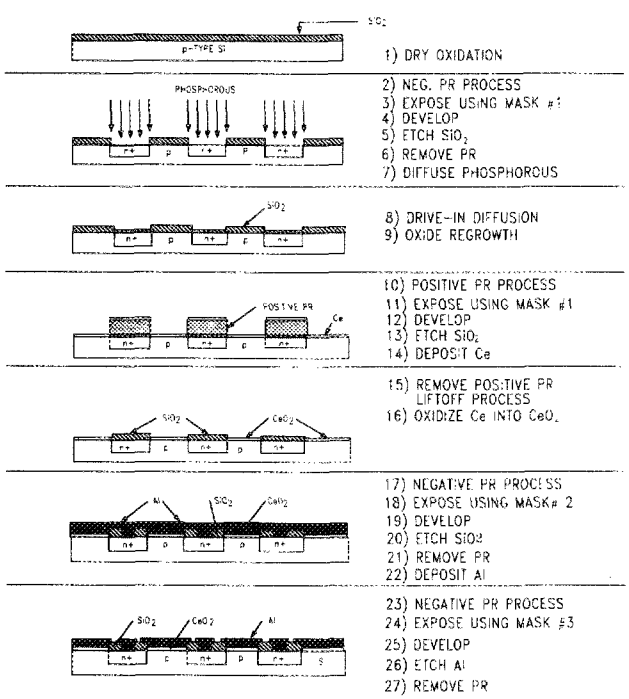

FIG. 1. Fabrication sequence for the MOS transistor.

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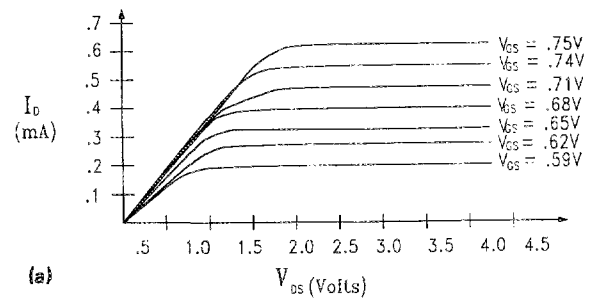


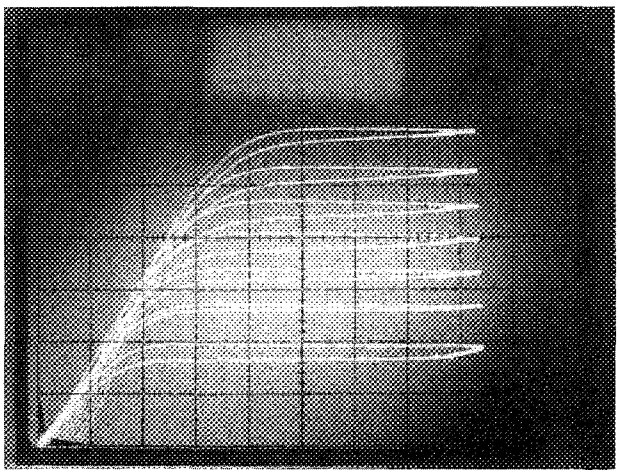
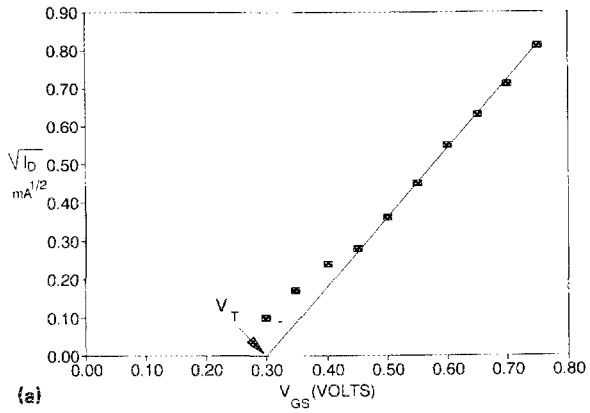


FIG. 2. (a) Plot of I_D vs V_{DS}. (b) Photograph of the I_D vs V_{DS} curve.



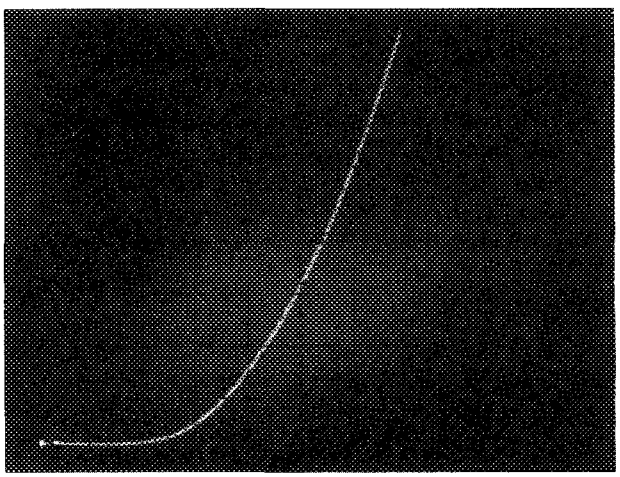


FIG. 3. (a) Plot of $I_D^{1/2}$ vs V_{GS}. (b) Photograph of I_D vs V_{GS}.

effect of CeO_2 on the MOS threshold voltage and the gate capacitance are reported.

II. EXPERIMENTAL

The device was fabricated on a 2 in. *p*-type Si wafer with a ⟨100⟩ orientation and a resistivity between 8–15 Ω cm. The substrate was cleaned with trichloroethylene, acetone, methanol and deionized water with a resistivity of 17.7 MΩ cm. The wafer was then placed in sulfuric peroxide cleaner following a "hot etch" ($6NH_4F$:1HF). After proper masking sequences, the source and drain regions were opened for the predeposition of phosphorous. Solid solubility concentration was achieved in a diffusion furnace at 900 °C for 20 min. This was followed by a drive-in step, a dry–wet–dry oxidation sequence, each of 10 min duration, at 1100 °C. The carrier gas for dry oxidation was oxygen and nitrogen was used for the wet oxidation. A second masking sequence for the gate region was performed, wherein the area over which CeO_2 was to be deposited was etched thoroughly of SiO_2 in a hot etch solution. Ce was then deposited by filament evaporation using a tungsten boat in a cryogenic pump vacuum system. Approximately 70 mg of Ce was evaporated on the wafer in a vacuum of 1×10^{-5} Torr. Several thickness measurements were made over the 2 in. diam Si wafer using an optical interferometer. The measurements resulted in thickness variations of $\pm$ 100 Å. The wafer was placed at a distance of 20 cm from the filament evaporator using a glass chimney. Ce deposited on areas other than the gate region was removed by a lift-off process. The wafer was then placed in a dry oxidation furnace and the complete oxidation of the cerium film was achieved in 10 min at 400 °C with a constant flow of O_2. The oxidation uniformity was excellent, as indicated by optical measurements done on these films. A third masking step was performed on the source and drain for the opening of the contact windows. Aluminum was then deposited by thermal evaporation in the cyro pumped vacuum system. The fourth masking step was done to define the contacts, where Al was etched in a solution of phosphoric acid and deionized water (one part phosphoric to three parts deionized water) and heated to about 90 °C. The Al etchant does not attack CeO_2 as it can be etched only by buffered hydrofluoric acid. Figure 1 outlines the fabrication process employed.

III. RESULTS

The CeO_2 *n*-type enhancement MOS transistors were fabricated with a gate oxide thickness of 0.16 μm on a silicon substrate with a ⟨100⟩ orientation. The gate width was 200 μm.

A HP177 curve tracer was used to measure the characteristics of the devices. Figure 2(a) shows typical characteristic curves. These curves were redrawn, for clarity, from the photographs shown in Fig. 2(b) taken from the curve tracer. Figure 3(a) shows the square root of the drain current versus the gate voltage redrawn from photographs shown in Fig. 3(b). The threshold voltage determined from this graph shows a value of approximately 0.3 V. This value is representative of a number of samples measured on a typical 2 cm × 2 cm Si substrate. A MOS device with a SiO_2 gate of thickness

0.16 μm grown on a ⟨100⟩ substrate orientation has a threshold voltage of approximately -2.4 V. Such a large negative threshold voltage can only be attributed to sodium contamination introduced during the fabrication of the device. Both the CeO_2 and SiO_2 gate devices were fabricated under the same processing conditions, but the effect of oxide charges was less dramatic in CeO_2 than in SiO_2. The interface charges for both the CeO_2 and the SiO_2 gate MOS devices were calculated using the measured threshold voltages. The SiO_2 gate MOS device yielded an interface charge of 3.8×10^{11} q C/cm^2 with $V_T = -2.4$V. With the CeO_2 gate, the interface charge was 1.5×10^{10} q C/cm^2 with $V_T = 0.3$V. For the SiO_2 gate the device is on for zero gate voltage. The normally on effect in the n-type enhancement device using SiO_2 is a problem that is dealt with by special fabrication methods. Ion implantation is usually required to adjust the threshold voltage to positive values. CeO_2 does not present this problem and hence does not require an additional processing step for charge reduction.

The transconductance of the device biased at 0.4 mA is approximately 2 mA/V as obtained from the I_D versus V_{GS} curve. This is typical of most MOS devices.

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