

The Four-Gate Transistor

S. Cristoloveanu,¹ B. Blalock,² F. Allibert,^{1,5} B. Dufrene,³ M. Mojarradi⁴

¹Institute of Microelectronics, Electromagnetism, and Photonics (UMR CNRS, INPG, UJF)
ENSERG, BP 257, 23 rue des Martyrs, F38016 Grenoble Cedex 1, France

²Department of Electrical and Computer Engineering
The University of Tennessee, Knoxville, TN 37996-2100, USA

³Department of Electrical and Computer Engineering
Mississippi State University, Mississippi State, MS, USA

⁴Jet Propulsion Laboratory; Pasadena, CA; USA

⁵SOITEC S.A., Chemin des Franques, Bernin, 38926 Crolles, France

Abstract

The four-gate transistor or G^4 -FET combines MOSFET and JFET principles in a single SOI device. Experimental results reveal that each gate can modulate the drain current. Numerical simulations are presented to clarify the mechanisms of operation. The new device shows enhanced functionality, due to the combinatorial action of the four gates, and opens rather revolutionary applications.

1. Introduction

MOS transistors with two gates are attractive in terms of improved performance and extended scalability [1,2]. Multiple-gate MOSFETs can also be useful for signal mixing and more complex (non-binary) logic functions. The innovative 4-gate transistor (G^4 -FET) presented in this paper has the *maximum* number of gates which can be achieved. The body of the device (Fig. 1) is surrounded by a top MOS gate (V_{PG}), a bottom substrate gate (V_{SUB}), and two side junction gates ($V_{JG1,2}$). Section 2 shows that the architecture and processing of the 4-gate transistor takes advantage of the isolation capabilities of the SOI technology. Experimental data are described in section 3 and explained in section 4 using detailed numerical simulations.

2. Device description

An n-channel G^4 -FET is formed from a normal partially-depleted SOI MOSFET with p-channel. The N-type body is provided with two independent N^+ body contacts, on each side of the channel, which act as source

and drain (Fig. 1). The former source and drain of the original p-channel MOSFET are P^+ doped and play the role of *lateral junction gates*. These gates control the channel cross-section. With the possibility to bias the substrate as a *back gate* and the poly-Si as a *top gate*, the new device is indeed a four-gate transistor with narrow channel and accumulation-mode operation.

It is worth noting the differences between the G^4 -FET and the original MOSFET. In a G^4 -FET, the drain current is composed of majority carriers and flows in a direction perpendicular to that in the original inversion-mode MOSFET. The gate length of the MOSFET defines the channel width W of the G^4 -FET and vice-versa.

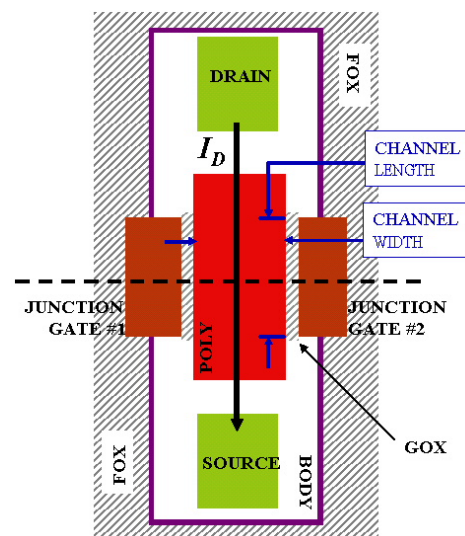


Figure 1. Top view of the G^4 -FET structure.

The G^4 -FET does not require any special processing and is naturally adapted to CMOS technology scaling. Device control will increase as the two junction-gates come closer to one another.

3. Electrical characteristics

The device presented in this paper is n-channel with a $1.5\mu\text{m}$ length and a $0.35\mu\text{m}$ width. It has been fabricated on commercially available thick film (partially depleted) SOI wafers. Complementary p-channel G^4 -FET have identical configuration and reciprocal doping regions.

The fabricated devices are fully operational and robust. For simplicity, the junction-gates have been tied together during the measurements. Due to the presence of four gates, several operating modes are possible, depending on the front poly-Si gate voltage (V_{PG}), the junction-gates voltage (V_{JG}) and the substrate voltage (V_{SUB}). Figure 2 shows drain current $I_D(V_D)$ characteristics which exhibit the three typical regions of operation: linear, triode and saturation. The drain current is clearly modulated by both V_{PG} and V_{JG} . High levels of current are reached for strong accumulation at the front interface ($V_{PG} > 0$) and low reverse biasing of the junction gates (or $V_{JG} = 0$). Avalanche breakdown occurs beyond 15 volts and can be increased by design.

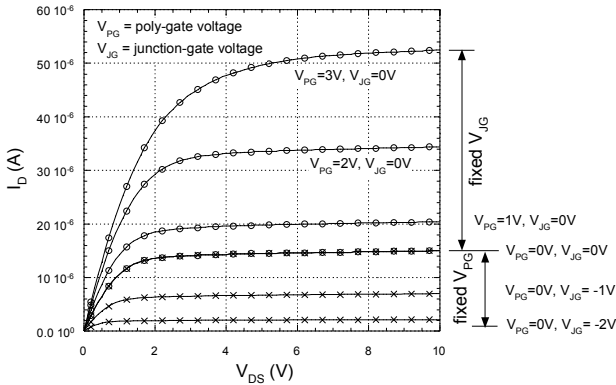


Figure 2. Measured $I_D(V_D)$ curves for $V_{SUB} = 0\text{ V}$.

Figure 3 shows the influence of V_{PG} on I_D vs. V_{JG} curves with the G^4 -FET operating in the linear region. A subthreshold region, where the current varies exponentially, being governed by the junction-gates, is visible. The junction-gates enable full control of the drain current, from off-state to on-state, as long as the channel is not too strongly accumulated. There is a trade-off between the maximum conductance and the minimum subthreshold swing of the G^4 -FET. As a matter of fact, the subthreshold slope improves for depletion at the front interface ($V_{PG} < 0$).

Therefore, the efficiency of the junction gates is increased not only in narrow channels but also when the top gate is biased in depletion. Their influence on the drain current is visible on the reciprocal curves I_D vs. V_{PG} of Figure 4. At large reverse bias V_{JG} , the current is

cut off for low negative values of V_{PG} . The top-gate threshold voltage is a strong function of V_{JG} . For lower V_{JG} , the current level is under control, but the device cannot be turned off. This is because the body of the transistor remains partially depleted, unless there is a lateral action from the junction gates.

The transconductance curves, g_m vs. V_{PG} or g_m vs. V_{JG} , are rather complex. The transconductance increases as the junction-gates become less depleted, allowing a wider conductive channel. Two distinct regions in g_m vs. V_{PG} curves are observed when the conduction mechanisms changes from depletion-controlled neutral-mode to accumulation-mode. Mobility degradation by surface scattering is observed in strong accumulation.

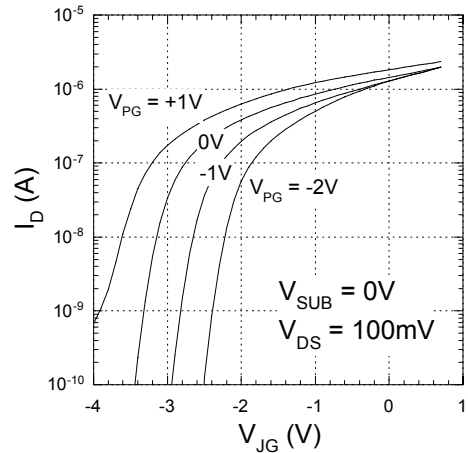


Figure 3. Measured I_D versus V_{JG} for various V_{PG} and $V_{SUB} = 0\text{ V}$.

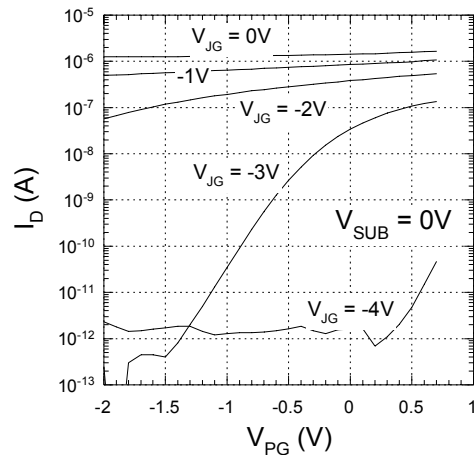


Figure 4. Measured I_D versus V_{PG} for various V_{JG} and $V_{SUB} = 0\text{ V}$.

The role of the back gate, accumulated and depleted, is shown in Figures 5 and 6, respectively. When the back interface is strongly accumulated (Fig. 5), the device cannot be completely turned off, even for large negative voltages on the top gate and junction gates. However, the junction gates and the top gate still provide a double

control of the current level. This mode of operation is interesting for applications requiring high currents.

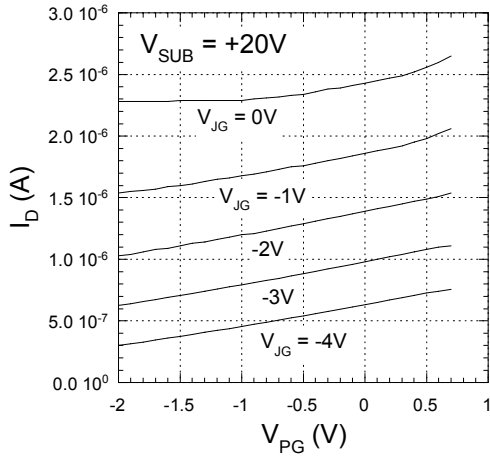


Figure 5. $I_D(V_{PG})$ for various V_{JG} at $V_D=100\text{mV}$ and $V_{SUB}=20\text{V}$.

On the other hand, when a negative voltage is applied on the substrate, the back interface becomes depleted (the channel thickness decreases) and the device can be turned off easily, even for moderate values of V_{PG} and V_{JG} . Figure 6 shows that the subthreshold swing improves rapidly as the front gate is also driven into depletion ($V_{PG} < 0\text{ V}$) and reaches excellent values (below 100mV/decade).

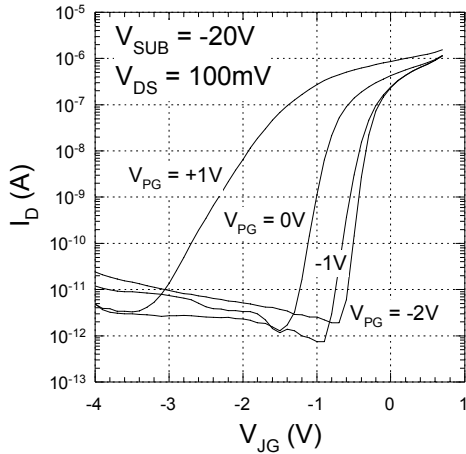


Figure 6. I_D versus V_{JG} for various V_{PG} at $V_D=100\text{mV}$ and $V_{SUB}=-20\text{V}$.

4. Simulations

Numerical simulations of the carrier distribution in the G^4 -FET were conducted using Silvaco Atlas. The device cross-section (Figs. 7 and 8) is the same as for a short n-channel MOSFET, except that the current flows perpendicular to the figure and the two lateral terminals are inter-connected and used as junction gates. These simulations are used to gain insight into the mechanisms controlling the conductive path (*i.e.* non-depleted region)

inside the body of the transistor. The results are only qualitatively representative of the actual device under test.

All simulated G^4 -FETs had a 5 nm thick gate-oxide, a 100 nm thick active silicon layer, and a 100 nm thick buried oxide. The lateral gates had a $2 \times 10^{20}\text{ cm}^{-3}$ P-type doping. The channel width (between the two lateral gates) was 0.3 μm and the transistor body received a $2 \times 10^{17}\text{ cm}^{-3}$ N-type doping.

The simulations show that the channel cross-section can be controlled to some extent by each gate. As far as the front gate is concerned, Figure 7-a shows the position of the depletion region for a V_{PG} voltage close to flat-band condition. The depletion regions (white zones on both sides of the channel) are only due to the junctions and their extension depends on V_{JG} bias. The conduction layer is neutral (non-depleted grey area), relatively wide, and covers the entire film thickness.

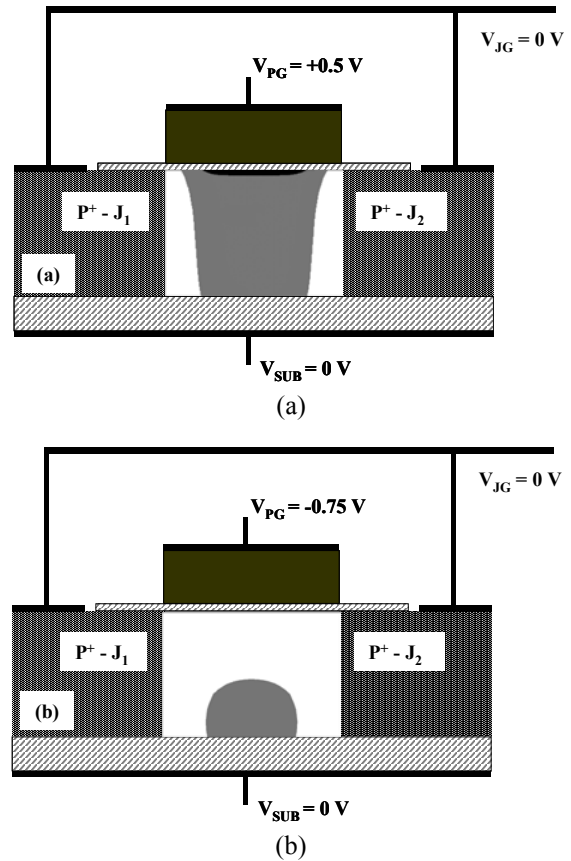


Figure 7. 2D simulation of the cross-section of the G^4 -FET with grounded junction-gates and substrate. Poly-gate voltage is either close to flat-band voltage (a) or at maximum depletion (b). Depleted regions are represented in white, non-depleted regions in grey, and accumulated regions in black.

When the top-gate bias is switched to a negative value corresponding to a maximum depth of the depletion region (onset of front-channel inversion, Figure 7-b), the conductive layer is shrunk and repelled towards the back

interface. The use of top-gate voltages between these values ($-0.75 < V_{PG} < +0.5$ V) enables the control of the thickness of the conductive path.

A symmetrical situation occurs for back-gate biasing. However, combined effects from top, bottom and side gates provide the ultimate control of the cross-section of the conductive path. When the back interface and junction-gates are depleted, the conducting path cannot cover the whole body of the transistor, even if the front gate is accumulated ($V_{PG} = +0.5$ V, Figure 8-a). In the opposite case (negative V_{PG}), the front interface is driven in depletion and the conductive path shrinks gradually. At some point, the path completely disappears ($V_{PG} = -0.75$ V, Figure 8-b), thus turning the device off.

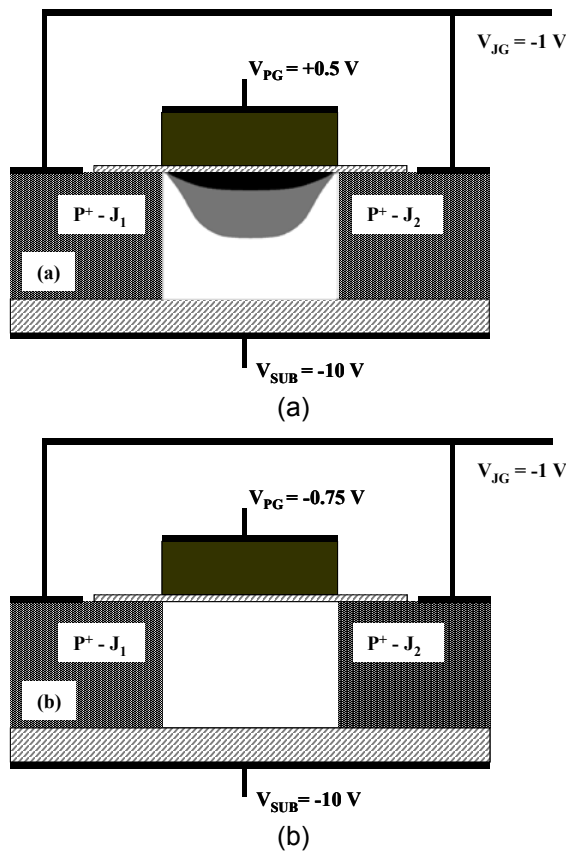


Figure 8. 2D simulation of the cross-section of the G⁴-FET with depleted junction-gates and back interface. Front interface is either in (a) accumulation or (b) depletion. Colors as in Figure 7.

Additional simulations confirm that the drain current is governed by two distinct mechanisms: near-surface variation of the carrier density in the channel (MOS effect at the front and back interface) and variation of the cross-section of the channel (by lateral JFET effect and vertical MOS depletion effect).

The latter aspect is most fascinating, because a tiny conductive path is nothing but a quantum wire. The size of such a G⁴-FETs wire can be electrically adjusted. Even more importantly, the wire can be moved across the body by tuning the four gates. In particular, placing the

conductive layer in the center of the body avoids surface roughness scattering and improves carrier mobility.

Note that in a partially-depleted SOI MOSFET, the association of front and back gate biases does not achieve full depletion. Only by adding the lateral junction effect and keeping the body narrow (short inter-junction separation) can the current be switched off in a G⁴-FET. It is the coupling of vertical and depletion regions that allows full depletion to occur, even before the two lateral depletion regions (in extremely narrow bodies) or the vertical depletion regions (in thinner or lower doped films) merge. A charge-sharing model, such as used for short-channel effects in MOSFETs, is therefore not suitable for the G⁴-FET because it is based on the superposition of 'perfectly' depleted regions. Our view is that 2-D coupling does much more: a depletion region activated by one gate allows the depletion regions controlled by the other gates to extend further.

5. Conclusion

We have proposed and described a unique four-gate transistor. The G⁴-FET takes advantage of the flexibility of SOI technology and combines MOS-like and JFET-like field-effects to control current flow. The G⁴-FET can be used to mix high and low gate voltages, achieve low noise and RF performance, emulate quantum wires with electrically controlled size, etc. Combinatorial manipulations of the 4 gates are expected to provide high-density digital logic per transistor. Although the preliminary experiments and simulations fully validate the device concept, more work is needed for exploring the G⁴-FET capabilities.

6. Acknowledgements

The work described in this paper was carried out for the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

7. References

- [1] S. Cristoloveanu, T. Ernst, D. Munteanu and T. Ouisse, "Ultimate MOSFETs on SOI: ultra-thin, single gate, double gate, or ground plane," *Int. J. of High Speed Electronics and Systems, WOFE'99*, vol. 10, no. 1, pp. 217-230, 2000.
- [2] F. Allibert, S. Cristoloveanu and A. Zaslavsky, Proc. ESSDERC'01, H. Ryssel, G. Wachutka, H. Grünbacher ed., Frontier group, 2001, pp.267-270.