Open access • Journal Article • DOI:10.1088/1748-0221/7/01/C01019

The GOTTHARD charge integrating readout detector: design and characterization

Aldo Mozzanica, Anna Bergamaschi, Roberto Dinapoli, H. Graafsma ...+7 more authors

Institutions: Paul Scherrer Institute

Published on: 01 Jan 2012 - Journal of Instrumentation (IOP Publishing)

Topics: Photon counting, High dynamic range, Application-specific integrated circuit, CMOS and Dynamic range

The GOTTHARD charge integrating readout detector: design and characterization

2012 JINST 7 C01019

(http://iopscience.iop.org/1748-0221/7/01/C01019)

PUBLISHED BY IOP PUBLISHING FOR SISSA

RECEIVED: *November 16, 2011*
ACCEPTED: *November 30, 2011*
PUBLISHED: *January 4, 2012*

13th INTERNATIONAL WORKSHOP ON RADIATION IMAGING DETECTORS,
3–7 JULY 2011,
ETH ZURICH, SWITZERLAND

The GOTTHARD charge integrating readout detector: design and characterization

A. Mozzanica,[a,1] **A. Bergamaschi,**[a] **R. Dinapoli,**[a] **H. Graafsma,**[b] **D. Greiffenberg,**[a] **B. Henrich,**[a] **I. Johnson,**[a] **M. Lohmann,**[b] **R. Valeria,**[a] **B. Schmitt**[a] **and S. Xintian**[a]

[a] *Paul Scherrer Institut,*
Villigen 5232, Switzerland
[b] *DESY,*
Notkestrasse 85, D-22607 Hamburg, Germany

E-mail: aldo.mozzanica@psi.ch

ABSTRACT: A charge integrating readout ASIC (Application Specific Integrated Circuit) for silicon strip sensors has been developed at PSI in collaboration with DESY. The goal of the project is to provide a charge integrating readout system able to cope with the pulsed beam of XFEL machines and at the same time to retain the high dynamic range and single photon resolution performances typical for photon counting systems.
The ASIC, designed in IBM 130 nm CMOS technology, takes advantage of its three gain stages with automatic stage selection to achieve a dynamic range of 10000 12 keV photons and a noise better than 300 e.n.c.. The 4 analog outputs of the ASIC are optimized for speed, allowing frame rates higher than 1 MHz, without compromises on linearity and noise performances. This work presents the design features of the ASIC, and reports the characterization results of the chip itself.

KEYWORDS: X-ray detectors; Si microstrip and pad detectors; Front-end electronics for detector readout

[1] Corresponding author.

doi:10.1088/1748-0221/7/01/C01019

Contents

2012 JINST 7 C01019

1 Introduction

A new generation of free electron laser based Xray sources is emerging: the Linac Coherent Light Source [1] (LCLS) and SPring-8 Angstrom Compact Free Electron [2] (Sacla) are operational, the European X-ray Free Electron Laser [3] (E-XFEL) is under construction at DESY, and the Swiss Free Electron Laser [4] (SwissFEL) is planned to be commissioned in 2016.

These machines introduce a new set of requirements from the detector point of view, which can be summarized in the following points:

- single photon sensitivity, to offer a data quality similar to a photon counting device at low intensities
- extremely high dynamic range, up to 10^4 12 keV photons per pulse per channel
- low noise over the full range, so that measurements are limited by the photon statistics and not by the detector noise itself
- ability to cope with the 4.5 MHz repetition rate of the E-XFEL machine.

The Paul Scherrer Institut is part of the AGIPD collaboration [5, 6], which develops a 2D detector for the E-XFEL, and is committed to the development of detectors for the SwissFEL project. In this framework the detector group at PSI has developed, in collaboration with DESY, a 1D microstrip detector system called GOTTHARD (Gain Optimizing microsTrip sysTem witH Analog ReaDout), whose readout ASIC is the topic of this work.

The first part of the paper is focused on the design of the ASIC itself: the preamplifier and the gain switching logic are described in section 2.1, while section 2.2 gives an overview of the CDS and fast readout chain architectures. In Sec 3 the paper reports the results obtained during the device characterization. Section 3.1 focuses on the noise measurement in the single photon regime, while in section 3.2 the noise at low gain and the linearity are addressed.

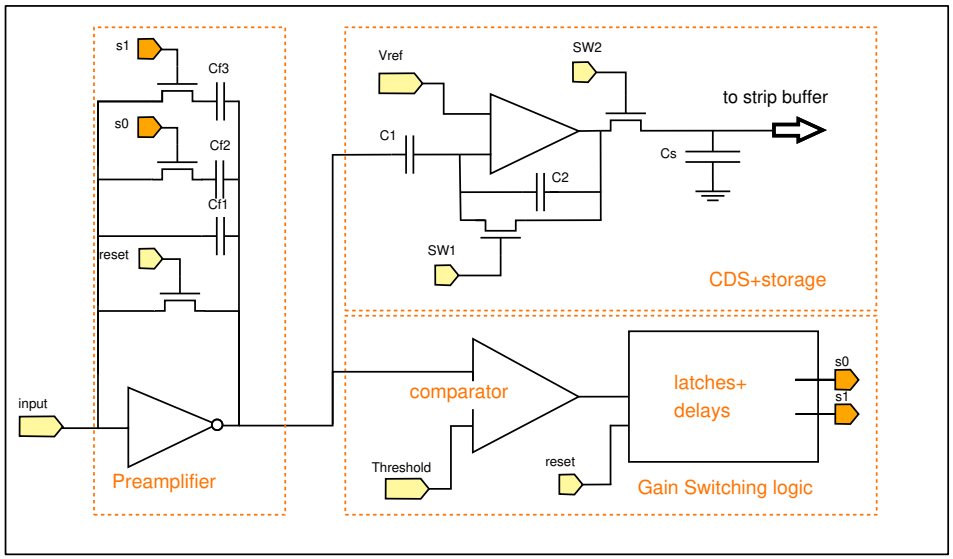

Figure 1. Schematic view of the channel architecture.

2 ASIC design

The ASIC has been designed with a modular detector system in mind. On the module, a row of ten ASICs is wire bonded to a 1280 strip 50 μm pitch silicon sensor, as in the MYTHEN detector [7, 8]. The GOTTHARD ASIC, designed in IBM 130 nm technology, consists of 128 identical channels, operated in parallel, and of the periphery circuitry which provides the I/O capabilities and the digital control of the chip. The channels are stacked together to allow wire bonding of the input pad of each channel to the corresponding pad on a 50 μm pitch strip sensor. The design is the result of a multi year effort: three prototype ASICs have been developed, and after every iteration extensive tests have been performed on the prototypes themselves. The early tests are reported in [9].

The ASIC is quite compact, its physical dimensions being 6.4×1.2 mm^2. In the following subsections the various blocks composing the ASIC design are described.

2.1 Preamplifier with gain switching logic

The front end block, shown in figure 1, is based on an inverter based preamplifier in charge integrating configuration. The preamplifier gain can be tuned: a fixed small size feedback capacitor is used for the high gain, while the insertion of two capacitors, $\sim$10 and $\sim$100 times bigger respectively, lowers the gain to a medium or low value. While the gain setting can be fixed with an external signal, in the normal mode of operation the control of the gain is automatically handled by the front end circuit itself. For this purpose, the output of the preamplifier is continuously monitored by a comparator. When the signal level crosses the threshold the gain switching logic is triggered. The threshold voltage is common for all the channels and is placed at the border of the output range of the preamplifier. The logic, based on delay stages and latches, controls the insertion of the feedback capacitors, according to the following rules:

- if the switching from high to the medium gain is not enough to bring the output back into the preamplifier output range, after $\sim$5 ns a second switching to low gain is performed

2012 JINST 7 C01019

- the second switching from medium to low should not be done in case of signal spikes due to the transient response after the first switching.

In the idle state the preamplifier is kept in reset at the low gain mode, so that all the feedback capacitor are emptied. A few nanoseconds before the beginning of the measurement these capacitors are disconnected so that the gain is set to high. Then the reset switch is opened and the input charge starts to be integrated. The amplifier switches depending on the amount of input charge flowing into the readout channel. The output voltage and the gain (encoded in two digital bits) are sampled at the end of the integration time. Together, these allow to determine the incoming charge with the help of a gain calibration curve.

2.2 CDS stage and fast analog readout

One of the main sources of noise at the high gain setting is the reset noise, i.e. the fluctuations of the preamplifier output voltage $V_{\mathrm{pre}}(t)$ after the release of the reset switch. This reset voltage acts as a baseline on top of which the real integrated signal starts rising, so that its fluctuations directly contribute to the output noise. This noise source can be effectively neutralized with a CDS (Correlated Double Sampling) stage [10]. The goal of this stage is to perform an analogue subtraction between the preamplifier output voltage at a time t_1 ($V_{\mathrm{pre}}(t_1)$) and the voltage of the same node at a time t_2 ($V_{\mathrm{pre}}(t_2)$). This is accomplished by one operational amplifier with a feedback capacitor as shown in figure 1: if the switch SW1 is opened at time t_1, the output V_{cds} of the CDS operational amplifier is equal to $V_{\mathrm{cds}}(t) = V_{\mathrm{ref}} + (C_1/C_2)(V_{\mathrm{pre}}(t_1) - V_{\mathrm{pre}}(t))$. If the switch SW2 is opened at t_2, the voltage stored on the C_s capacitor is linear with $V_{\mathrm{pre}}(t_1) - V_{\mathrm{pre}}(t_2)$. The gain of the stage can be tuned changing the ratio between C_1 and C_2. In the normal switching gain operation a gain of ~ 1.6 for the CDS stage has been chosen; this value allows the use of most of the preamplifier and the operational amplifier output ranges. A second mode of operation, called VHG (Very High Gain) mode, can be selected: this mode disables the automatic switching, fixes the preamplifier in high gain and doubles the value of C_2 inserting a second capacitor in parallel. This has a dual effect of increasing the gain of the CDS stage to ~ 3, which suppresses any noise contribution from the downstream readout chain, and of reducing the bandwidth of the preamplifier due to the increased output load. Measurements performed on prototypes showed that the CDS technique is not beneficial when the gain is switched: the output voltage after switching (medium or low gain) shows smaller fluctuations with respect to the voltage stored at t_1, with the preamplifier in high gain. For this reason a digital logic that bypasses the CDS stage after the first gain switching has been implemented.

At the end of the integration time (i.e. when SW2 opens) the analog signals present at the 128 storage capacitors C_s on the chip have to be sent to the external ADCs to be digitized. The task is accomplished by a readout chain, which has been designed to fulfill the following requirements:

- it has to be fast, in order to collect the highest possible fraction of the 4.5 MHz repetition rate E-XFEL pulses. A frame rate of 1 MHz has been selected as a design target
- it has to be low noise, so that the noise contribution from the readout would be negligible with respect to the preamplifier noise, at least for the HG and VHG modes
- can be directly coupled to the ADC inputs, in order to greatly simplify the system design.

2012 JINST 7 C01019

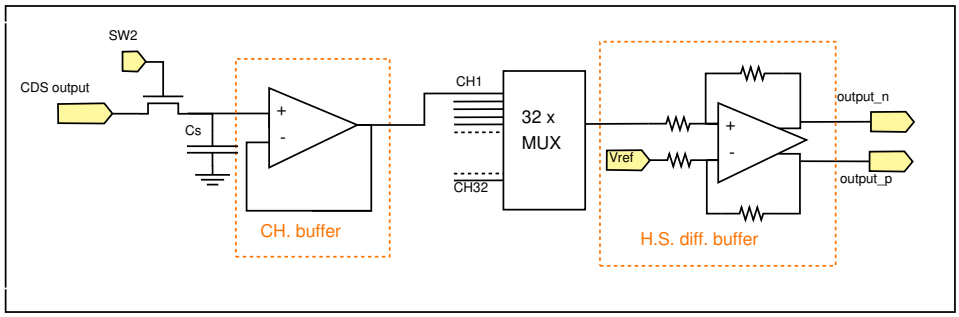

Figure 2. Schematic representation of the high speed readout chain. The signal stored on the sampling capacitor C_s is buffered and the buffer output feeds, through a multiplexer, the high speed single ended to differential off-chip driver. The 128 channels of the ASIC are divided in 4 blocks of 32 channels each.

The former requirement is the hardest to fulfill. The 1 MHz readout speed has been achieved with a fast readout clock (32 MHz) together with a parallel readout architecture, consisting of 4 analog outputs per chip, or 40 ADC channels per detector module. A schematic view of the resulting readout circuit is shown in figure 2: the 128 channels are grouped in 4 groups of 32 channels each. A distributed multiplexer, clocked at 32 MHz, connects one channel at a time to the off chip driver. The capacitive load of the bus line and of the off-chip driver input node has to be charged in $(32\ \text{MHz})^{-1}$=33 ns; for this reason a high power buffer is present at the output of each channel. The off chip driver converts the signals from single ended to differential and is strong enough to drive the low impedance load of the ADC input.[1]

3 ASIC characterization

The ASIC performances were tested with the help of a prototype assembly shown in figure 3. The ASIC and the sensor were mounted and wire bonded to an adapter PCB (Printed Circuit Board), which was mounted on the general purpose test system as described in [9]. The sensor strips have an estimated capacitance of $\sim$ 1 pF. The following subsections will report the results obtained in terms of noise and linearity on the full dynamic range of the ASIC.

3.1 Noise at high gain

To measure the noise in the high sensitivity range, the automatic switching has been disabled and the gain fixed to HG or VHG. The detector has been irradiated with Xray fluorescence light (from Mo, Ag and Cu samples) generated in a Xray tube setup at PSI. While the ASIC noise in ADC units can be measured in absence of any signal, the photon irradiation is essential to calibrate the system in terms of eV/ADC, which allows a conversion of the noise in eV or equivalent noise charge (e.n.c.). A few μs integration time was selected; this value is big enough to get reasonable photon statistics but small enough to make the leakage current contribution to the noise negligible. For each measurement a large number of frames has been collected, with and without photons: the ones without photons have been used to compute the "dark image", a channel by channel offset which takes into account both the variation in the electronics and the sensor leakage current.

[1] The converter is the AD9252, a 8 channel 50Ms/s 14 bit ADC from Analog Device.

2012 JINST 7 C01019

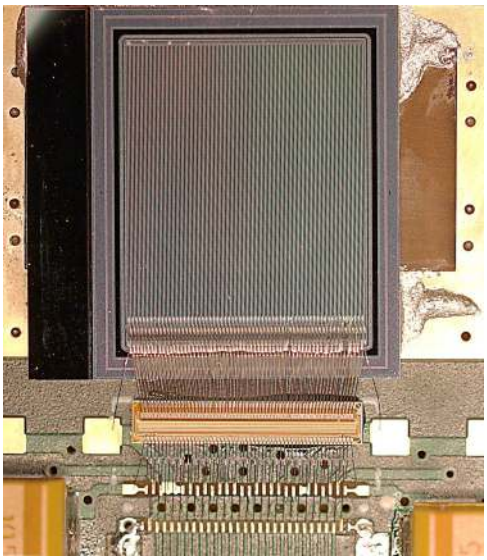

Figure 3. Picture of a GOTTHARD readout ASIC wire bonded to a 128 channel 50 μm pitch silicon microstrip sensor. This prototype assembly was used for the tests reported in this work.

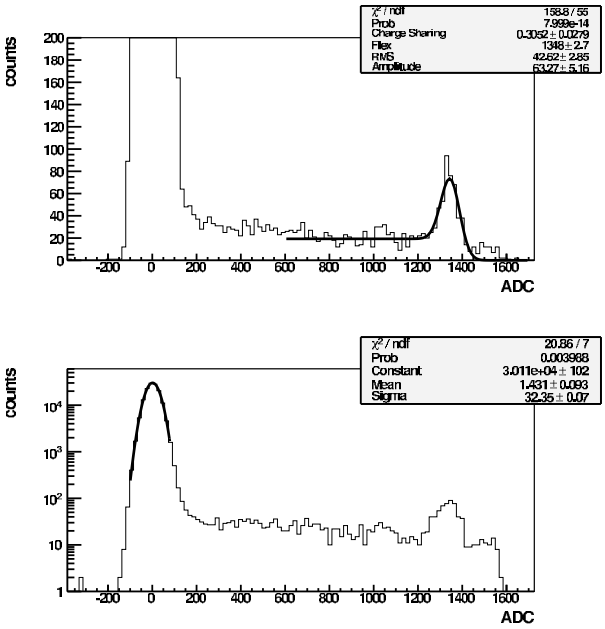

Figure 4. Pulse height distribution, in linear and logarithmic scales, of a typical ASIC channel in case of Ag fluorescence light irradiation, with gain set to VHG. The noise peak, fitted with a Gaussian curve, measures the noise in ADC units, and the position of the photon peak, fitted with a Gaussian superimposed to an error function that takes into account the charge sharing effect, allows to obtain the gain in eV/ADC (16.4 eV/ADC in this example). The width of the photon peak is bigger than the noise peak one because it is the result of the superposition of the K_α and K_β fluorescence lines.

This dark image is then subtracted from the data recorded with Xrays: the resulting pulse height distribution for a typical channel in VHG mode is shown in figure 4. From the fitting parameter on

2012 JINST 7 C01019

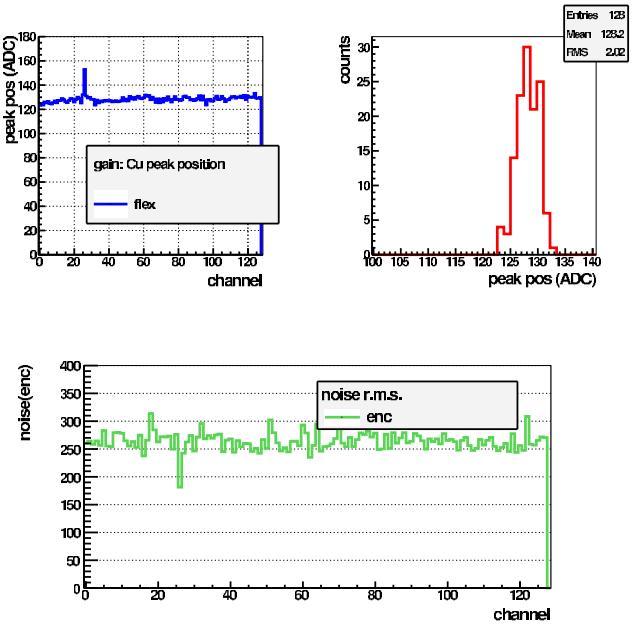

Figure 5. Profile and distribution of the gain (top), measured as the photon peak position, and noise profile (bottom) for the detector in HG mode and Cu fluorescent light irradiation. Channel 26 is unconnected to the sensor and the fitting algorithm did not converge.

the plot, a noise of $\sim$ 150 e.n.c. can be computed for this channel; others channels have a noise (in VHG mode) within 10% of this value.

The gain and noise profiles can be extracted fitting the pulse height distributions of all channels: figure 5 shows, for a Cu irradiation and HG mode, a gain uniformity better than 2 % and a noise better than 300 e.n.c.. Assuming a conservative limit for the photon detection of 5 σ above the noise floor, the measured noise figures assure a single photon sensitivity down to $\sim$5.5 keV in HG mode and down to $\sim$2.7 keV in VHG mode.

3.2 Noise and non linearity in gain switching mode

The ASIC performances at the lower gain cannot easily be tested with Xrays: in fact, the noise of the electronics is smaller than the fluctuation on the number of photons itself (that follows a Poisson statistics). For this reason, a different source of signal had to be used. A battery powered low intensity lamp shining on the detector has been selected. Since the conversion of one visible light photon in the detector generates only one electron-hole pair compared to the few thousand from one Xray, the Poisson fluctuations in the number of the visible light photons are, for the same detector input signal, reduced by the square root of this ratio, and are thus negligible. Since the light flux was constant, the collected charge has been changed simply varying the integration time; this can be controlled with a high resolution and the method gives a charge at the input that is intrinsically linear.

With the ASIC in automatic switching gain mode, the integration time has been increased in small steps, and for each step hundreds of frames have been recorded. The mean value and r.m.s. of these frames have been extracted: the resulting plot is shown, for a typical channel, in figure 6. A

2012 JINST 7 C01019

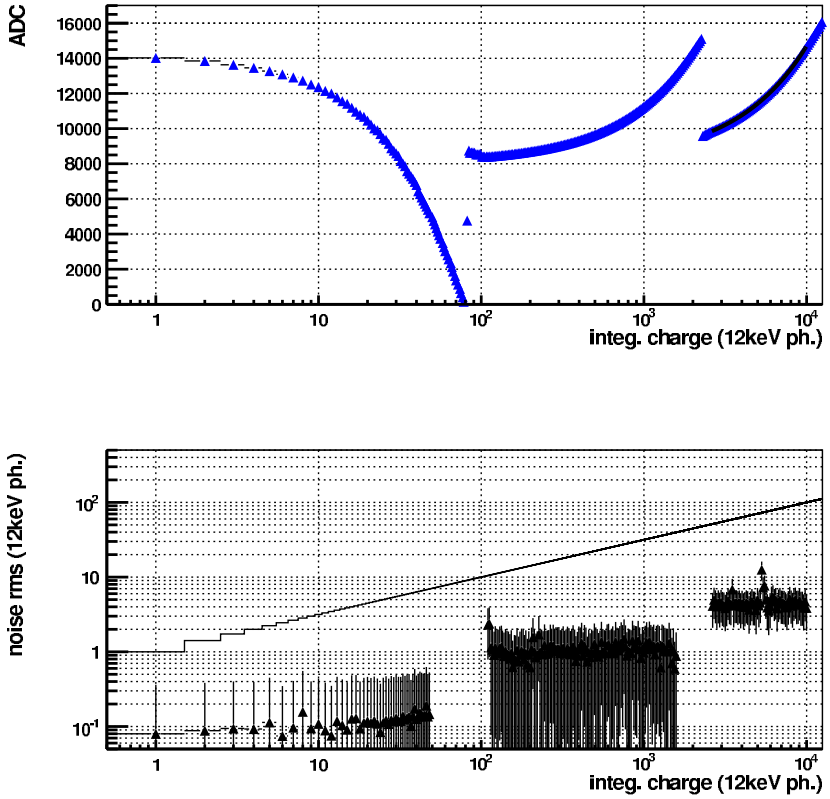

Figure 6. Typical channel response as a function of the input charge (top), in logarithmic scale, and noise as a function of the input charge (bottom), in bi-logarithmic scale. The line in the bottom plot is the Poisson statistical limit equal to the square root of the number of photons. Note that the sign of the slope of medium and low gain is reversed, due to the bypass of the CDS stage that is automatically performed after the switch. See the text for the axis conversion procedure. Noise data points are not computed in the switching regions, since the conversion factors are not well defined if the digital gain information is, as in this case, not used.

linear fit of the output vs. time curve in the HG region has been used, together with the conversion factor eV/ADC extracted from the single photon measurements, to translate the X scale from time unit into number of 12 keV photons. The slopes of the linear fits of the three gain regions, are the conversion factors that have been used to translate the r.m.s. noise from ADC units into the number of photons. The results completely fulfill the design specifications, with a dynamic range in excess of 10^4 12 keV photons and a noise that is everywhere negligible with respect to the Poisson photon fluctuations.

The same data set used for noise evaluation can be used to measure the linearity error of the ASIC: this can be defined as the difference between the data points of figure 6 (top) and a linear function fitting them. The results are shown in figure 7, in linear and logarithmic scales: the errors from linearity are smaller than one 12 keV photon at low input values and within $\pm 0.5\%$ of the incoming signal at higher intensities. This values should be acceptable for most experiments; in case a better linearity is required it is possible to reduce the threshold, to use only the more linear part of the response (e.g. from 2000 to 7000 photons for low gain - see figure 7(top)), but reducing at the same time the dynamic range of the system.

2012 JINST 7 C01019

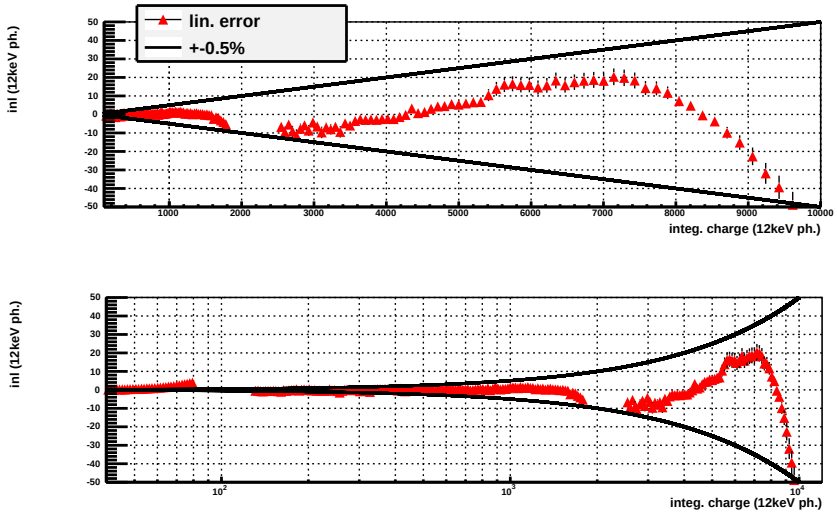

Figure 7. Linearity error, or integral non linearity, as a function of the input charge, in linear (top) and logarithmic (bottom) scales. A $\pm 0.5\%$ error band is also shown.

4 Conclusions

A readout ASIC for a microstrip silicon sensors based on charge integration and automatic gain switching has been developed and tested at the Paul Scherrer Institut. The characterization of the chip demonstrated the fulfillment of the design specification, in particular:

- single photon sensitivity for photon energies down to a few keV
- gain uniformity at a few percent level
- dynamic range up to than 10^4 12 keV photons
- electronic noise negligible with respect to statistic photon fluctuations
- linearity better than 0.5% for the full dynamic range.

Following these positive tests, the readout chip is being integrated into bigger systems: a detector module with 10 ASICs coupled to a 1280 channels 50μm pitch sensor has been designed and is now in the commissioning phase. The detector module is equipped with a Gigabit data link. This allows a continuous frame rate greater than 50 kHz for operation at Synchrotron sources as well as a 1 MHz frame rate, in bursts, for operation at the E-XFEL. The characterization of the complete detector module will be the focus of future work.

References

[1] https://slacportal.slac.stanford.edu

[2] T.Takan and T. Shintake, *SCSS X-FEL Conceptual Design Report*, Japan (2005), http://www-xfel.spring8.or.jp/SCSSCDR.pdf.

2012 JINST 7 C01019

[3] M. Altarelli et al., *The European X-Ray free-electron laser, technical design report*, DESY 2006-097 (2006).

[4] R. Ganter et al., *SwissFEL Conceptual Design Report*, PSI Bericht 10-04 (2010), http://www.psi.ch/swissfel/CurrentSwissFELPublicationsEN/SwissFEL_CDR__v19_03.03.11-small.pdf

[5] X. Shi et al., *Challenges in chip design for the AGIPD detector*, *Nucl. Instr. Meth.* **A 624** (2010) 387.

[6] B. Henrich et al., *The adaptive gain integrating pixel detector for the European XFEL*, *Nucl. Instr. Meth.* **A 633** (2011) S11.

[7] A. Bergamaschi et al., *Photon counting microstrip detector for time resolved powder diffraction experiments*, *Nucl. Instrum. Meth.* **A 604** (2009) 136.

[8] A. Mozzanica et al., *MythenII: A 128 channel single photon counting readout chip*, *Nucl. Instrum. Meth.* **A 607** (2009) 250.

[9] A. Mozzanica et al., *A single photon resolution integrating chip for microstrip detectors*,*Nucl. Instrum. Meth.* **A 633** (2011) S29.

[10] W. Buttler at al., *Noise filtering for readout electronics*, *Nucl. Instrum. Meth.* **A 288** (1990) 187.

2012 JINST 7 C01019