The Heterogeneous Integration of Optical Interconnections Into Integrated Microsystems

Nan Marie Jokerst, *Fellow, IEEE*, Martin A. Brooke, *Member, IEEE*, Sang-Yeon Cho, Scott Wilkinson, Michael Vrazel, Suzanne Fike, John Tabler, Yoong Joon Joo, Sang-Woo Seo, D. Scott Wills, and April Brown

Invited Paper

***Abstract*—Emerging techniques for integrating optoelectronic (OE) devices, analog interface circuitry, RF circuitry, and digital logic into ultra-mixed signal systems offers approaches toward and demonstrations of integrated optical interconnections in electrical microsystems. As rising data rates dictate the use of optical interconnections and interfaces at increasingly smaller distances, optical interconnections stand at a threshold of opportunity for pervasive implementation if cost-effective integration process technology and performance can be implemented. Heterogeneous integration is one approach toward the integration of compound semiconductor OE devices, Si CMOS circuits, and organic materials. Heterogeneous integration approaches, which utilize dissimilar materials which can be independently grown and optimized, and are subsequently bonded together into an integrated system, are particularly attractive methods for creating high-performance microsystems. This paper describes a variety of optical interconnections integrated into microsystems using thin film heterogeneous integration. Thin film heterogeneous integration is attractive from the standpoint that the topography of the integrated microsystem can remain flat to within a few microns, substrates which are often optically absorbing are removed, both sides of the thin film devices can be processed (e.g., contacted, optically coated), and three-dimensionally stacked structures can be implemented. Demonstrations of interconnections using thin film heterogeneous integration technology include an integrated InGaAs/Si CMOS receiver circuit operating at 1 Gbps, an InGaAs thin film photodetector bonded onto a foundry Si CMOS microprocessor to demonstrate a single chip optically interconnected microprocessor, smart pixel emitter and detector arrays using resonant cavity enhanced P-i-N photodetectors bonded on top of per-pixel current controlled oscillators and resonant cavity enhanced light emitting diodes integrated onto digital to analog converter gray-scale per-pixel driver circuitry, and photodetectors embedded in waveguides on electrical interconnection substrates to demonstrate chip-to-chip embedded waveguide interconnections.**

***Index Terms*—Embedded MSM photodetector, heterogeneous integration, high-speed optical interconnection, integrated microsystems.**

Manuscript received December 6, 2002; revised February 5, 2003. This work was supported in part by the National Science Foundation, in part by the National Science Foundation Electronic Packaging Research Center and its member companies, in part by the State of Georgia Yamacraw Initiative and its member companies, in part by the Georgia Tech Broadband Institute and its member companies, and in part by the Air Force Office of Scientific Research.

N. M. Jokerst, M. A. Brooke, and A. Brown were with the School of Electrical and Computer Engineering, National Science Foundation Packaging Research Center, Georgia Institute of Technology, Atlanta, GA 30332-0250 USA. They are now with the Pratt School of Engineering, Department of Electrical and Computer Engineering, Duke University, Durham, NC 27708–0291 USA (e-mail: njokerst@ee.duke.edu).

S.-Y. Cho, S. Wilkinson, M. Vrazel, S. Fike, J. Tabler, Y. J. Joo, S.-W. Seo, and D. S. Wills are with the School of Electrical and Computer Engineering, National Science Foundation Packaging Research Center, Georgia Institute of Technology, Atlanta, GA 30332-0250 USA.

Digital Object Identifier 10.1109/JSTQE.2003.813307

I. Introduction and Motivation

OPTICAL interconnections are pervasive at long-haul distances, and, as per-channel data rates rise, conventional electrical interconnections face multiple challenges at increasingly shorter distances. Electrical interconnects face critical tradeoffs between power consumption, interconnect area, and signal integrity, even at interconnect lengths as short as the board, module, and chip level. Physical material and structural limitations will ultimately force technology changes at the physical layer if interconnect and system performance gains are to continue well into the future. Critical questions facing optical interconnections are how to implement optical interconnections at these shorter distances and, in fact, all distances, in a cost-effective manner, and what are the breakpoints at which it is necessary and at which it is possible to integrate optical interconnections and interfaces into a system. Eventually, the integration of optical signal handling and processing into electrical systems will also be justified by some system specifications.

For the next generation of systems, optical technology now stands at a threshold where the integration of optical interconnections and optical functions into board, package, and chip-level electrical systems is projected in industry roadmaps. These projections for the integration of optical interconnections range from 5 to 15 years, but the preponderance of electrical microsystem analyses project that optics will play a role in electrical systems. Critical to the implementation of optics in electronic systems is the method of integration and the cost to integrate the optics. The integration of optical functions such as interconnection into system-on-a-package (SOP) and system-on-a-chip (SOC) implementations stands at a similar threshold to that which electronics faced in the 1970s. Electronics in the 1970s stepped into the modern electronic age through the revolution that transformed common circuits from discrete components mounted on boards to integrated circuits in silicon. The unit cost and circuit complexity advantages that directly resulted from high yield, large area parallel fabrication of circuits in an integrated process such as silicon CMOS have

1077-260X/03$17.00 © 2003 IEEE

led to the unparalleled increases in computational performance at a diminishing cost that the world has enjoyed for the last 25 years. If optical interconnections can be integrated at the board, package, and chip level with processes that are compatible with, and cost comparable to, electronic manufacturing technologies, then optics will see high volume, broad market implementation.

Many quantitative comparisons of interconnection performance have been published discussing electrical and optical interconnections [1]–[3], and the question of how to integrate optical interconnections into an electrical interconnection system is currently a topic of intensive study. Optical interconnect approaches include free-space interconnects with diffractive optical elements [4], silicon optical bench interconnects [5], and guided wave interconnections, including substrate guided mode interconnects [6], fiber-optic waveguides [7], and integrated waveguides [8]. This paper will discuss a heterogeneous integration approach to optical interconnection interfaces for fiber, free space, and waveguide optical interconnections both singly and in "smart pixel" arrays, and will explore a fully integrated planar lightwave circuit approach to microsystems integration with optical interconnection, as well.

One of the most critical questions that must be addressed for optical interconnections and interfaces in electrical systems relates to material compatibility and process compatibility with the wide variety of materials that are used today in electrical microsystems. The electronic materials used commonly today are not necessarily those that will optimally be used for the integration of optical signals into these microsystems. The materials choices cover a wide range of organic and inorganic materials, and material development, with a particular emphasis on polymers, is an area of intensive research and progress. Materials that are of interest for integrated microsystems include silicon and Si CMOS circuits, compound semiconductors and the optoelectronic (OE) and high-speed electronic devices fabricated from these materials, organics such as polymers and epoxies for optical waveguides and electronic substrates, inorganic materials such as silicon dioxide and silicon nitride for passivation, encapsulation, and waveguides, and metals for electrical interconnections. The microsystem integration of these materials, using processes and structures that do not compromise the performance optimization of individual components in the integrated microsystem, is an ambitious goal in this field.

One approach to microsystems integration is heterogeneous integration, or the bonding and processing of dissimilar materials into a single system. Because the components for integration are separately grown and can be partially to fully fabricated before integration, the opportunity to demonstrate high levels of performance with few device fabrication tradeoffs and little processing impact is possible. Generally, the heterogeneous integration of materials utilizes deposition technologies and bonding technologies for devices that may or may not include a metal electrical interconnection layer.

There are a number of approaches to heterogeneous integration, including bump bonding (also called flip chip bonding) [9], wafer bonding [10], and thin film integration (sometimes also called epitaxial liftoff [11]). Bump bonding is a quite common commercial bonding technology for mounting chips onto boards which uses microscale balls of metal on device surface contacts to connect chips to boards. Drawbacks to bump bonding include the condition that all contacts are available on one surface for bumping, and that substrates are often not optically transparent. Wafer bonding, which atomically bonds together semiconductor and/or oxide interfaces using pressure and temperature, offers an attractive method of bonding a different material into a host substrate. Wafer bonding lends itself most directly to systems that need areas of bonded material consistent with compound semiconductor growth substrates. Drawbacks to wafer bonding include the degradation of Si CMOS circuits as host substrates in the wafer bonding process, and the relatively small size of compound semiconductor growth substrates compared to Si and board/module substrates. Often, the prospect for mixing and matching bonded material structures and devices on one substrate is attractive for an integrated microsystem, and often, these bonded devices are only necessary in a small, selected area of the host substrate.

The third approach is thin film integration, which bonds components in thin film form (with the growth/fabrication substrate removed) onto a host substrate to form the integrated microsystem [12]. Thin film heterogeneous integration is attractive from the standpoint that the topography of the integrated microsystem can remain flat to within a few microns, substrates which are often optically absorbing are removed, both sides of the thin film devices can be processed (e.g., contacted, optically coated) [13], and three-dimensionally stacked structures can be implemented [14], [15]. The primary drawback to thin film integration is that materials and devices which are on the order of microns thick must either be transferred and bonded after the growth substrate is removed (although this enables selective, sparse distribution of different structures over the host substrate) or the growth substrate must be removed from the device after bonding.

A number of heterogeneously integrated microsystem optical interconnections and interfaces have been demonstrated using thin film integration, and some unique integration opportunities exist for thin film integration, including three-dimensional (3-D) stacking of active devices, and embedding OE devices into waveguides. In the next sections of this paper, thin film InGaAs photodetectors heterogeneously integrated receiver links will be presented, and then, results from these receiver links integrated with a microprocessor on a single chip will be discussed. These integrated microsystem interconnections are focused upon surface normal optical input. For "SOP" optical interconnection implementations, waveguides are attractive choices, and, in this context, beam turning from the waveguide onto the substrate is important. An alternative to beam turning from waveguides is to embed photodetectors in the waveguides, and to electrically interconnect the receiver circuits to the electrical outputs of the photodetector (thus,"turning the electrons" rather than the photons). The heterogeneous integration of thin film InGaAs photodetectors integrated onto Si electrical interconnection substrates that are embedded in polymer waveguides will be the final topic herein addressing heterogeneously integrated optical interconnections.

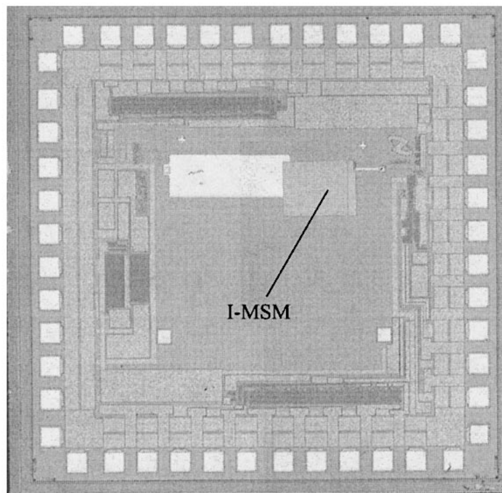

Fig. 1. 250×250 μm^2 InGaAs/InP I-MSM integrated onto a 0.25-μm differential Si CMOS receiver.

II. Heterogeneous Integration of Thin Film Photodetectors Onto Si CMOS Circuits

Heterogeneous integration often offers a significant reduction of packaging parasitics between the integrated device and the host substrate. One example is the integration of photodetectors directly onto transimpedance amplifiers (TIAs). By eliminating the wire bonds and package leads between these components, packaging parasitic limitations such as the typical 50-Ω input impedance to the TIA can be avoided. By directly bonding the photodetector to the TIA, a higher input impedance can be used, and, as a result, the TIA design can be more sensitive. Just as important from a noise standpoint, by minimizing the interconnection distance from the photodetector output to the TIA input, pickup of digital noise can be minimized. Digital noise is a critical factor in the design of integrated OE interconnections into digital electronic systems. When complex very large scale integration (VLSI) circuitry such as a microprocessor is integrated onto the same integrated circuit as a sensitive OE TIA, the 100–500 mV of noise created by a typical microprocessor generates high levels of signal noise in the receiver input. Noise immunity is a critical issue for highly sensitive analog circuitry operating in mixed-signal systems. Typical optical receivers use a single-ended analog preamplifier, which is highly susceptible to power supply fluctuations and external noise. In particular, analog receivers operating in digital environments are subject to power rails through the substrate. For these types of mixed-signal applications, a differential analog design provides improved noise immunity as well as stable biases for OE devices within the system. Differential receiver circuits utilize more space and more power than single ended designs, but are capable of operating in noisy digital environments. Fig. 1 is a photomicrograph of a 0.35-μm digital Si CMOS differential receiver circuit that was designed for heterogeneous integration and operation at 1 Gbps. This design is a building block OE interface that is intended for insertion onto a single Si CMOS chip with complex, noisy Si CMOS logic circuitry. This 1 Gbps differential receiver was heterogeneously integrated with a large-area thin film InGaAs/InP inverted (I-) metal-semiconductor-metal (MSM) photodetector to realize an OE integrated circuit (OEIC) sensitive to wavelengths of 1.3 and 1.55 μm.

The I-MSM photodetectors are an example of how thin film device designs can be used to enhance device performance. Even though MSM structure photodetectors have a lower intrinsic capacitance than P-i-N photodetectors, which enables MSMs to operate at a higher speed for the same detection area, the MSM finger electrodes of conventional MSMs shadows the optical input to the devices, thus decreasing the responsivity of the photodetector. Numerous MSM investigations including back illumination [16] and transparent electrodes [17] have addressed this responsivity problem, however, back illumination creates practical problems in optical alignment and packaging, and the resistivity of the transparent electrodes causes speed degradation in the MSMs. Although these devices exhibited responsivities of 0.75 A/W, the submicron features, defined using electron beam direct write lithography, has limited throughput for manufacturing at this time. I-MSMs are thin film MSMs with the growth substrate removed and fingers on the bottom of the device to eliminate finger shadowing, to enhance the MSM responsivity [18]. These I-MSMs exhibit responsivities comparable to P-i-N photodiodes while maintaining lower capacitances per unit area than P-i-Ns, which enable much larger detecting areas for similar device capacitances [18]. The photodetector in Fig. 1 is a heterogeneously integrated 250×250 μm^2 InGaAs I-MSM bonded to a fully differential Si CMOS receiver. This integrated receiver operated at 1 Gbps with a bit-error-rate (BER) of 6.8×10^{-10} and demonstrated a high level of alignment tolerance due to the large photodetector [189]. Typical responsivities for these nonantireflection coated devices integrated in Fig. 1 was 0.5 A/W, although responsivities for antireflection coated devices of 0.7 A/W has been reported for an I-MSM with a 1-μm-thick absorbing region [18]. For a specified data rate, the electrode geometry, layer structure, and area of the I-MSM can be optimized for a particular application. The results reported herein pertain to OE receivers designed specifically for alignment tolerance.

The I-MSM photodetectors integrated onto the TIA in Fig. 1 were grown by molecular-beam-epitaxy on semi-insulating InP. The grown layers consisted of: 2000 Å InGaAs stop etch layer, 400 Å InAlAs cap layer, 500 Å graded layer, 7400 Å InGaAs absorbing layer, 500 Å graded layer, and 400 Å InAlAs cap layer. All layers were nominally undoped and lattice-matched to the InP substrate. The InAlAs cap layers were used to enhance the Schottky barrier height of the MSM photodetector. The graded layers smoothed heterostructure energy band discontinuities, which can trap photogenerated carriers and degrade the bandwidth of the detector. The InGaAs absorbing region made these detectors suitable for detecting wavelengths of 1.3 and 1.55 μm. Ti/Au electrodes were deposited as the Schottky contacts with thicknesses of 250 Å and 2250Å, respectively. The detectors were fabricated with 250×250 μm^2 detecting areas, and the electrodes were 2-μm-wide with 5-μm spacings, with a calculated capacitance of 0.43 pF. MSM device mesas were defined photolithographically, etched down to the stop etch layer using citric acid/H_2O_2 (10 : 1), and the mesas were then embedded in a handling layer of Apeizion W

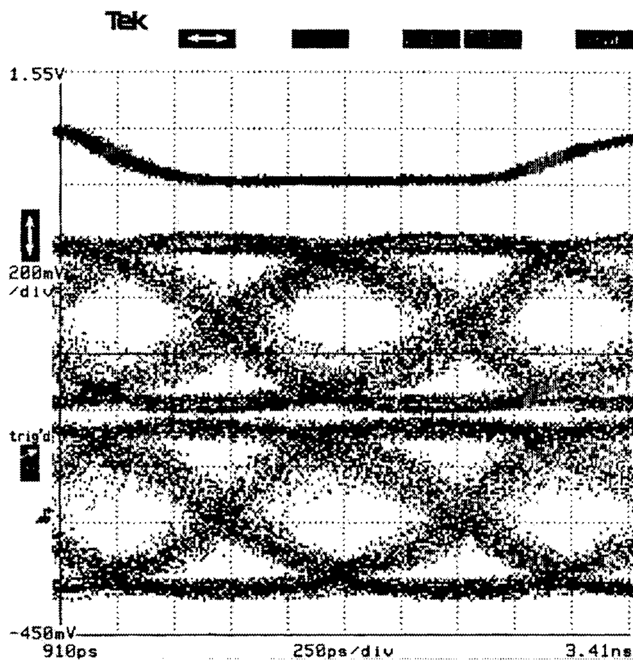

Fig. 2. Eye diagram of the differential receiver outputs at 1 Gbps.

wax. The substrate and stop etch layers were removed using HCl and a second citric acid/H_2O_2 (1 : 1) solution, respectively. The mesas were bonded to a transparent transfer diaphragm, the wax handling layer was removed, and individual mesas were bonded metal-metal bonded onto the circuit by bonding the MSM contact pads (which faced the receiver) to the receiver circuit [19]. The BER performance of the integrated receiver was tested using a 1550 nm distributed feedback laser pigtailed to a single-mode fiber. The heterogeneously integrated receiver had a measured BER of 6.8×10^{-10} at a data rate of 1 Gbps with an average optical input power of -10 dBm. The eye diagram at this data rate is shown in Fig. 2. Smaller heterogeneously integrated I-MSM photodetectors with the same material structure and integration process technology have also been integrated. For 50-μm-diameter integrated photodetectors, the integrated TIA operated at 1.2 Gbps with a BER of 10^{-11}.

III. Single-Chip Optically Interconnected Microprocessor

The integrated receiver design implemented in Fig. 1 has also been integrated into 0.8-μm digital Si CMOS with a microprocessor on a single chip, as shown in Fig. 3. The differential receiver was integrated with an I-MSM and operated at 100 Mbps in the noisy digital environment with a BER of 10^{-9}. This heterogenous integrated chip serves as an outstanding example of an "ultra mixed signal system," which incorporates analog, digital, and optical signals integrated onto a chip and which, as a result, offers all of the noise challenges of such integrated microsystems [20].

In this paper, a differential analog receiver was integrated with a digital microprocessor on the same die, and the receiver was integrated and tested in a noisy digital microprocessor environment. The single-instruction multiple-data (SIMD) microprocessor performed simple operations based upon the optical input data. The digital circuitry is a SIMD microprocessor, and acts as a digital noise source for the analog receiver circuit. The integrated receiver/SIMD circuit is a subset of an on-focal plane imaging system, in which the SIMD processes data from an imaging array that is preprocessed by on-focal plane analog to digital converters, and is then passed to the receiver using an optical link [21]. This processor node is part of a processor array called SIMPil [22]. The node includes a traditional processor datapath plus additional units for interfacing with a detector array. The first implementation of the node includes an 8-bit datapath with an arithmetical, logical, and shift unit, and a 16-bit multiply-accumulator, which is commonly used in image processing applications. These functional units access an eight-word register file, and each node has 64 words of local memory. Up to 256 words can be addressed in the instruction set. SIMPil nodes communicate through a nearest neighbor north, east, west, and south (NEWS) network using special registers in the datapath.

The differential receiver that was designed, tested, and integrated with the SIMD microprocessor has a fully differential current mode input, current to voltage conversion, and voltage gain stages [23]. After fabrication of the CMOS circuitry through the MOSIS foundry, the unpackaged die was hybrid integrated with a thin film InP-based I-MSM using the same process described to integrated the differential receiver shown in Fig. 1. The hybrid integrated OEIC was then wire bonded into a pin grid array package and tested.

The electrical and optical performance of the differential receiver integrated with the microprocessor has been measured. At a data rate of 100 Mbps, in the presence of digital noise, with an electrical input current of 5 μA (equivalent to an input sensitivity of -20 dBm, for a 0.5 A/W responsivity detector) into a 50-ohm input resistance with a coupling capacitance of 10 nF, the BER was 10^{-9}. The power dissipation was approximately 50 mW. With a detector integrated onto the receiver and optical signal applied, the receiver output voltage signals output through the on-chip comparator were measured, and produced the eye diagram shown in Fig. 4.

IV. Smart Pixel Optical Interconnection Systems

The heterogeneous integration of arrays of optical emitters and detectors onto circuitry for two-dimensional (2-D) array interconnections is also of great interest for high aggregate data rate output from and input to integrated circuits. In fact, this is an area where historically, for military imaging applications such as focal plane imaging arrays, infrared imaging arrays have been bump bonded to integrated circuit readout and signal processing circuitry [24]. Thin film heterogeneous integration techniques have been used by a number of groups to demonstrate such "Smart Pixel" arrays [25], and herein, an imaging array of photodetectors bonded to Si CMOS luminance to frequency converters (oscillators) and resonant cavity enhanced (RCE) light emitting diodes (LEDs) bonded to gray scale emitter drivers will be discussed. Because the individual pixels are not connected to one another in the final integrated array, there is mitigation of the localized stresses which can exist when bump bonding

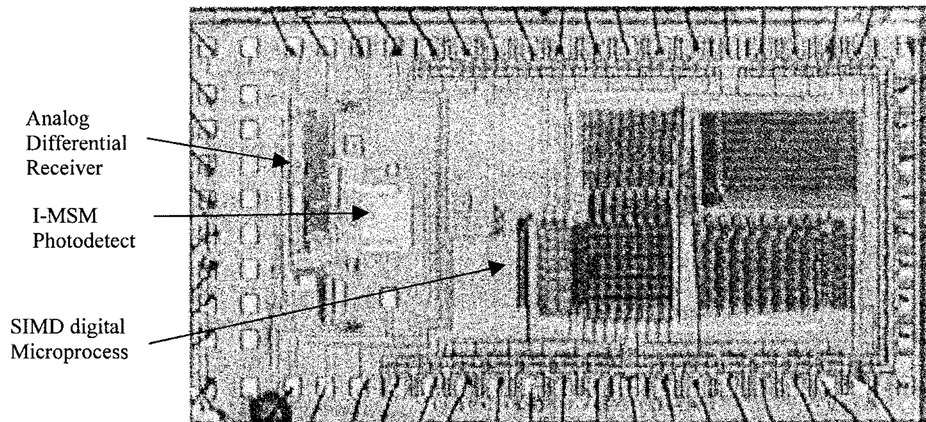

Fig. 3. Photomicrograph of the integrated OE circuit, including the SIMD digital microprocessor, analog differential receiver circuit, and hybrid integrated thin film InP/InGaAs I-MSM.

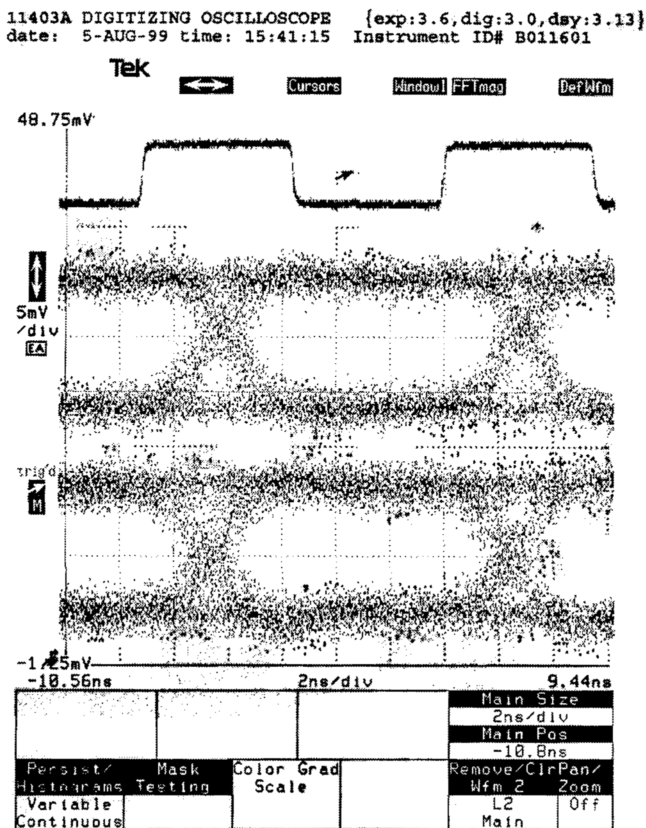

Fig. 4. Eye diagram at 100 Mbps from the output of the receiver integrated with a microprocessor on a single integrated circuit shown in Fig. 3.

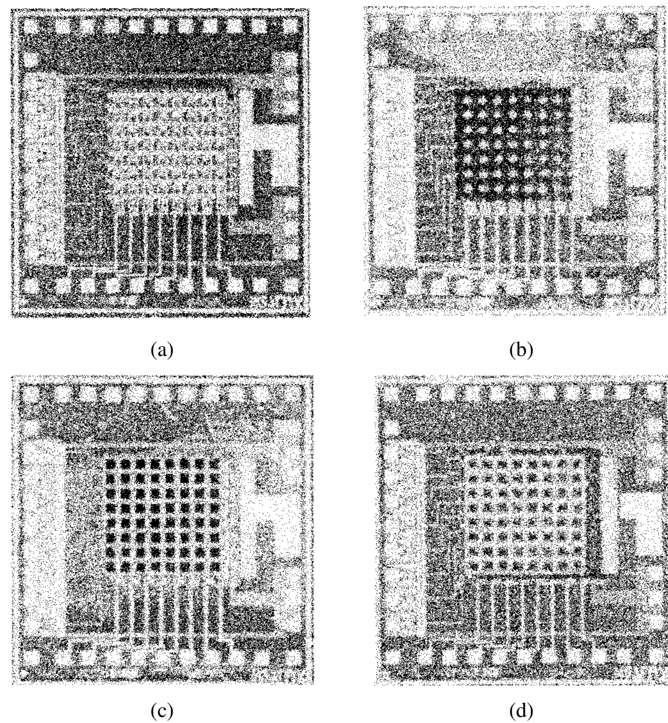

Fig. 5. Photomicrographs of thin film heterogeneously integrated thin film GaAs/AlGaAs P-i-N detector array bonded directly on top of an 8 × 8 array of Si CMOS VLSI signal processing circuitry. (a) Si CMOS VLSI circuit. (b) Thin film GaAs PiN detector linked array metal/metal bonded to Si CMOS circuit. (c) Separation of array. (d) Isolation and top metallization to complete the heterogeneous integration.

standard imaging arrays (with the growth substrate attached) to signal processing circuitry substrates which are not matched in coefficient of thermal expansion to the imaging array.

To create the smart pixel imager, an 8 × 8 array of thin film P-i-N photodetectors was integrated directly on top of a silicon MOSIS TinyChip using thin film integration techniques similar to those described earlier. The compound semiconductor detector array was fabricated from AlGaAs/GaAs/AlGaAs double heterostructure (DH) P-i-N material. The lattice-matched detector material, as grown, consisted of a semi-insulating GaAs substrate, AlAs (undoped, 2000 Å) sacrificial etch layer, $Al_{0.3}Ga_{0.7}As$ ($n_o = 10^{19}$ cm^{-3}, 5000 Å), GaAs (undoped, 1.1 μm), and $Al_{0.3}Ga_{0.7}As$ ($p_o = 2.5 \times 10^{17}$ cm^{-3}, 5000 Å). In order to achieve the 3-D electrical interconnect, a silicon circuit consisting of an 8 × 8 array of oscillators [shown in the photomicrograph in Fig. 5(a)] was spin-coated with a layer of polyimide and cured. Vias were dry etched in the polyimide using a reactive ion etcher to expose the underlying metal pads on the circuit. Ti/Au (150 Å/3000 Å) pads were then deposited onto the circuit to electrically connect the underlying circuit to the surface of the polyimide. The Ti/Au was then patterned into an 8 × 8 array of pads (100-μm pads spaced by 25 μm), with each pad centered over a via in the polyimide. These pads

served as the bottom contact for the photodetectors. This enabled the photodetectors to be integrated directly on top of the Si CMOS signal processing circuitry, enabling a high fill factor in the imaging array.

Prior to separating the detector epilayers from the GaAs substrate to create the thin film photodetectors, a p-type ohmic contact was deposited onto the structure and patterned into an 8×8 array pads. Using a selective wet chemical etch, the structure was mesa etched to a depth of 0.5 μm, with a 50 μm connecting bar of semiconductor left between each pixel. The entire array was then selectively mesa etched to the AlAs stop layer, separated from the substrate through a sacrificial etch of the AlAs layer in $HF:H_2O$ (1 : 10), and bonded to a transfer diaphragm. The connected array was then aligned over the Ti/Au pads on the circuit and contact bonded to the circuit, as shown in Fig. 5(b). To define 64 individual devices, the linking material was removed using $SiCl_4$ in the RIE, as shown in Fig. 5(c). A layer of polyimide was then spun on top of the circuit and cured to electrically isolate the bottom pads of the array from the top contacts. An 8×8 array of vias were etched in the polyimide using RIE, and a via was also opened over a common bias contact on the circuit for electrical connection of the common top contact of the detectors to the processing circuitry. A broad area n-type top contact was vacuum deposited on top of the array, and had 60 μm windows patterned over each device as windows to the detectors, as shown in Fig. 5(d). The circuit was then wire bonded into a standard 40-pin DIP package for testing.

The circuit integrated with the P-i-N photodetectors was an 8×8 array of current controlled oscillators fabricated in 2-μm CMOS by the MOSIS foundry. The core of the oscillator was a loop of three digital inverters, with one of the inverter's current limited through current mirrors controlled by the photodetector. The photodetector current regulated the switching speed of this inverter stage, which in turn regulated the frequency of the oscillator. The circuit output an oscillation frequency for each pixel which was a function of incident light intensity. There were approximately four different maximum value ranges of oscillating frequencies in the array, and the pixels followed a general trend in the slope of the frequency as a function of incident power [26]. Independent of the fact that the devices had a maximum oscillating frequencies in excess of 20 MHz, around 1–5 MHz, in the 100-KHz range, or under 100 KHz, the majority demonstrated seven decades (50 dB) of operation from 0-dB attenuation (maximum optical power input) to dark [26].

A smart pixel emitter array has also been fabricated using similar integration techniques with RCE LEDs heterogeneously integrated onto five-bit digital-to-analog converters used to provide adjustable drive current to the array of optical devices [27]. An 8×8 of RCE LEDs was bonded to the Si CMOS circuitry, which included 64 repeated cells in 2-μm CMOS in an 8×8 array, with each circuitry cell located underneath RCE LED pixel. This application demanded an extremely small circuit. Each cell included a five-bit DAC with a (five-bit) memory register, a two-input address decoder, a section of data bus, and an output current gain/driver stage. The size of each pixel was 416×416 μm. A photomicrograph of the several of the DAC/memory/address-decoder/output-driver cells is shown in Fig. 6, and the 8×8 array chip with 64 integrated infrared

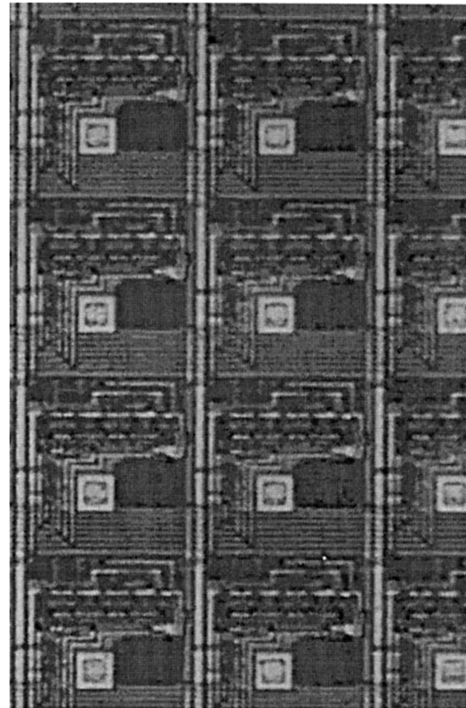

Fig. 6. Photomicrograph of several sections of the 8×8 grayscale circuit array.

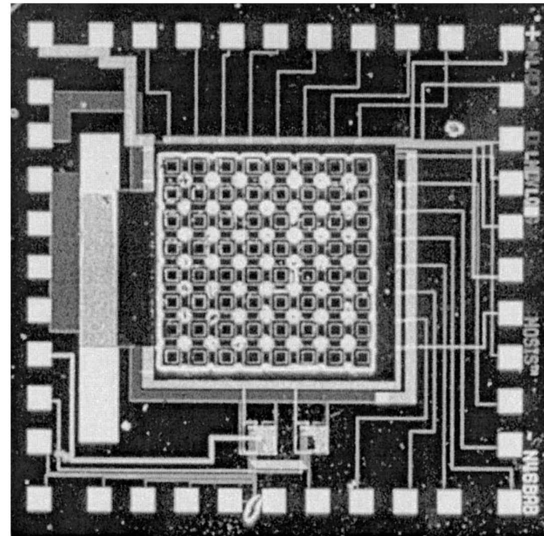

Fig. 7. Photomicrograph of the 8×8 array chip with integrated infrared LEDs.

LEDs on top of the circuitry is shown in Fig. 7. A photograph of the chip displaying a distinctive logo (a "GT" for the Georgia Institute of Technology, with the top of the T crossing the G) is presented in Fig. 8. Vertical cavity surface emitting lasers (VCSELs) have also been integrated onto host substrates using substrate removal and bonding techniques [40], and would also be prime candidates for thin film integration for smart pixel vertical interconnections.

An important aspect of thin film integration is the reliability of thin film devices bonded to host substrates. While each mixed material system must be evaluated separately, some indications of reliability can be gleaned from a few experiments. Lifetime testing of the metal-mirror RCE LEDs that were integrated onto

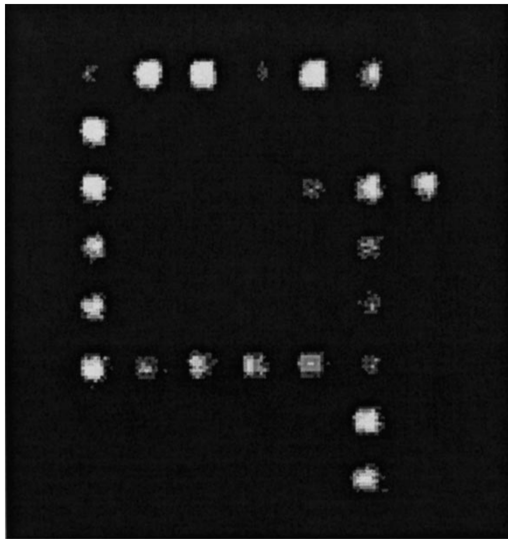

Fig. 8. Photograph of the 8 × 8 grayscale array displaying a Georgia Tech logo.

the DAC circuit has been completed on a limited number of devices [41]. The thin film metal-mirror RCE LEDs were bonded to silicon nitride-coated Si substrates and were driven with a square wave with a 100-μs pulse width at 25 mA. The output power of the devices increased steadily in the first 500 h of testing to 111% of the initial output power, which probably represents a burn-in of the contacts. The devices then leveled off to 107% of the initial output power, and varied by less than 1% for the remainder of the 5000 h test. The device did not fail at 5000 h, but the experiment was terminated at that time. The RCE LED spectrum did not change measurably during the 5000 h experiment.

V. Chip-to Chip-Optical Interconnections Using Thin Film Photodetectors Embedded in Waveguides

Removal of the growth substrate from integrated devices not only reduces the optical (absorption, scattering) and electrical (contact resistance) parasitics associated with the substrate, but also enables some unique heterogeneous integration implementations because the devices are on the order of microns thick. Three-dimensional stacking of emitters and detectors can be used for colocated, single fiber bidirectional links [14], [28], photodetectors with different wavelength sensitivities can be stacked 3-D for fully registered multispectral imaging [15], and thin film devices can be embedded in waveguide interconnections [29]. Although all of these examples are optical interconnections, we will focus on photodetectors embedded in waveguides for chip-to-chip optical interconnections.

Electrical boards, modules, and integrated circuits are essentially planar, and thus, planar waveguide optical interconnections match electrical interconnection substrates from a topographical standpoint. There are a variety of approaches to the partitioning of optical and electrical signals in a mixed electrical/optical interconnection system: 1) turn the optical beam out of the substrate into the OE active device or 2) keep the optical beam confined to the substrate, and embed the active OE device in the substrate. Optical beams can be turned 90 ° using mirrors or gratings, and can be turned into either optical/OE devices, or onto OEICs, such as those presented earlier in this paper. By employing diffractive optical elements, such as preferential gratings, high coupling efficiency and limited spectral selectivity can be achieved [30]. However, to emit or detect these outcoupled beams means that the active OE devices must operate facing the board/module/chip, in a flip chip orientation or as a flip chip OEIC. The drawbacks to this approach include the alignment constraints of the optical beam and decrease in coupling efficiency as the photodetectors decrease in size with increasing data rates.

Another approach is to have the optical signals originate and/or terminate in the waveguide directly on the board/module/chip, without optical beam turning. Optical interconnections with integrated waveguides and OE devices in a single substrate and epilayers [31]–[35] have been reported in compound semiconductors, such as InP-based materials, with reported high coupling efficiency and monolithic integration. However, the use of polymer waveguides and low-cost epoxy and polymer substrates is of great interest for optical interconnections in electrical interconnection systems, and thus, there is a research focus upon polymer waveguides for low-cost optical interconnections which are process compatible with current board, module, and integrated circuit technology. Polymer waveguides integrated onto Si [34] or GaAs [35], [36] electrical interconnection substrates with photodetectors fabricated in the substrate have been demonstrated. However, this approach does not accommodate epoxy and polymer substrates. An alternative embedded waveguide approach utilizes thin film OE devices, which can be bonded to any host substrate, including polymer and epoxy boards such as FR4. The polymer waveguide material can be deposited directly under and/or onto the thin film active OE devices, which are thus embedded directly into the waveguide.

Implementing these types of planar lightwave circuit (PLC) optical interconnections with embedded emitters and detectors may eliminate the need for optical beam turning elements which route the beam perpendicular to the surface of the board/module/chip for emission and detection interfaces. This embedded approach also reduces waveguide to active OE device optical alignment to a thin film device bonding/assembly step with sequentially aligned masking steps to integrate the waveguide and interface electronics, which mimics integrated circuit fabrication. In addition, the integration of additional PLC passive and further active embedded devices opens multiplexing and optical signal processing options for more complex microsystems. The assembly tradeoff that is inherent in the embedded optical waveguide interconnection is that the OE active devices are bonded directly to the substrate rather than bumped to the substrate. To minimize the impact of introducing optical interconnections into electrical interconnection substrates, the embedded OE waveguide interconnections can be integrated onto a fabricated electrical interconnection substrate through postprocessing. To enhance yield, the optical interconnections on the boards can be electrically tested before chipset integration.

Both evanescent and direct coupling can be implemented using this heterogeneous integration technology, if a thin film

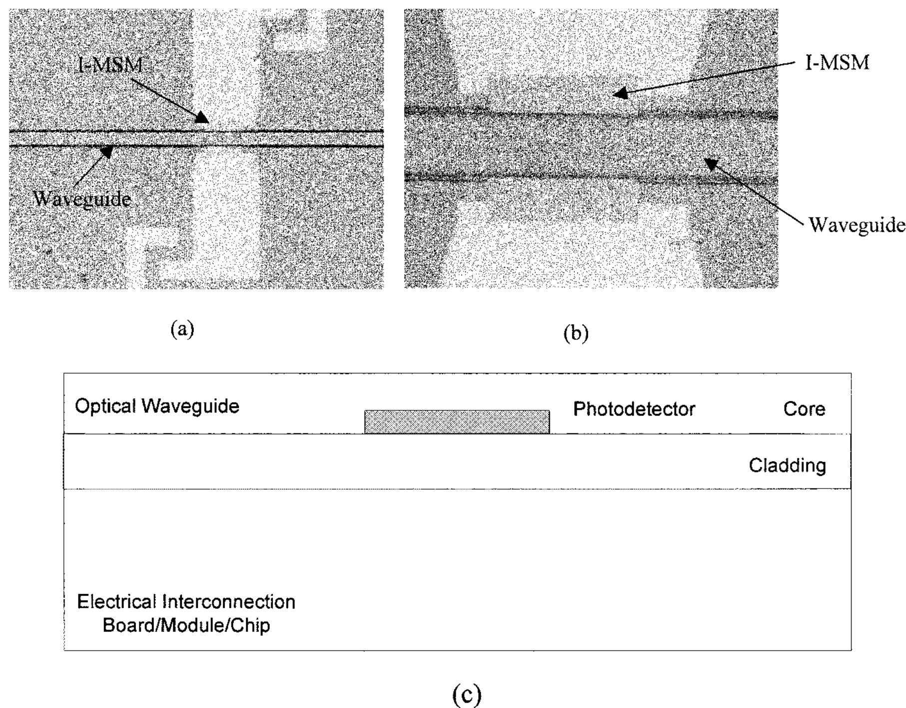

Fig. 9. Photomicrographs of (a) Fabricated I-MSM PD integrated with BCB polymer waveguide on a SiO_2-coated (3-μm-thick) silicon substrate, (b) closeup photomicrograph of 3(a), and (c) cross-sectional schematic of the I-MSM embedded in the polymer waveguide.

photodetector is embedded in the cladding or core of the waveguide, respectively. The integration processes described herein have been applied to Si substrates, and are also being applied to high-temperature epoxy FR4 boards. A number of configurations of embedded thin film photodetectors in polymer waveguides have been described [29]; herein will be presented the integration processes and measurement results for the integration of a thin film InGaAs PD embedded in a benzocyclobutene (BCB) polymer waveguides integrated onto a Si interconnection substrate.

The thin film InGaAs I-MSM photodetectors were fabricated and bonded to metal contacts on an SiO_2/Si substrate in the processing sequence previously described. The processing differences were that Schottky contacts of 40 Å Pt/350 Å Ti/400 Å Pt/2500 Å Au were deposited, and interdigitated fingers 100-μ m long with 2-μm-finger width and 2-μm-finger spacing were defined on a 100 $\times$ 150 μm detection area. The 400-Å-thick Pt layer acts as a diffusion barrier for the Au into the Ti during the polymer optical waveguide thermal curing process [37]. The final thickness of the MSMs was 0.9 μm. The thin film MSM photodetectors were transferred and bonded to contact pads of Ti/Au (400 Å/5000 Å), which were defined on the SiO_2-coated (3-μm-thick) silicon wafer. The 3-μm-thick SiO_2 layer on the Si wafer acts as a buffer layer for the waveguide. To increase the adhesion of the I-MSM to the pads, a 10-min 150 °C anneal was performed after the device was bonded to the contact pads.

The waveguide fabrication process was then performed to embed the photodetector between the Si substrate and the waveguide. BCB was used as the waveguide core layer, and was spin coated onto the I-MSM contact pad, resulting in a core layer thickness of 5.8 μm. A thermal cure was carried out in a nitrogen ambient to avoid oxidation of the BCB, since oxidization can slightly increase the refractive index of the film [38]. To minimize the scattering loss due to the surface roughness of the core layer, the core layer was chemimechanically polished using Rodel 3116B and deionized water. The abrasive used for the slurry was 0.05 μm Al_2O_3. The final thickness and surface roughness of the core layer were 3.9 μm, and 600 Å, respectively, as measured by a profilometer. The BCB planar waveguide was patterned into a 100-μm-wide channel waveguide using a photoresist mask and dry etching. The width of the fabricated waveguide was designed to match the detection area (100 $\times$ 150 μm) of the embedded I-MSM PD to maximize the coupling efficiency from the waveguide to the embedded PD. Fig. 9 shows the fabricated I-MSM PD embedded in the BCB polymer waveguide.

The I-MSM dark current and photoresponse were measured before and after waveguide fabrication, and the direct optical coupling was measured after the I-MSM was embedded in the waveguide. The I-MSM surface normal responsivity was measured before the waveguide was integrated onto the detector, and, without antireflective coating, had a measured responsivity of 0.38 A/W at 5 V. After the waveguide integration, to test the waveguide coupling, the Si substrate was cleaved to produce an endface on the polymer waveguide, and a single mode optical fiber was butt-coupled to the polymer waveguide endface. Fig. 10 shows the measured dark current before and after the polymer optical waveguide process, as well as the photocurrent due to the coupling from the waveguide the I-MSM PD embedded in the waveguide. The dark current, which is 2.7 nA at 5 V, improves slightly after the waveguide process, which may be due to the low-temperature annealing of the I-MSM Schottky contacts. The photocurrent at 5 V was 46.58 μA. Thus, the op-

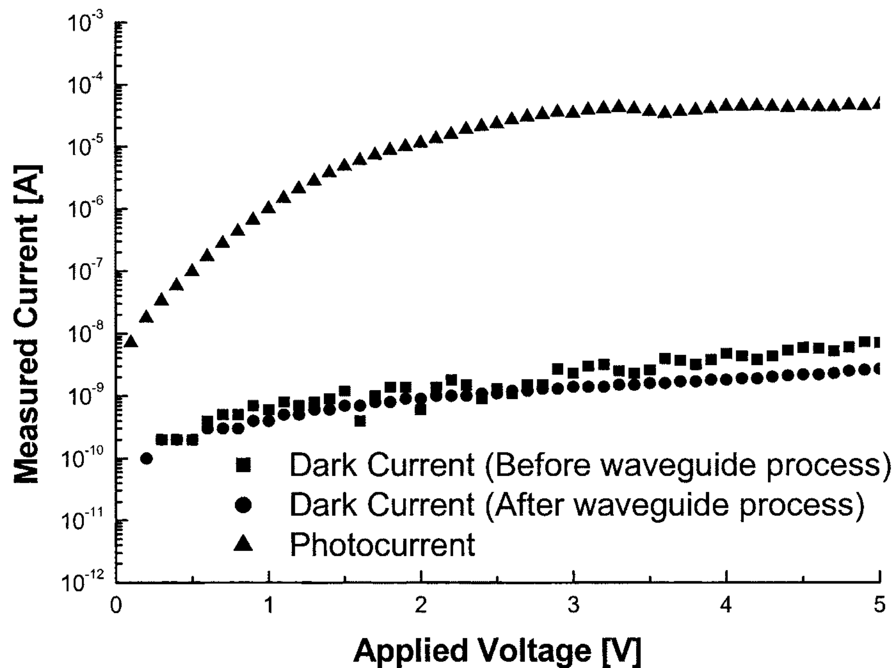

Fig. 10. Dark and photocurrent measurement of thin film I-MSM photodetector embedded in a polymer waveguide.

tical signal in the waveguide has been successfully coupled into the photodetector.

The coupling from the waveguide to the PD is difficult to estimate. The coupling from the waveguide into the embedded PD has been calculated for this structure, and this theoretical coupling is consistent with an estimate of the coupling through measurements. However, these measurements can only provide an inexact estimate due to the difficulty in estimating the fiber to waveguide endface coupling. The optical signal coupling efficiency was calculated for the embedded I-MSM PD and multimode waveguide structure based on the 2-D finite-difference beam propagation method (BPM). The high index contrast between the waveguide and the embedded I-MSM PD and the reflection at the embedded I-MSM PD interface was addressed using wide-angle and bidirectional BPM [39]. The estimated coupling efficiency from the 3.9-μm-thick multimode waveguide into the 150-μm-long embedded I-MSM PD was 59.4% using scalar wave analysis. The coupling efficiency from the waveguide to the embedded I-MSM PD was also grossly estimated based upon the experimentally measured coupling. The output from the input single mode optical fiber was 1.45 mW. Using 3-D scalar BPM, an estimated 16.7% of this optical signal is coupled into the waveguide. The optical signal travels 5 mm from the fiber input to the detector, which causes a loss of 0.18 dB. Thus, The estimated optical power at the input of embedded detector is 0.23 mW. Based upon the surface normal responsivity (0.38 A/W) and the photocurrent (46.58 μA) from the embedded photodetector when it is excited in the waveguide, it is possible to estimate that 0.12 mW of optical power is absorbed by the photodetector. Thus, the estimated coupling efficiency is 52.6%, which is on the same order of magnitude as the theoretical coupling efficiency. Although this estimate of the coupling efficiency is gross, it does indicate that sufficient coupling can be achieved to create a viable interconnect.

VI. Conclusion

Emerging heterogeneous integration techniques for integrating OE devices, analog interface circuitry, RF circuitry, and digital logic into ultra multisignal systems holds great promise for integrating optical interconnections into microsystems. As data rates dictate the use of optical interconnections and interfaces at increasingly smaller distances and higher data rates, to accommodate the speeds and desirable footprints of highly integrated systems, interfaces will become more integrated. Heterogeneous integration is one approach toward the integration of compound semiconductor OE devices, Si CMOS circuits, and organic materials such as polymers for waveguides and epoxies for printed circuit boards. Optical interconnections stand at a threshold of opportunity for pervasive implementation if cost-effective integration process technology and performance can be implemented into integrated microsystems.

Acknowledgment

The authors wish to thank the Microelectronics Research Center staff of the Georgia Institute of Technology, Atlanta, for their assistance with microfabrication, and DuPont for the donation of PI2611 polyimide.

References

[1] E. D. Kyriakis-Bitzaros, N. Haralabidis, M. Lagadas, A. Georgakilas, Y. Moisiadis, and G. Halkias, "Realistic end-to-end simulation of the optoelectronic links and comparison with the electrical interconnections for system-on-chip applications," *J. Lightwave Technol.*, vol. 19, pp. 1532–1542, Oct. 2001.

[2] W. Ryu, J. Lee, H. Kim, S. Ahn, N. Kim, B. Choi, D. Kam, and J. Kim, "RF interconnect for multi-Gbit/s board-level clock distribution," *IEEE Trans. Adv. Packag.*, vol. 23, pp. 398–407, Aug. 2000.

[3] D. A. B. Miller, "Rationale and challenges for optical interconnects to electronic chips," *Proc. IEEE*, vol. 88, pp. 728–749, June 2000.

[4] S. K. Tewksbury and L. A. Hornak, "Optical clock distribution in electronic systems," *J. VLSI Signal Process.*, vol. 16, pp. 225–246, 1997.

[5] M. Rassaian and M. W. Beranek, "Quantitative characterization of 96.5Sn3.5Ag and 80Au20Sn optical fiber solder bond joints on silicon micro-optical bench substrates," *IEEE Trans. Adv. Packag.*, vol. 22, pp. 86–93, Feb. 1999.
[6] S. J. Walker and J. Jahns, "Optical clock distribution using integrated free-space optics," *Opt. Commun.*, vol. 90, pp. 359–371, 1992.
[7] P. J. Delfyett, D. H. Hartman, and S. Z. Ahmad, "Optical clock distribution using a mode-locked semiconductor laser-diode system," *J. Lightwave Technol.*, vol. 9, pp. 1646–1649, Dec. 1991.
[8] L. Yujie, L. Lei, C. Chulchae, B. Bipin, and R. T. Chen, "Optoelectronic integration of polymer waveguide array and metal-semiconductor-metal photodetector through micromirror couplers," *IEEE Photon. Technol. Lett.*, vol. 13, pp. 355–357, Apr. 2001.
[9] Y. Liu, E. Strezelecka, J. Nohava, M. Hibbs-Brenner, and E. Towe, "Smart-pixel array technology for free-space optical interconnects," *Proc. IEEE*, vol. 88, pp. 764–768, June 2000.
[10] U. Gosele, Q.-Y. Tong, A. Schumacher, G. Krauter, M. Reiche, A. Plossl, P. Kopperschmidt, T.-H. Lee, and T.-H. Kim, "Wafer bonding for microsystems technologies," *Sensors and Actuators A (Physical)*, vol. A74, no. 1–3, p. 161, 1999.
[11] E. Yablonovitch, T. Gmitter, J. P. Harbison, and R. Bhat, "Extreme selectivity in the liftoff of epitaxial GaAs films," *Appl. Phys. Lett.*, vol. 51, pp. 2222–2224, 1987.
[12] N. M. Jokerst, M. A. Brooke, J. Laskar, D. S. Wills, A. S. Brown, M. Vrazel, S. Jung, Y. Joo, and J. J. Chang, "Microsystem optoelectronic integration for mixed multisignal systems," *IEEE J. Select. Topics Quantum Electron.*, vol. 6, pp. 1231–1239, Nov.–Dec. 2000.
[13] N. Jokerst, "Hybrid integrated optoelectronics: Thin film devices bonded to host substrates," *Int. J. High-Speed Electron. Syst.*, vol. 8, no. 2, pp. 325–356 , 1997.
[14] D. L. Geddis and N. M. Jokerst, "Co-located stacked thin-film bi-directional devices," in *Proc. IEEE Conf. Lasers and Electro-Optics*, Long Beach, CA, May 2002, pp. 138–139.
[15] S. Seo, D. Geddis, N. Jokerst, and M. Brooke, "Stacked thin film InGaAs and GaAs photodetectors for fully registered wavelength discrimination," in *Proc. IEEE Lasers and Electro-Optics Society Annu. Meeting*, Glasgow, Scotland, Nov. 2002, pp. 841–842.
[16] J. H. Kim, H. T. Griem, R. A. Friedman, E. Y. Chan, and S. Ray, "High-performance back-illuminated InGaAs/InAlAs MSM photodetector with a record responsivity of 0.96 A/W," *IEEE Photon. Technol. Lett.*, vol. 4, pp. 1241–1244, 1992.
[17] I. Adesida, J. W. Seo, W. Wohlmuth, C. Caneau, and R. Bhat, "Long wavelength metal-semiconductor-metal photodetectors with Ti/Au and indium-tin-oxide electrodes," in *Proc. 6th Int. Conf. Indium Phosphide and Related Materials*, 1994, pp. 284–287.
[18] O. Vendier, N. M. Jokerst, and R. Leavitt, "High performance thin film inverted MSM Photodetectors," *IEEE Photon. Technol. Lett.*, vol. 8, pp. 266–268, Feb. 1996.
[19] M. Vrazel, J. J. Chang, I.-D. Song, K. Chung, M. Brooke, N. M. Jokerst, A. Brown, and D. S. Wills, "Highly alignment tolerant InGaAs inverted MSM photodetector heterogeneously integrated on a differential Si CMOS receiver operating at 1 Gbps," in *Proc. 51st Electron. Components and Technol. Conf.*, 2001, pp. 8–13.
[20] J. J. Chang, S. Jung, M. Vrazel, K. Jung, M. Lee, M. A. Brooke, and N. Jokerst, "Hybrid optically interconnected microprocessor: An InP I-MSM integrated onto a mixed-signal CMOS analog/microprocessor IC," *Proc. Int. Soc. Opt. Eng.*, vol. 4089, pp. 708–714, 2000.
[21] Y. Joo, S. Fike, K. S. Chung, M. Brooke, N. M. Jokerst, and D. S. Wills, "Application of massively parallel processors to real time processing of high speed images," in *Proc. 4th Int. Conf. Massively Parallel Process. Using Opt. Interconnect.*, Montreal, Canada, June 22–24, 1997, pp. 96–100.
[22] S. M. Chai, A. Lopez-Lagunas, D. S. Wills, N. M. Jokerst, and M. A. Brooke, "Systolic processing architectures using optoelectronic interconnects," in *Proc. 4th Int. Conf. Massively Parallel Process. Using Opt. Interconnect.*, Montreal, Canada, June 22–24, 1997, pp. 160–166.
[23] M. Lee, "A quasimonolithic optical receiver using a standard digital CMOS technology," Ph.D. dissertation, School of Elect. Comput. Eng., Georgia Inst. Technol., Atlanta, 1996.
[24] K. Boustedt, "GHz flip chip-an overview," in *Proc. 48th Electron. Components and Technol. Conf.*, 1998, (Cat.CH 36 206), pp. 297–302.
[25] A. Krishnamoorthy and K. Goossen, "Optoelectronic-VLSI: Photonics integrated with VLSI circuits," *IEEE J. Select. Topics Quantum Electron.*, vol. 4, pp. 899–912, Nov.–Dec. 1998.
[26] S. Fike, B. Buchanan, N. M. Jokerst, M. Brooke, T. Morris, and S. DeWeerth, "8×8 array of thin film photodetectors vertically electrically interconnected to silicon xircuitry," *IEEE Photon. Technol. Lett.*, vol. 7, pp. 1168–1170, Oct. 1995.
[27] S. T. Wilkinson, J. Tabler, N. M. Jokerst, M. Brooke, and R. P. Leavitt, "An 8x8 array of resonant cavity enhanced light emitting diodes integrated onto silicon grayscale (32 level) driver circuitry," in *Proc. IEEE LEOS 9th Annu.*, vol. 2, 1996, pp. 277–278.
[28] J. Cross, B. Buchanan, L. Carastro, A. Lopez-Lagunas, A. Tony Wang, N. Jokerst, M. Brooke, S. Wills, and M. Ingram, "A single fiber bi-directional optical link using co-located emitters and detectors," *IEEE Photon. Technol. Lett.*, vol. 8, pp. 1385–1387, Oct. 1996.
[29] S. Cho and N. Jokerst, "Polymer waveguide optical interconnections for electrical interconnection substrates," in *Proc. IEEE Conf. Lasers and Electro-Optics*, Long Beach, CA, May 2002, pp. 161–162.
[30] S. M. Schultz, E. N. Glytsis, and T. K. Gaylord, "Volume grating preferential-order focusing waveguide coupler," *Opt. Lett.*, vol. 24, pp. 1708–1710, 1999.
[31] S. Kollakowski, A. Strittmatter, E. Dröge, E. H. Böttcher, and E. H. Bimberg, "65 GHz InGaAs/InAlGaAs/InP waveguide-integrated photodetectors for the 1.3-1.55 μm wavelength regime," *Appl. Phys. Lett.*, vol. 74, pp. 612–614, 1999.
[32] E. H. Böttcher, H. Pfitzenmaier, E. Dröge, S. Kollakkowski, A. Stittmatter, D. Bimberg, and R. Steingrüber, "Distributed waveguide-integrated InGaAs MSM Photodetectors for high-efficiency and ultra-wideband operation," in *Proc. IEEE 11th Int. Conf. Indium Phosphide and Related Materials*, 1999, pp. 79–82.
[33] R. T. Chen, L. Lin, C. C. Choi, Y. J. Liu, B. Bihari, L. Wu, S. Tang, R. Wickman, B. Picor, M. K. Hibbs-Brenner, J. Bristow, and Y. S. Liu, "Fully embedded board-level guided-wave optoelectronic interconnects," *Proc. IEEE*, vol. 88, pp. 780–793, 2000.
[34] C. H. Buchal, A. Roelofs, M. Siegert, and M. Löken, "Polymeric strip waveguides and their connection to very thin ultrafast metal-semiconductor-metal detectors," in *Proc. Mater. Res. Soc. Symp.*, vol. 597, 2000, pp. 97–102.
[35] F. Gouin, L. Robitaille, C. L. Callender, J. Noad, and C. Almeida, "A 4×4 optoelectronic switch matrix integrating an MSM array with polyimide optical waveguides," *Proc. SPIE*, vol. 3290, pp. 287–295, 1997.
[36] C. L. Callender, L. Robitaille, J. P. Noad, F. Gouin, and C. Almeida, "Optimization of metal-semiconductor-metal (MSM) photodetector arrays integrated with polyimide waveguides," *Proc. SPIE*, vol. 2918, pp. 211–221, 1997.
[37] D. G. Ivey, P. Jian, R. Bruce, and G. Knight, "Microstructural analysis of Au/Pt/Ti contacts to p-type InGaAs," *J. Mater. Sci.: Mater. Electron.*, vol. 6, pp. 219–227, 1995.
[38] R. Kirchoff, C. Carriere, K. Bruza, N. Rondan, and R. Sammler, "Benzocyclobutenes: A new class of high performance polymer," *J. Macro. Sci.-Chem.*, vol. 28, pp. 1079–1113, 1991.
[39] G. Fischbeck, R. Moosburger, M. Topper, and K. Peterman, "Design concept for singlemode polymer waveguides," *Electron. Lett.*, vol. 32, pp. 212–213, 1996.
[40] H. Fathollahnejad, D. Amthine, R. Droopad, G. Maracas, and S. Daryanani, *Electron. Lett.*, vol. 30, no. 15, pp. 1235–1236, 1994.
[41] S. T. Wilkinson, "Resonant cavity photonic devices for optical interconnects," Ph.D. dissertation, School of Elect. and Comput. Eng., Georgia Inst. Technol., Atlanta, Aug. 1996.

Nan Marie Jokerst (S'83–M'88–SM'98–F'02) received the Ph.D. degree from the University of Southern California, Los Angeles, in 1989.

She joined the Electrical Engineering faculty of the Georgia Institute of Technology, Atlanta, in 1989, where she is currently the Joseph M. Pettit Professor of Optoelectronics in the School of Electrical and Computer Engineering and the Optoelectronics Thrust Leader for the National Science Foundation Engineering Research Center in Electronic Packaging. She has published and presented over 175 papers, three book chapters, and holds three patents and has two pending.

Prof. Jokerst has organized and served on numerous conference committees and has served on the Board of Directors of the Optical Society of America as the Chair of the Engineering Council, and on the IEEE Lasers and Electro-Optic Society (LEOS) Board of Governors as an Elected Member, and as the Vice President of Conferences for IEEE LEOS. She has also served as the Elected Chair, Vice Chair, Secretary, and Treasurer of the Atlanta IEEE Section. She received an IEEE Millennium Medal in 2000, the Harriet B. Rigas Education Award from the IEEE Education Society, a DuPont Young Faculty Award, a National Science Foundation Presidential Young Investigator Award, Newport Research Award, and three teaching awards, and she was a Hewlett Packard Fellow. She is an Optical Society of America Fellow.

Martin A. Brooke (S'85–M'86) received the B.E. degree (first class honors) from Auckland University, Auckland, New Zealand, in 1981 and the M.S. and Ph.D. degrees in electrical engineering from the University of Southern California, Los Angeles, in 1984 and 1988, respectively.

He is currently an Associate Professor of Electrical Engineering at the Georgia Institute of Technology, Atlanta. He holds four U.S. patents. He has published more than 100 articles in technical journals and proceedings, and articles on his work have appeared in several trade publications. His expertise is in high-speed, high-performance signal processing. Current projects he is involved with include learning neural network hardware development, neural network prediction of turbulent flow, focal plane image processing hardware development, 1–20 Gbps digital CMOS transceiver circuits for low-cost fiber optic communication, nonlinear filtering algorithms for telecommunications, nonlinear analog to digital converter design, accurate modeling of high-speed circuit parasitics, and statistically relevant device models for accurate prediction of high performance integrated circuit yield.

Professor Brooke won a National Science Foundation Research Initiation Award in 1990, the 1992 IEEE Midwest Symposium on Circuits and Systems Myril B. Reed Best Paper Award, and the 2003 Institute Best Thesis Advisor Award from Georgia Tech.

Sang-Yeon Cho received the B.S. and M.S. degrees in electrical and computer engineering from SungKyunKwan University, Seoul, Korea, in 1997 and 1998 respectively, and the M.S.E.C.E. degree in 2000, from the Georgia institute of Technology, Atlanta, where he is currently pursuing the Ph.D. degree.

His research interest is in high-speed optical interconnection using thin film active OE devices with polymer optical waveguides.

Scott Wilkinson, photograph and biography not available at time of publication.

Michael Vrazel received the B.S. degree in physics from the University of Alabama, Tuscaloosa, in 1997 and the M.S. degree in electrical engineering in 2000 from the Georgia Institute of Technology, Atlanta, where he is currently pursuing the Ph.D. degree.

His area of research is in high-speed alignment tolerant OE devices.

Suzanne Fike, photograph and biography not available at time of publication.

John Tabler, photograph and biography not available at time of publication.

Yoong Joon Joo, photograph and biography not available at time of publication.

Sang-Woo Seo received the B.S. degree in electrical and computer engineering from Ajou University, Suwon, Korea, in 1997 and the M.S. degree from the Kwangju Institute of Science and Technology (KJIST), Gwangju, Korea, in 1999. He is currently pursuing the Ph.D. degree at the Georgia Institute of Technology, Atlanta.

He has experience in semiconductor laser devices at KJIST and his current main interest is the development of thin film detectors for multispectral imaging and high-speed optical interconnections.

D. Scott Wills, Kwangju Institute of Science and Technology.

April Brown, Kwangju Institute of Science and Technology.