The High-Mobility Bended n-Channel Silicon Nanowire Transistor

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***Abstract*—This work demonstrates a method for incorporating strain in silicon nanowire gate-all-around (GAA) n-MOSFETs by oxidation-induced bending of the nanowire channel and reports on the resulting improvement in device performance. The variation in strain measured during processing is discussed. The strain profile in silicon nanowires is evaluated by Raman spectroscopy both before device gate stack fabrication (tensile strains of up to 2.5% are measured) and by measurement through the polysilicon gate on completed electrically characterized devices. Drain current boosting in bended n-channels is investigated as a function of the transistor operation regime, and it is shown that the enhancement depends on the effective electrical field. The maximum observed electron mobility enhancement is on the order of 100% for a gate bias near the threshold voltage. Measurements of stress through the full gate stack and experimental device characteristics of the same transistor reveal a stress of 600 MPa and corresponding improvements of the normalized drain current, normalized transconductance, and low-field mobility by 34% (at maximum gate overdrive), 50% (at $g_{\max}$), and 53%, respectively, compared with a reference nonstrained device at room temperature. Finally, it is found that, at low temperatures, the low-field mobility is much higher in bended devices, compared with nonbended devices.**

***Index Terms*—Micro-Raman spectroscopy, mobility, multiple-gate MOSFET, silicon nanowire, strained Si.**

I. Introduction

TOP-DOWN fabricated silicon nanowire MOSFETs are of great interest as the future building blocks of electronic circuits. The superior electrostatic control of the gate in gate-all-around (GAA) architectures of nanowire MOSFETs results in better control of short-channel effects, compared with bulk, single-gate, and double-gate silicon-on-insulator (SOI) devices, thus making nanowires intrinsically more scalable than their planar counterparts. In addition, nanowires have been found to possess superior mechanical [1] and electrical properties [2], compared to bulk silicon, as a result of their confined dimensions.

At the same time, CMOS technology has experienced enormous progress over the past few decades, first by dimensional scaling and, more recently, by the introduction of novel materials and strain engineering, which improve device performance [3]. In order for nanowire devices to achieve their full potential, it should also be possible to take advantage of the innovations made for planar devices, such as strain, but this is not a trivial task, because their processing, metrology, and experimental behavior could be significantly different. In this work, we demonstrate how electron mobility can locally be enhanced in the GAA MOSFET channel by oxidation-induced bending, which introduces tensile strain in the channel.

In Section II, we briefly describe device fabrication. Then, in Section III, we discuss the influence of strain on carrier mobility, both in general terms and specific to this work. In Section IV, we present strain measurements using Raman spectroscopy and analyze the stress profiles obtained in devices both before and after gate stack deposition. The electrical characteristics of nanowire devices are shown in Section V. Device mobility enhancement is presented in Section VI, and the temperature behavior of the GAA nanowire devices is discussed in Section VII. Finally, a short discussion and the paper conclusions follow in Section VIII.

II. Device Fabrication

Fabricating 3-D devices is more challenging than planar structures, because it requires control of processing in three dimensions. In addition, process metrology is more difficult since it is no longer possible to monitor processing by simply observing the planar surface of the wafer.

In this paper, the devices are fabricated using a top-down technology, in which nanowire capability is achieved by smart processing, i.e., a hard mask spacer technology combined with isotropic etching and a series of sacrificial oxidation steps. A simplified schematic of the process flow, following initial wire creation and including the oxidation-induced bending, is shown in Fig. 1(a). An illustration of the process flow using cross sections is shown in Fig. 1(b), suggesting the possibility of obtaining both triangular and pentagonal cross sections. Fig. 1(c)–(e) shows fabricated triangular, pentagonal, and

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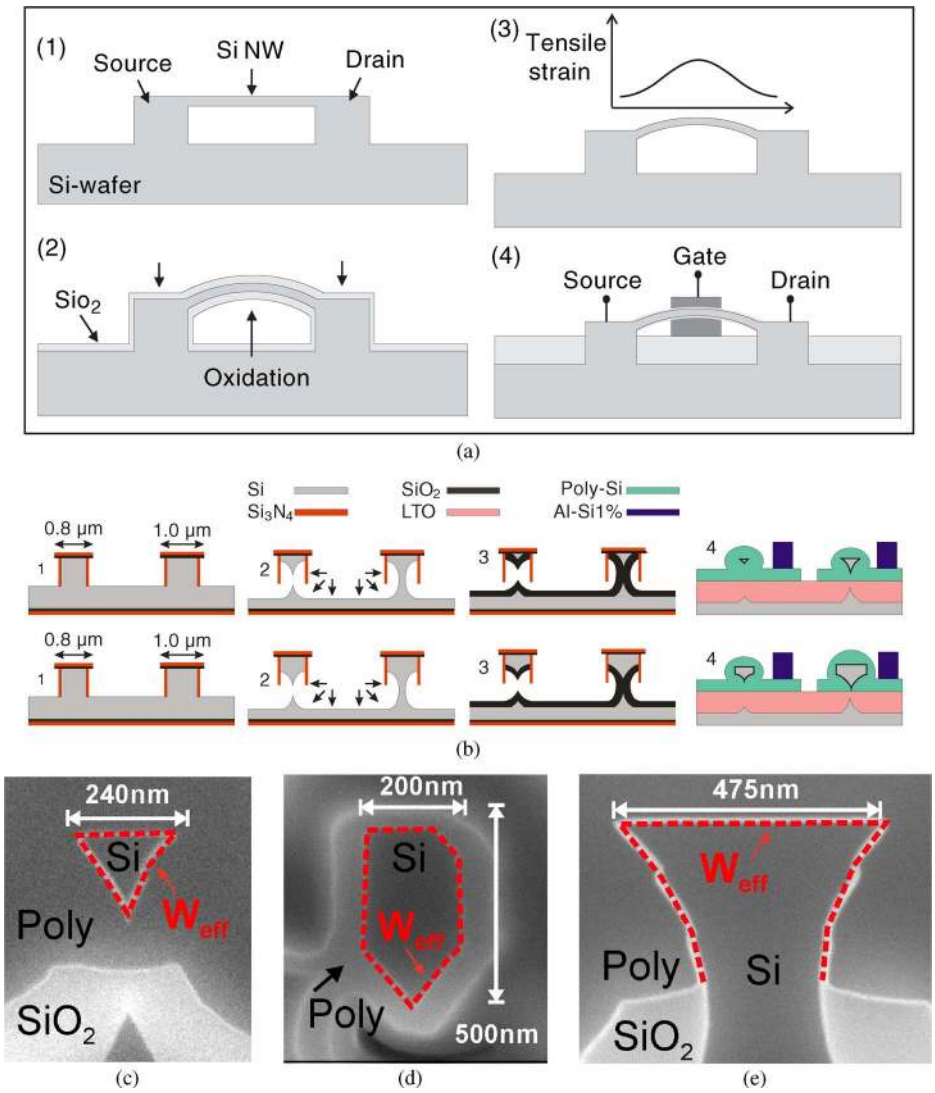

Fig. 1. (a) Schematic of the part of the process flow showing 1) a silicon nanowire suspended between source and drain, 2) bending of the nanowire by thermal oxidation, 3) bending and, hence, strain remains after oxide removal, and 4) local-SOI fabrication by low-temperature oxide (LTO) deposition and etch-back, followed by gate stack formation, implantation, and activation. Not shown are isolation and metallization steps. (b) Successive cross sections during fabrication showing that, depending on the top designed width and depth of etching, the resulting cross section of the suspended silicon wires can be (top) triangular or (bottom) pentagonal. Three possible device cross sections resulting from our process, depending on the design width at the top: (c) triangular cross section, (d) pentagonal cross section, and (e) body-tied device (called nonbended and considered as a reference device in this work). Also shown is the measured effective channel width W_{eff} for each device.

body-tied cross sections. Top-view scanning electron microscope (SEM) images of fabricated bended nanowires and GAA device are shown in Fig. 2; the out-of-plane nanowire bending is clearly visible.

As shown in Fig. 1(b)–(d), depending on the designed wire dimensions and process parameters, on any given wafer, we will have some devices that are suspended and some devices that are still connected to the substrate. The suspended devices turn into bended GAA devices, whereas devices that remain connected to the substrate cannot become bended and instead become tri-gate (or nonbended) devices, which we use as control devices for the suspended GAA devices. More detailed information about the processing and, particularly, concerning the initial nanowire fabrication is available in [4].

Since, in this work, we are limited to a lithographic resolution of 0.8 μm, we use oxidation to shrink the dimensions of the device cross sections to the 100-nm range. Smaller devices having diameters of down to 5 nm have also been fabricated, but scattering and possibly quantization effects limit the mobility in these smallest devices; therefore, they are not included in the mobility study presented here and are reported elsewhere [5], [6]. Such nanowires with extremely small cross sections can be exploited for their low-temperature Coulomb blockade effects [5]. In addition to eliminating the need for expensive lithography setups, the oxidation step used to reduce dimensions also has the benefit of inducing large tensile strain in the nanowires, which remains after oxide removal, as evidenced by the visible bending of devices. This is discussed here.

A. Thermal Oxidation as Strain-Inducing Technique

The volume expansion of the oxide during thermal oxidation has long been known to induce strain in silicon, and this has been shown to enhance the transconductance [7] and mobility

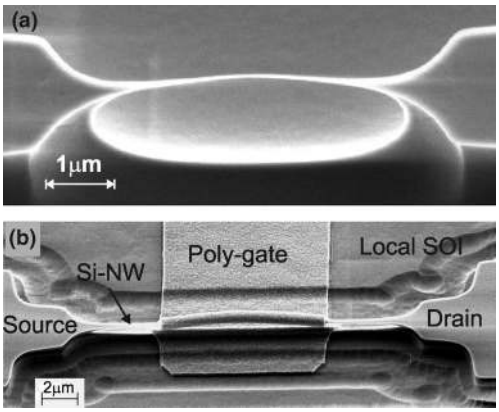

Fig. 2. (a) SEM image of a nanowire after oxide removal (naked nanowire), where the visible bending indicates strain in the wire. (b) GAA nanowire MOSFET, with the polysilicon gate still showing visible bending of the nanowire. The location of the different contact source, drain, and gate is indicated, although the isolation and metallization have not been completed yet.

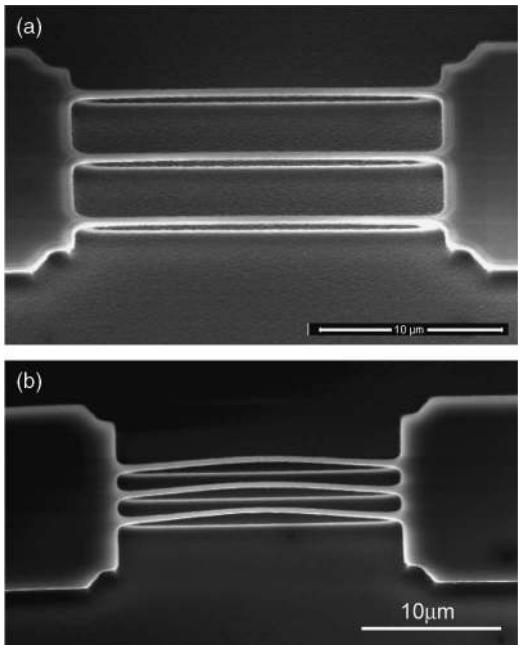

Fig. 3. SEM image of three parallel released silicon nanowires with a length of 20 μm. (a) Before thermal oxidation and (b) after thermal oxidation steps (the 110-nm thermal oxide is not removed from the wires in this image), showing local bending in both cases and good reproducibility of the process.

in silicon nanowires [8], [9]. Normally, one would expect a relaxation of the strain to take place once the straining oxide layer is removed; hence, most studies investigate the strain effects while maintaining the oxide.

However, in our case, we have observed that the wires are also visibly bent after oxide and hard mask removal [see Fig. 3(a)]. Recent works [10], [11] indicate that the major source of this strain after the stripping step is releasing the mechanical potential energy in the Si nanowire accumulated during oxidation because of restrictions on in-plane elongation and restrictions on out-of-plane buckling because of the tensile hard mask on top, causing in-plane elongation and out-of-plane bending of the Si nanowire during the stripping step and reaching up to 2.6 GPa of uniaxial tensile stress in the Si nanowire. It is worth mentioning that, according to our recent work [11], accumulation of temporary tensile stress was observed during suspension of the Si nanowires covered with a tensile hard mask on top and before the oxidation step due to possible relaxation of tensile stress in the tensile hard mask across the suspended Si nanowire and on the source–drain pads close to the anchor parts. This initial temporary stress significantly relaxes during heating of the wafer to the oxidation temperature, followed by thermal oxidation due to viscoelastic relaxation of stress in the thin films of the hard mask and geometrical reconfiguration of the Si nanowire during the oxidation step. During the stripping step, the source of this stress due to the tensile hard mask disappears and therefore cannot have any contribution in the final stress level of the Si nanowire after the stripping step.

Thermal-oxidation-induced strain in submicrometer single-crystal silicon beams fabricated on SIMOX substrates has been reported in [12], where the observed permanent bending of nanobeams was assumed to be associated with the injection of Si self-interstitial atoms during oxidation. It was also reported that the permanent buckling phenomenon and the related induced strain increase with a reduction in beam thickness. However, the reported strain values assume that the accumulation of tensile strain due to possible self-interstitial silicon atoms during oxidation apparently cannot exceed 0.012% [13]; therefore, this phenomenon by its own cannot explain the higher strain values obtained in our Si nanowires with a hard mask on top. The oxidation in this work was carried out at 1000 °C, although such high temperatures are not optimal for strain enhancement as certain viscoelastic relaxation is expected [7]. For future strain enhancement engineering, thermal oxidation should be performed below the glass transition temperature of SiO_2 (960 °C) to avoid such viscoelastic relaxation. It is worth noting that a systematic study of the bending process control and variability is out of the scope of this paper. Fig. 3(b) shows three parallel bended nanowires just after oxidation (without removing the oxide layer) and suggests that significant wire bending in micrometer-long nanowires is possible and locally reproducible. In conclusion, we consider that the tensile strain-building mechanism in the reported structures is very complex. Its evaluation and engineering should take into account the role of possible self-interstitial silicon atoms during oxidation, the possible superplastic deformation, and the release of potential energy accumulated in clamped–clamped silicon beams (including the role of the hard mask used to protect the released structures).

B. Scalability of the Proposed Technique

In this paper, long Si nanowires fabricated using a bulk platform were used to demonstrate validation of the local oxidation technique to induce local tensile strain in the suspended channels. This technology, as described in detail in [11], can be scaled down to provide, e.g., 1-μm-long, 10-nm-wide, and 10-nm-thick suspended uniaxially tensile strained Si nanowires using an SOI platform. Submicrometer gate lengths could be achieved with more advanced lithography; however, the use of such local SOI technique by isotropic etching has practical limits in terms of device pitch, control, and aspect ratio of the released (suspended) structures.

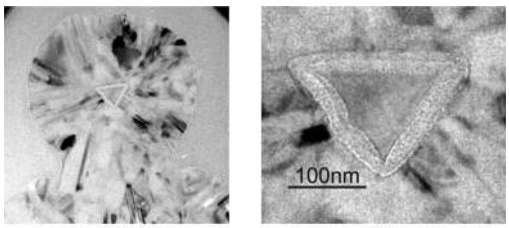

Fig. 4. (a) Transmission electron microscopy image of a GAA MOSFET through the channel, showing the full device, where the polysilicon gate is visible. (b) Zoom on the silicon nanowire core showing that the difference in oxidation rate along the various different crystal planes gives a variation in gate oxide thickness.

III. Strain as Booster of Carrier Mobility

The deformation of the silicon lattice caused by stress influences the band structure of silicon; a shift of the band positions can influence the respective band population and scattering rates, whereas the effective carrier mass is directly related to the band curvature.

Depending on the carrier type, the crystalline direction of silicon, and the type of strain, the lattice deformation can either lead to an improvement or a deterioration of the transport properties. Thus, strain engineering is used to enhance the performance of both n-channel MOS and p-channel MOS devices in modern CMOS nodes below 90 nm [14], [15]. For planar devices and SOI, there has been extensive research on the effects of strain as a performance booster [16]–[19], and recently, this interest has extended to silicon nanowires [12], [20]. Uniaxial compressive strain is found to enhance performance in silicon nanowire pMOSFETs in [21], whereas uniaxial tensile strain enhancement is used as a booster for tri-gate nMOSFETs [22].

For most industrial strain technologies, there is no systematic correlation of the dependence of the performance enhancement as a function of the amount of strain, simply because, for process-induced strain, it is not possible to arbitrarily vary the amount of strain. Mechanical die bending is a practical method that is often used to obtain such a correlation between performance and strain as it allows for a gradual variation of the strain in the wire.

This method is used in [2], where He and Yang presented the giant piezoresistance effect in silicon nanowires, which were found to be about two orders of magnitude larger than that for bulk silicon, with larger piezoresistance found for decreasing dimension and p-type doping. The accuracy of the method is questioned in [23]; however, the interest in strained silicon nanowires as the building block of future electronic circuits is as keen as ever. In addition, the points raised in [23] should not influence our result as we have good ohmic contacts at both source and drain, and we are directly evaluating the low-field mobility in the MOSFET inversion layer.

For nMOSFETs, uniaxial $\langle 110 \rangle$ and biaxial tensile strain are found to be particularly efficient [24], [25]. In this work, channels are all aligned along the $\langle 110 \rangle$ direction on a (100) wafer, so this is the orientation of the top channel of the triangular cross section. The two underlying concave side channels (see Fig. 4), however, do not have a well defined crystal orientation.

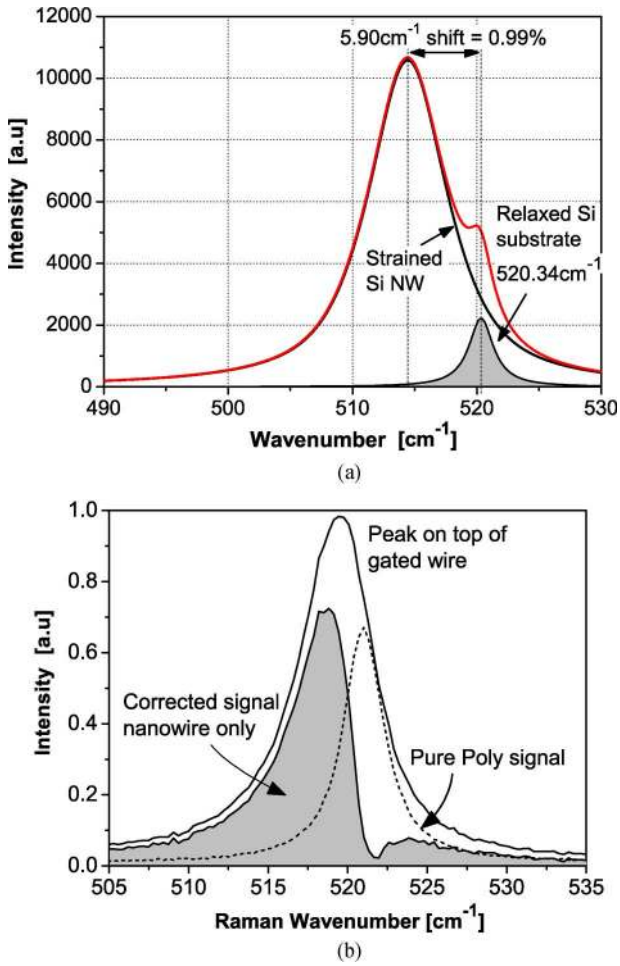

Fig. 5. (a) Typical Raman intensity profile showing how the spectra measured on the nanowire are a superposition of the signals from the strained nanowire and the underlying bulk silicon substrate. (b) Extraction of the wire signal (gray filling) from the combined spectrum of the wire and (solid line) polysilicon measured on top of the wire and (dotted line) the pure polysilicon signal measured on the flat wafer.

IV. Strain Measurements

For this study, a Raman spectrograph HR was used. Strain analysis by Raman spectroscopy relies on the sensitivity of the Raman peak position to strain (see Fig. 5). Thus, a shift in the Raman peak from the sample can directly be related to the residual or applied strain. The position of the nanowire peak with respect to a nonstressed sample (e.g., the bulk Si substrate) indicates the nature of the strain, tensile strain causes a downshift of the peak, and a compressive strain will shift the Raman peak toward larger wavenumbers.

The area maps and line scans along and across the nanowires and devices were carried out, and the resulting spectra were analyzed in order to accurately determine the strain. The step size between adjacent measurements is critical in determining spatial resolution. In our measurements, a step size of 100 nm was used. Raman data were converted to absolute values of strain using phonon deformation potentials [26].

The conversions used are

$$\text{Stress [GPa]} = \text{Shift}/4.596\ \text{cm}^{-1}$$

$$\text{Strain} = \text{Stress [GPa]}/169\ \text{GPa}.$$

The peak fitting of both naked nanowires and wires with a gate stack is carried out using a special software developed for the deconvolution and peak fitting of spectral features. The calibrated peak-fitting process enables a minimal error of < 0.07 cm^{-1} (corresponding to 15 MPa) in the measurements of naked nanowires.

A bulk silicon peak may show in the same spectrum as the nanowires if the nanowire is much thinner than the laser penetration depth or if the laser spot simultaneously illuminates both the wire edge and the unstrained Si substrate. The result is a combined spectrum of two peaks, and the shift separating them is proportional to the strain in the nanowire [27], [28]. Nonstrained nanowires do not exhibit a shift from the bulk Si position.

For the strain measurement on naked silicon nanowires (prior to gate stack formation), an excitation source of 514.5 nm was used. This has a penetration depth of approximately 760 nm in silicon and enabled the Raman signal from within the nanowire to be distinguished from that of the surrounding material.

Strain evaluation in silicon nanowires, following gate stack formation, is more complicated. In addition to the strained nanowire and relaxed silicon substrate, there is a contribution to the Raman spectra of thick polysilicon and thin silicon oxide layers. The effect of the oxide layer can usually be neglected as it is almost transparent and it is thin. However, the effect of the polysilicon layer can be challenging for strain evaluation. The first major factor is the polysilicon thickness, which places restrictions on the laser wavelength that can be used. Since the polysilicon layer is about 500 nm thick, the laser wavelength must be higher than 514 nm in order to penetrate through the polysilicon and reach the nanowire. Therefore, for processed devices, a 632-nm laser was used to measure strain in the nanowire. Fig. 5(b) compares the spectrum from a processed device with a polysilicon gate stack with that obtained from polysilicon alone, which was measured away from the nanowire region. The signal for strain in the nanowire (filled gray curve) was calculated by subtracting the contribution of the polysilicon from the combined spectrum. Due to the increased diameter of the wire, once the gate stack is deposited, there is no substrate peak observed in the combined spectrum for the wire and the gate stack.

The polysilicon uniformity and structure further complicates strain characterization in nanowires with processed gate stacks. Due to the mixture of different grain sizes and various defects, the peak shape and peak position often differ from those of single-crystal silicon, which is 520.7 cm^{-1}. The polysilicon Raman spectrum is characterized by a larger full-width at half-maximum and lower intensity than those of the single-crystal silicon and has its peak position determined by deposition conditions [26]. This increases the error in identifying the peak position of Raman measurements in actual devices and is a particular problem for low values of strain in the nanowires.

In [9], Raman measurements confirmed the presence of high tensile strain in oxidized silicon nanowires after oxide removal; these results are shown in Fig. 6, which is a combination of measurements and statistical analysis. Typical measured strain values were about 1%, and the highest actual measurement was ~2.5% (4 GPa). Greater stress was present in some of the longer wires, but these would break when exposed to the laser light before a measurement could be completed. This may be due to laser heating of the highly stressed NW or may also result from defects in the wire. A stress/strain profile measured along a 20-μm-long suspended nanowire is shown in Fig. 7.

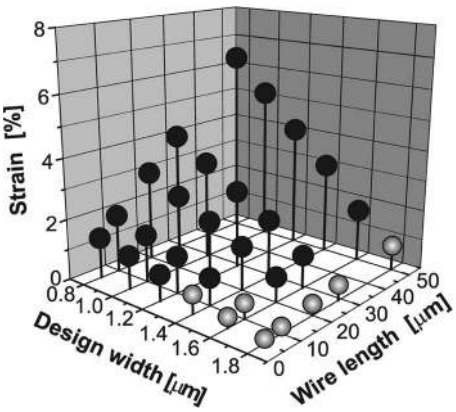

Fig. 6. Strain dependence on nanowire length L from 5 to 50 μm and on the designed (lithographic) widths measured on pentagonal wires after oxide removal and before gate stack creation. Gray circles correspond to wires that are probably not suspended, so measurements correspond to residual stress in corners.

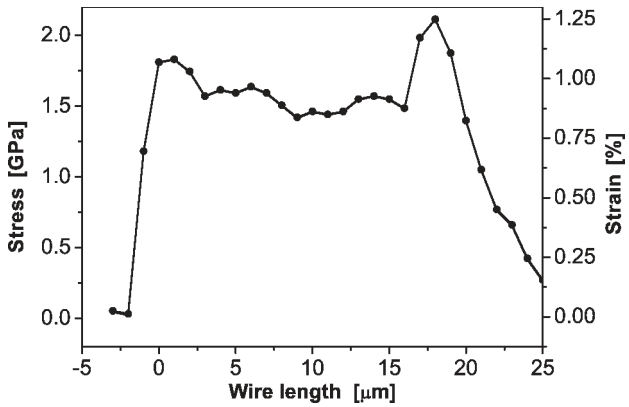

Fig. 7. Stress/strain profile before the gate stack measured in a 20-μm-long nanowire.

The results shown in Figs. 7 and 8 were measured on pentagonal nanowires without the gate stack, whereas the actual nanowires on which we performed the electrical characterization had triangular cross sections. The current work aims to correlate the stress profile and performance enhancement while providing a deeper understanding of these effects. Therefore, we have measured the strain profile (Fig. 8) and electrical characteristics (Fig. 9) in two triangular devices, one of which is bended, i.e., strained, and one of which is nonbended.

The lower strain values observed in the measurements through the polysilicon gate may be a result of some strain relaxation taking place in the final process steps, the most notable of which is the high-temperature (1050 °C) gate oxide growth. It signifies that even higher levels of enhancement should be obtainable if the strain relaxation can be reduced. Furthermore, the bended device in Fig. 8 is relatively large, so even greater levels of strain should be expected in smaller cross-sectional devices.

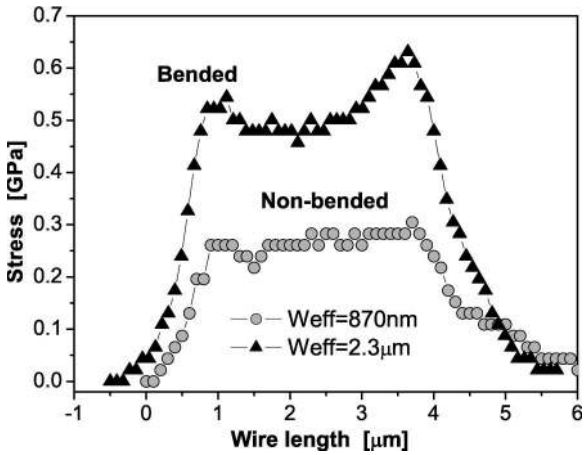

Fig. 8. Stress profiles measured through the full polysilicon gate stack in two 5-μm-long devices, whose electrical characteristics are shown in Figs. 9 and 10. The stress level measured in this full-processed GAA device is smaller than the levels measured in the longer suspended nanowires reported in Fig. 7. The measured strain can be derived using the following equation: strain = stress [GPa]/169 GPa.

In Fig. 8, we also observe a fairly high level of strain in the nonbended device, which ought to be nonstrained. We believe this to be due to the strain in the sharp corners of the device and may also be influenced by the polysilicon signal.

V. Electrical Characterization

The devices were measured by wafer probe testing. Room- and high-temperature dc measurements were carried out using a Microtech Cascade probe station and an HP 4155B semiconductor parameter analyzer, whereas the low-temperature measurements were carried out in a Süss MicroTec PMC 150 probe system.

The $I_D(V_{GS})$ characteristics of the same two devices on which strain measurements were carried out are shown in Fig. 9(a), and the corresponding current enhancement is shown in Fig. 10. The enhancement in I_D reaches a maximum of $\sim$160% close to the device threshold voltage V_T and becomes $\sim$38% at maximum gate voltage overdrive ($V_G - V_T = 1.5$ V). However, it should be noted that the exact enhancement value in this region is critically dependent on the value of V_T for each curve; therefore, any variation in V_T extraction is mirrored in a strong modification of the maximum enhancement near threshold. For the linear strong inversion part of the curve, a slight variation of the threshold voltage is not important; in this region, the enhancement is seen to slowly decrease as the gate bias increases. In general, we observe that the enhancement is inversely proportional to the effective field, i.e., the greater the effective field, the lower the enhancement. Fig. 9(b) reports the normalized transconductance enhancement versus the gate overdrive $V_G - V_T$; a maximum improvement is confirmed in the bended channel near the threshold voltage. ($g_{\max}$ improvement is 50%.)

Fig. 11 shows the corresponding $I_D(V_{DS})$ enhancement curves for different levels of gate bias. The gain close to $V_{DS} = 0$ V is similar for all values of V_{GS} (all higher than 1 V; therefore, given that $V_T \sim 0$ V, this corresponds to the region $V_G - V_T > 1$ V in Fig. 10, where the improvement

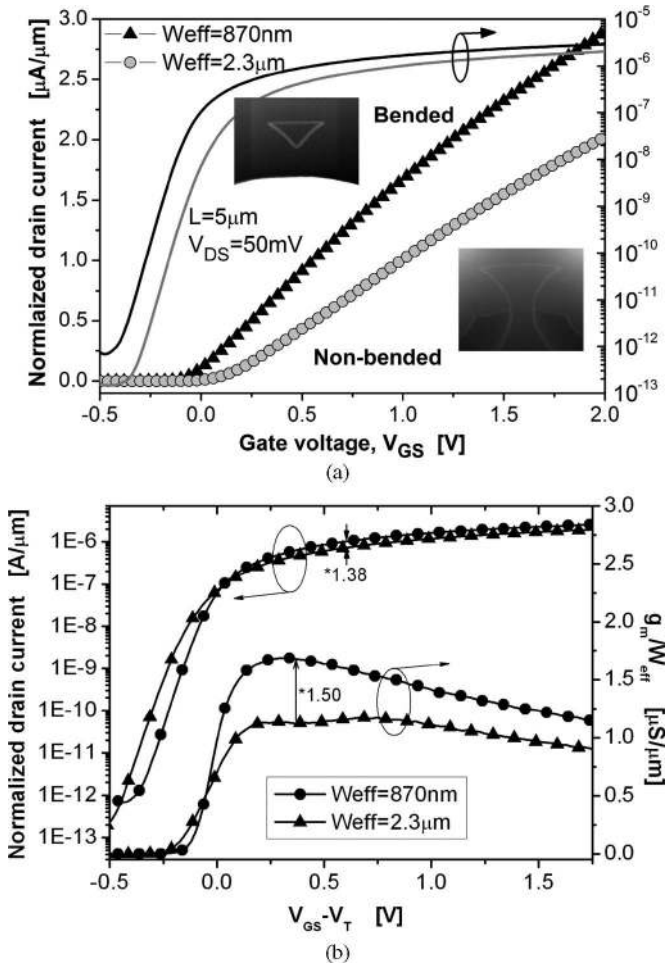

Fig. 9. (a) $I_D(V_{GS})$ characteristics of a bended and a nonbended MOSFET, the same devices for which the strain profiles are shown in Fig. 8. For the bended device, the extracted value of VT is -0.0384 V, and for the nonbended device, it is $+0.1525$ V. (b) Normalized transconductance $g_m(V_{GS} - V_T)$ for the same devices showing an improvement of 50% in the normalized $g_{\max}/W$ of the bended device, compared with that of the reference nonbended device. The inset of (a) shows the SEM images with cross sections of the measured devices that have been cut by focused ion beam (FIB), following electrical measurements. These SEM images serve to extract the width used to normalize the transconductance and extract the carrier mobility.

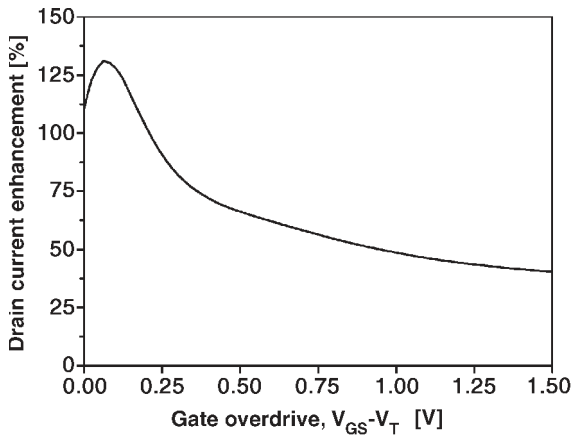

Fig. 10. Drain current enhancement as a function of gate overdrive for a bended device, compared with a nonbended device. The extraction is based on experimental data from Fig. 9.

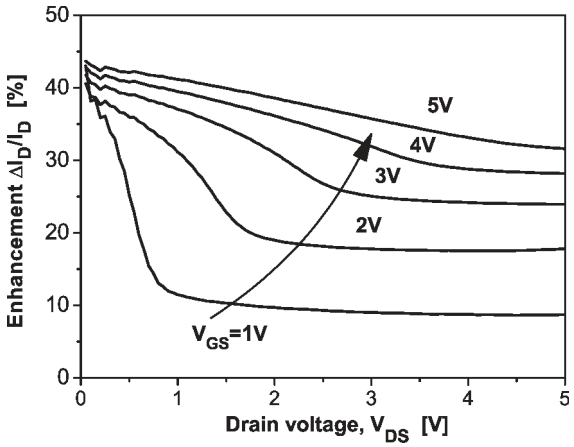

Fig. 11. Drain current enhancement curves for varying V_{GS}, all in strong inversion. The device effective widths for GAA and tri-gate are $W_{\rm eff} = 0.62$ μm and $W_{\rm eff} = 1.20$ μm; $L = 5$ μm for both devices. The tri-gate device serves as a reference for the evaluation of the current enhancement observed in the bended GAA device.

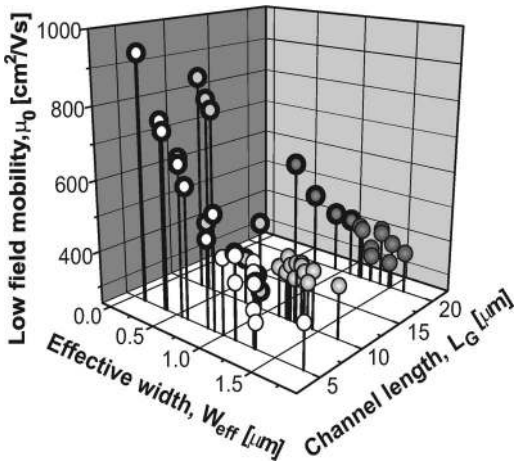

Fig. 12. Low-field mobility as a function of effective width for channel lengths of 5, 10, and 20 μm. Thick dark circles around measurement points indicate a bended GAA device.

saturates and is almost independent on V_G), and in the linear region, a strong dependence on V_{DS} and V_{GS} is observed. For all curves, the enhancement is almost constant (with V_{DS}) in the saturation region and increases with increasing V_{GS}. This can be understood from the drain current characteristics. In the linear region, I_D depends on both V_{GS} and V_{DS}, which is also the case for the enhancement characteristics, whereas, in the saturation region beyond pinchoff, the drain current is independent of V_{DS} and, hence, the constant strain sensitivity. The general increase in the strain enhancement with V_{GS} is due to the reduction in the effective field, as also confirmed by the experimental results reported by Vatedka *et al.* [29].

VI. Mobility Experimental Evaluation

The low-field mobility μ_0 is extracted by the $I_D/\sqrt{g_m}$ method [30], [31]. This method is particularly suited both because it allows for a separate extraction of the threshold voltage V_T and μ_0 and because it is quasi-independent of the series resistance. The low-field mobility is plotted as a function of effective width, i.e., the perimeter of the nanowire-gate dielectric interface, for three different gate lengths in Fig. 12. There is an important difference between the effective channel width $W_{\rm eff}$ of the measured transistors on which the mobility is extracted and the design width used in Fig. 6. A long wire with a design width of 1 μm will have a much smaller $W_{\rm eff}$ than a short wire with the same design width, as a result of the etching dynamics. This does not mean that the technology is not scalable, but that it needs to be taken into account in the design. Therefore, the strain data mapping from Fig. 6 cannot directly be correlated with the mobility results from Fig. 12, but it is worth noting that the devices showing smaller cross sections have systematically higher tensile strain and higher electron mobility. The channel length is also not necessarily limited by the wire length, which is practically defined by the distance between the two clamping regions.

For an accurate mobility extraction by method [30], a precise estimation of the oxide capacitance is needed. We have simulated the capacitance on equivalent GAA and tri-gate structures, and compared these to the theoretical expressions for a cylindrical and parallel plate capacitor, respectively. For the GAA structures, the expression for the cylindrical capacitance is more appropriate than that for a parallel plate, so we used this for the expression of $C_{\rm ox}$ for the small perimeter structures of $W_{\rm eff}$ less than approximately 600 nm.

For the smallest $W_{\rm eff}$, i.e., the bended GAA devices, we observe a sharp increase of about 100% in the low-field mobility, compared with the larger nonstrained tri-gate control devices. The highest extracted low-field mobility value is higher than 900 cm^2/V $\cdot$ s. This increase is explained by the large amount of strain measured in silicon nanowires. For comparison, for the device shown in Fig. 9(a) and (b), the low-field mobility enhancement is 53% (with an extracted value of 600 cm^2/V $\cdot$ s), which corresponds to a measured tensile stress level through the gate stack of $\sim$0.6 GPa. If we suppose a quasi-linear relationship between low-field mobility enhancement and stress up to about 1 GPa, this result suggests more-than-1.2-GPa channel tensile stress for 100% measured mobility enhancement. This estimation is in good agreement with the much higher strain values shown in Fig. 6. The different shape of the GAA MOSFETs, compared with that of the nonbended tri-gate devices, will also influence the electrostatics. We have carried out detailed 3-D simulations of this effect [32] and found that it may positively contribute to the device performance. In the best conditions for the present case, this influence may be as large as 10%–15%, but alone, it cannot explain the amount of mobility enhancement observed.

Using mechanical die bending, strain values ranging from 0.07% to 1.9% are found to result in mobility enhancements ranging from 2% to about 200% [17]–[19], [33]–[35].

Moreover, very recent reports on GAA MOSFETs fabricated on strained SOI [36] featuring a similar level of tensile uniaxial strain (2.1 GPa) show transconductance improvement by a factor of 2 over unstrained Si control NW devices, which is in full agreement with our results in this work.

It is worth noting that the extracted mobility reflects an average value over the wire, and in reality, the mobility will likely vary along the nanowire, following the variation of the

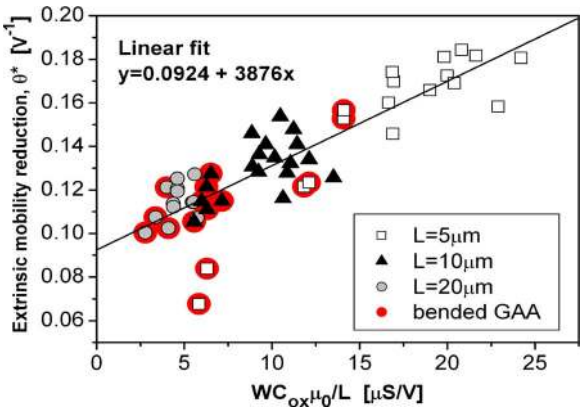

Fig. 13. Extrinsic mobility reduction factor θ^* as a function of $\mathrm{WC_{ox}}\mu_0/L$, along with a linear fit of all data points. The red circles around some plots indicate a bended GAA MOSFET. Strained and nonstrained devices appear to follow the same trend.

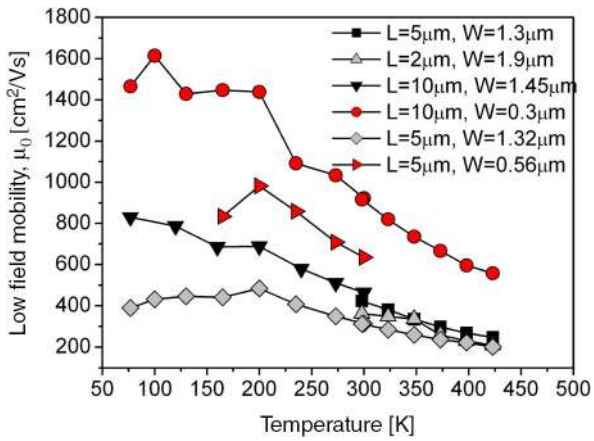

Fig. 14. Low-field mobility extracted by the method in [26] for different temperatures for six different devices, including two bended, i.e., strained, devices. The low-field mobility increases for all devices with decreasing temperature, but the increase appears to be more significant for the bended devices.

strain value. Thus, the *local* mobility enhancement can be larger than the values found in this work.

Overall, the reported values of low-field mobility higher than 900 $\mathrm{cm^2/V \cdot s}$ in our bended GAA MOSFET are remarkably high but physically not so surprising. There are a number of experimental factors that logically contribute to such increased mobility values: the low doping specific to our devices, the very low surface roughness (due to thermal oxidation), no quantization effects (due to the size of our GAA cross sections and relatively thick oxide), and, very importantly, the large amount of uniaxial tensile strain ($>$ 2 GPa), which was confirmed by the Raman investigations near the conducting interfaces.

In the following, we extend the mobility extraction analysis by the experimental investigation of the mobility reduction factor and series resistances in our GAA bended devices. The mobility reduction factor describes the mobility attenuation as a result of the vertical electric field it can be divided into; the extrinsic mobility reduction factor θ^*, which is highly dependent on series resistance; and the intrinsic mobility reduction factor θ, which is principally influenced by the interface quality.

The extrinsic mobility reduction factor is given by

$$\theta^* = \theta + \mathrm{W}\mu_0\mathrm{C_{ox}R_{SD}/L}$$

where R_{SD} is the source–drain series resistance. When the source–drain series resistance is taken into account, θ^* should replace θ.

The intrinsic mobility degradation factor θ and the source–drain series resistance R_{SD} can be extracted from the intercept and slope, respectively, if θ^* is plotted as a function of $\mathrm{WC_{ox}}\mu_0/L$ [30]. In a planar technology, this is achieved by varying the width and/or length of otherwise identical devices. Here, our results are shown in Fig. 13, taking into account the mobility variation with geometry.

In Fig. 13, the symbols surrounded by a larger circle indicate a bended device. The data points appear to lie on a straight line, and the bended devices seem to follow the same trend as the nonbended structures. From the linear fit, a low intrinsic mobility reduction factor θ with a value of 0.0924 $\mathrm{V^{-1}}$ is extracted, suggesting a high quality of the $\mathrm{Si/SiO_2}$ interface and a source–drain series resistance of 3.9 kΩ. The relatively high extracted series resistance is not surprising as no particular contact engineering has been performed (the reported contact resistance corresponds to Al on highly doped silicon regions of the wires). The intrinsic mobility degradation factor θ mainly depends on the interface quality; therefore, in our technology, there should not be a large difference between strained (bended) and nonstrained devices, as the strain is brought about by oxidation, which should not deteriorate the surface quality.

This is in contrast with work based on the use of SiGe substrates to introduce strain [37], where the accompanying germanium segregation is found to increase interface roughness and, thereby, the mobility degradation factor in strained devices, compared with nonstrained devices.

VII. Temperature Effects

The $I_D(V_{GS})$ electrical characteristics of bended and nonbended devices have been measured over a large range of temperatures (from 450 K down to 77 K), and the low-field mobility has been extracted by the method detailed in [30]. Some typical experimental results are plotted in Fig. 14. For both nonbended and bended devices, the threshold voltage is found to decrease by -0.8 mV/K, and both types of device show close-to-ideal inverse subthreshold slopes over the entire temperature range.

As the device operation temperature is reduced, the influence of phonon scattering on the mobility is decreased. It may therefore be expected that the enhancement of strained over nonstrained devices may decrease if the enhancement is based on strain-induced suppression of phonon scattering, as demonstrated in [38]. However, in Fig. 14, we observe the opposite effect: the low-field mobility enhancement tends to increase as the temperature is reduced. This is similar to the results found for strained FD-SOI devices in [39] and is in agreement with the temperature dependence of piezoresistive coefficients in low-doped silicon [40]. Fig. 15 shows the field-effect mobility μ_{fe} for two devices at different temperatures. For the nonbended device, we observe a slow increase in mobility with decreasing temperature, whereas, for the strained bended GAA MOSFET, this trend is much more pronounced. In addition, for

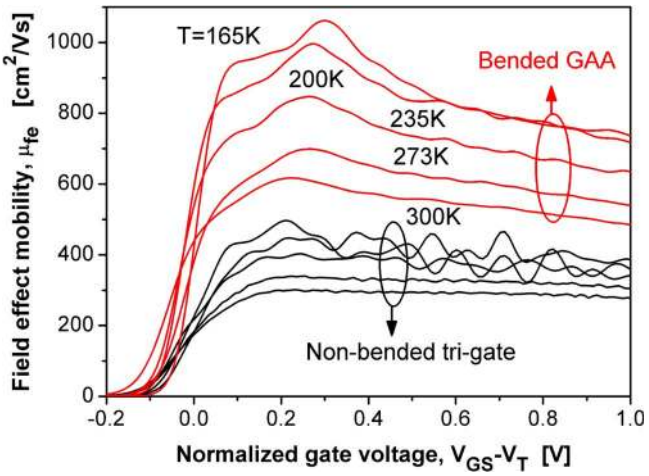

Fig. 15. Field-effect mobility $\mu_{\rm fe}$ versus V_{GS}–V_T. with the temperature as a parameter in bended and nonbended nanowire MOSFETs. Threshold voltage V_T is systematically extracted at each temperature in both types of devices, and $\mu_{\rm fe}$ is calculated based on transconductance data for $V_{DS} = 20$ mV. $W_{\rm eff}$ is 556 nm for the bended device and 1.328 μm for the nonbended device. $L = 5$ μm for both devices.

the bended GAA MOSFET, we observe a sort-of hump in the mobility characteristics, which increases when the temperature is reduced. This may also be due to the corner effect, which increasingly manifests itself at lower temperatures.

In [21], a constant enhancement is found for uniaxially strained devices, whereas biaxially strained devices experience a decreasing performance enhancement as temperatures are reduced below room temperature. This is found to originate from the smaller subband splitting between twofold and fourfold degenerate valleys of the conduction band in uniaxially strained $\langle 110 \rangle$ devices, compared with biaxially strained ones [39].

VIII. Discussion and Conclusion

In this paper, we have presented a method for the introduction of tensile strain locally in the channel of GAA nanowire MOSFETs, based on thermal-oxidation-induced bending. Strain measurements on naked silicon nanowires using Raman spectroscopy show large amounts of tensile strain up to 2.5%. Strain measurements from devices with a completed gate stack show lower values of strain $\sim$0.5%, which are most likely due to strain relaxation in the process, but we still observe a performance (drain current and transconductance) enhancement up to about 100%, depending on the applied biases, in the bended devices, compared with nonbended tri-gate devices, with the highest values of the low-field electron mobility higher than 900 $\rm cm^2/V \cdot s$. At room temperature, for a measured stress of 600 MPa through the gate stack of a bended channel, we measure an improvement of normalized $g_{\rm max}$ of 50% and a low-field mobility of 53% (corresponding to 600 $\rm cm^2/V \cdot s$), compared with a reference nonbended device. The low-field mobility enhancement in bended channels is found to be significantly increased at low temperatures. Overall, this work demonstrates that a local-strain technology can be an adapted performance booster for all-silicon nanowire MOSFETs; the bended channel silicon nanowire transistor is just one possible alternative to implement it.

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