The Impact of Low-Holding-Voltage Issue in High-Voltage CMOS Technology and the Design of Latchup-Free Power-Rail ESD Clamp Circuit for LCD Driver ICs

Ming-Dou Ker, *Senior Member, IEEE,* and Kun-Hsien Lin, *Member, IEEE,*

***Abstract*—The holding voltage of the high-voltage devices in snapback breakdown condition has been found to be much smaller than the power supply voltage. Such characteristics will cause the LCD driver ICs to be susceptible to the latchup-like danger in the practical system applications, especially while these devices are used in the power-rail ESD clamp circuit. A new latchup-free design on the power-rail ESD clamp circuit with stacked-field-oxide structure is proposed and successfully verified in a 0.25-μm 40-V CMOS process to achieve the desired ESD level. The total holding voltage of the stacked-field-oxide structure in snapback breakdown condition can be larger than the power supply voltage. Therefore, latchup or latchup-like issues can be avoided by stacked-field-oxide structures for the IC applications with power supply of 40 V.**

***Index Terms*—Electrostatic discharge (ESD), power-rail ESD clamp circuit, latchup, transient latchup (TLU), transmission line pulsing (TLP).**

I. Introduction

HIGH-VOLTAGE transistors in smart power technologies have been extensively used for display driver ICs, power supplies, power management, and automotive electronics. The electrostatic discharge (ESD) reliability is an important issue for high-voltage transistors with applications in these products. In smart power technology, high-voltage MOSFETs, silicon controlled rectifier (SCR) devices, and bipolar junction transistors had been used as on-chip ESD protection devices [1]–[6]. Those earlier works focused on analyzing and improving ESD robustness of the ESD protection devices in high-voltage CMOS processes [1]–[6]. However, the latchup or latchup-like failure from such ESD protection devices under normal circuit operating conditions was not considered, especially while the devices were used in the power-rail ESD clamp circuit.

The high-voltage CMOS technology has been widely used in the driver ICs to control the display of LCD panels. Fig. 1 shows the typical ESD protection scheme for LCD driver ICs (typically, gate driver with 40 V, and source driver with 12 V,

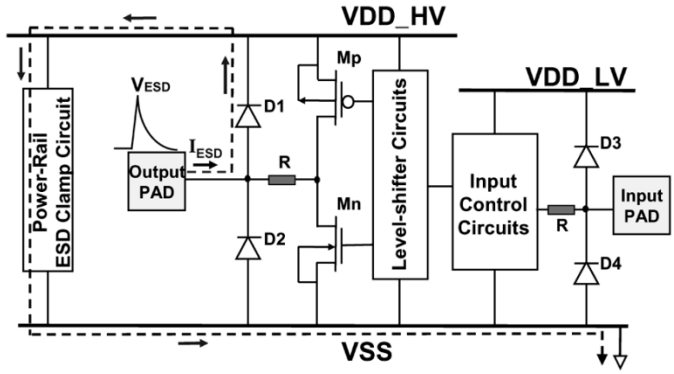

Fig. 1. Typical ESD protection scheme for LCD driver ICs.

for 14.1-in notebook LCD panel). The output buffers (Mp and Mn) are controlled by the input control circuits through the level-shifter circuits. The diodes D1–D4 are used as on-chip ESD protection devices for input and output pads. For the purpose of avoiding the unexpected ESD damage in the internal circuits of CMOS ICs, the turn-on-efficient power-rail ESD clamp circuit was placed between $V_{\rm DD}$ and $V_{\rm SS}$ power rails [7]. The ESD current at the output pad under positive-to-$V_{\rm SS}$ ESD stress can be discharged through the diode D1 to the $V_{\rm DD}$-HV power line, and then discharged through the power-rail ESD clamp circuit from the $V_{\rm DD}$-HV power line to the grounded VSS power line, as the dashed line shown in Fig. 1. Consequently, the traditional I/O circuits cooperating with the power-rail ESD clamp circuit can achieve a much higher ESD level [7]. When the ESD protection device is used in the power-rail ESD clamp circuit, the device is expected to be kept off under normal circuit operating conditions. During ESD stress conditions, the ESD protection device should be triggered on to discharge ESD current. If the holding voltage of the ESD protection device in power-rail ESD clamp circuits is smaller than the power supply voltage, the ESD device may be triggered on by the system-level electromagnetic compatibility (EMC)/ESD transient pulses to cause a very serious "latchup" or "latchup-like" failure in CMOS ICs. This phenomenon often leads to IC function failure or even destruction by burning out [8], [9].

The system-level EMC/ESD reliability of LCD panel has been requested up to 20 kV of ESD stress in the air-discharge mode. The system-level EMC/ESD test on an LCD panel of notebook by an ESD gun (Standard IEC 61000-4-2 [10]) is

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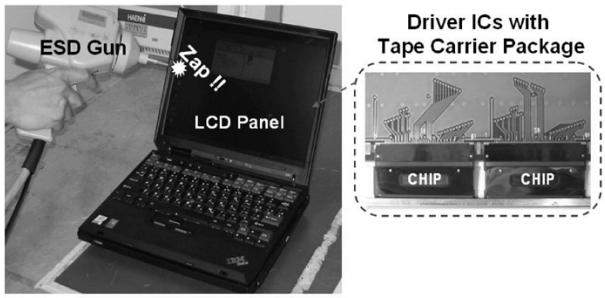
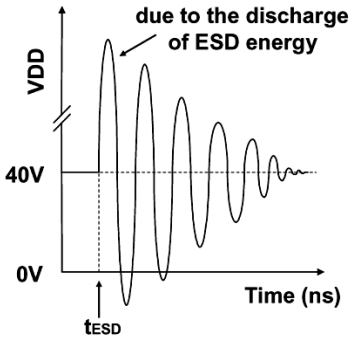


(a)



(b)

Fig. 2. (a) System-level EMC/ESD test on LCD panel of notebook by an ESD gun. The driver ICs with tape carrier package (TCP) are directly attached to the LCD panel. (b) Transient overshooting/undershooting voltage waveform on the $V_{\rm DD}$ pin of the driver ICs during system-level EMC/ESD test.

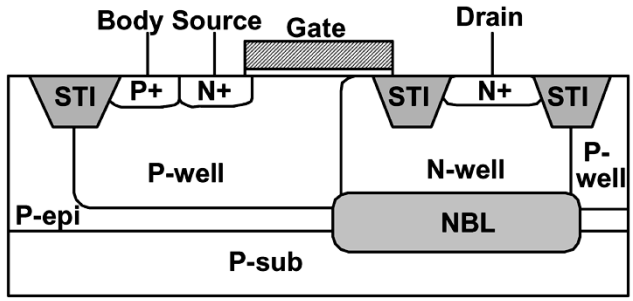
shown in Fig. 2(a). During the system-level ESD stress, the power lines of driver ICs in the LCD panel of notebook can be coupled with an overshooting/undershooting voltage up to several hundred volts [11], as shown in Fig. 2(b). In particular, the driver ICs with tape carrier package (TCP) are directly attached to the LCD panel. No room is available for the driver ICs with on-board de-coupling discrete components to shunt the ESD-zapping transient voltage away from the driver ICs. So, the transient voltage seen by the circuits in the driver ICs is quite large during such system-level EMC/ESD zapping.

In this study, the I–V characteristics of ESD protection devices fabricated in a 0.25-μm 40-V CMOS process under transmission line pulsing (TLP) stress are found to have a very low holding voltage [12]. The susceptibility of the ESD protection devices to the noise transient or glitch on the power lines during normal circuit operating conditions are investigated by the transient latchup (TLU) test [13]. A new latchup-free design on the power-rail ESD clamp circuit with stacked-field-oxide structure is proposed and verified in a 0.25-μm 40-V CMOS process to achieve the desired ESD level.

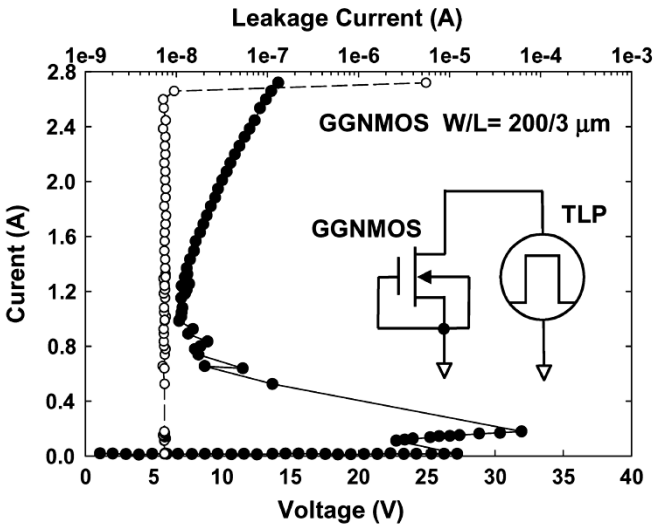
II. High-Voltage ESD Protection Devices

A. TLP I–V Characteristics

The lateral diffused MOS (LDMOS) device, SCR device, and field-oxide (FOD) device fabricated in a 0.25-μm 40-V CMOS process are studied in this work. The layout parameters of such ESD protection devices are drawn according to the foundry's ESD rules with the silicide-blocking mask. To investigate the turn-on behaviors of such ESD protection devices during high ESD current stress, a TLP generator [14] with a pulse width



(a)



(b)

Fig. 3. (a) Cross-sectional view and (b) TLP-measured I–V characteristic of high-voltage gate-grounded nMOS (GGNMOS) device fabricated in a 0.25-μm 40-V CMOS process.

of 100 ns and a rise time of $\sim$10 ns is used to measure the snapback I–V curves of the devices. The cross-sectional views and TLP-measured I–V characteristics of high-voltage gate-grounded nMOS (GGNMOS) device, SCR device, FOD device, and gate–$V_{\rm DD}$ pMOS (GDPMOS) are shown in Figs. 3–6, respectively.

For the high-voltage GGNMOS device in Fig. 3(a), the double-snapback characteristic has been found. As shown in Fig. 3(b), after the first TLP-trigger voltage at 27.2 V (52 V in dc), the device snaps back to 23 V, from where the voltage strongly increases again. Then, the device goes into the second snapback, and the voltage drops to only $\sim$7 V. The turn-on resistance of the first snapback state is much larger than that of the second snapback state. The double-snapback characteristic of the GGNMOS device is related to the turn-on behavior of the parasitic bipolar transistor and the occurrence of the Kirk effect (base push-out effect) [15], [16]. The second breakdown current (It2) of the GGNMOS device with 200-μm channel width is 2.7 A. For a high-voltage SCR device in Fig. 4(a), the characteristic of very low holding voltage and high ESD robustness has been found. As shown in Fig. 4(b), the holding voltage of the SCR device is only $\sim$4 V and the It2 current of the SCR device with 200-μm width is over 6 A. For the high-voltage FOD device structure shown in Fig. 5(a), the device is isolated by the n+ buried layer (NBL) from the common p-type substrate. The

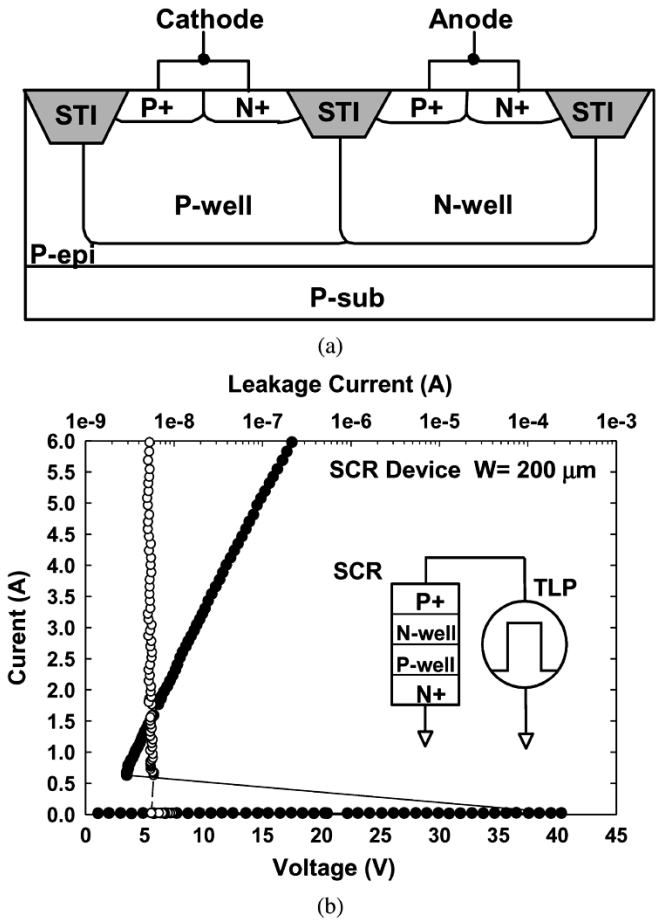


Fig. 4. (a) Cross-sectional view and (b) TLP-measured I–V characteristic of high-voltage silicon controlled rectifier (SCR) device fabricated in a 0.25-μm 40-V CMOS process.

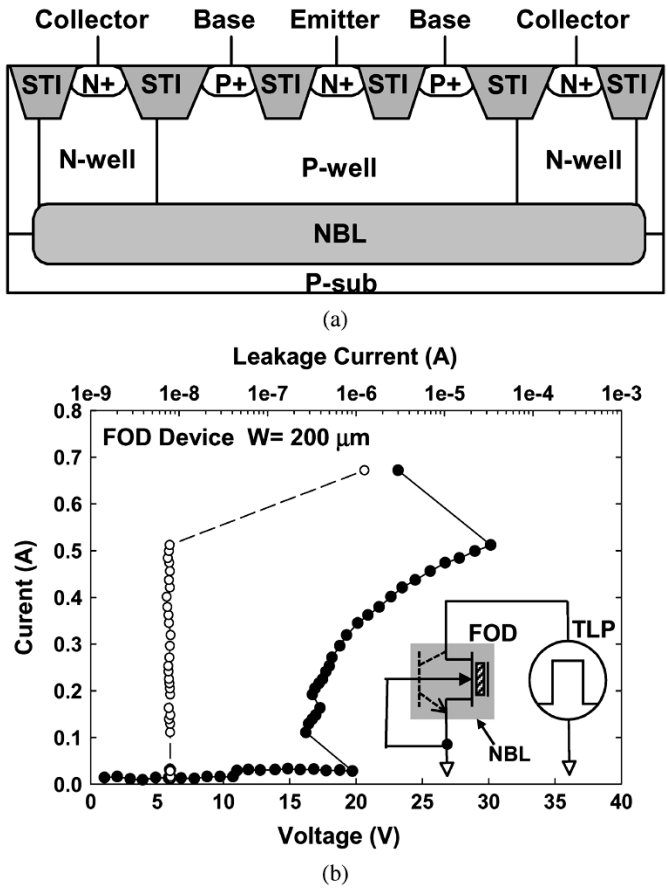


Fig. 5. (a) Cross-sectional view and (b) TLP-measured I–V characteristic of high-voltage field-oxide (FOD) device fabricated in a 0.25-μm 40-V CMOS process.

emitter diffusion is enclosed by the collector diffusion, while the base diffusion is inserted between the emitter diffusion and collector diffusion in the layout structure. The spacing from the collector diffusion to the emitter diffusion of the FOD device is 6 μm in this study. As shown in Fig. 5(b), the TLP-trigger voltage is 19.7 V (50 V in dc), and the holding voltage is $\sim$16 V. The $\mathrm{It2}$ current of the FOD device with 200-μm width is 0.5 A. The difference in trigger voltages of the device measured by dc (HP4155) and TLP is caused by the transient-coupling effect (dV/dt transient) through the parasitic capacitance in the drain/bulk junction of the device. The TLP is designed with a rise time of 10 ns to simulate the human-body-model (HBM) ESD event [17]. The dV/dt transient voltage at the zapping node can generate the displacement current to turn on the parasitic bipolar transistor of the device without involving the avalanche breakdown. Therefore, the trigger voltage of the device is lower by TLP measurement.

For the high-voltage GDPMOS device in Fig. 6(a), no snapback characteristic is found. The holding voltage of the device is larger than the supply voltage of 40 V. Due to the inefficient parasitic p-n-p bipolar action, the $\mathrm{It2}$ current of GDPMOS device with 200-μm channel width is only 0.06 A, as shown in Fig. 6(b). Therefore, GDPMOS is not suitable for on-chip ESD protection devices in high-voltage CMOS ICs due to too low ESD robustness.

B. Transient Latchup Test

TLU test is used to investigate the susceptibility of the ESD protection devices to the noise transient or glitch on the power lines during normal circuit operating condition. The measurement setup for TLU test is shown in Fig. 7. The positive or negative charging voltage (V_{charge}) on the energy storage capacitor (C1) generating the transient is used to trigger the device into the latch state [13]. A supply voltage of 40 V was used to bias the device under normal circuit operating conditions. The transient trigger source was connected directly to the device-under-test (DUT). The small resistance (R1) is used to protect the DUT when the DUT is triggered on into the latch state. In addition, the diode (D1) in Fig. 7 is used to avoid the damage to the power supply during TLU test [13]. The voltage waveform on the DUT (at node Y) during the TLU test is monitored by a digital oscilloscope with a sampling rate of 5 GHz in this experiment. The measured voltage waveforms on high-voltage GGNMOS device, SCR device, and FOD device under TLU test are shown in Figs. 8–10, respectively.

From the measured results, the devices are initially kept off before the transient trigger, therefore the voltage waveforms are initially kept at 40 V. After the transient trigger, the snapback characteristic in the device can be triggered on to generate a low-holding-voltage state. The clamped voltage level of the devices in snapback breakdown condition is consistent with the holding voltage measured by TLP stress. In Fig. 8,

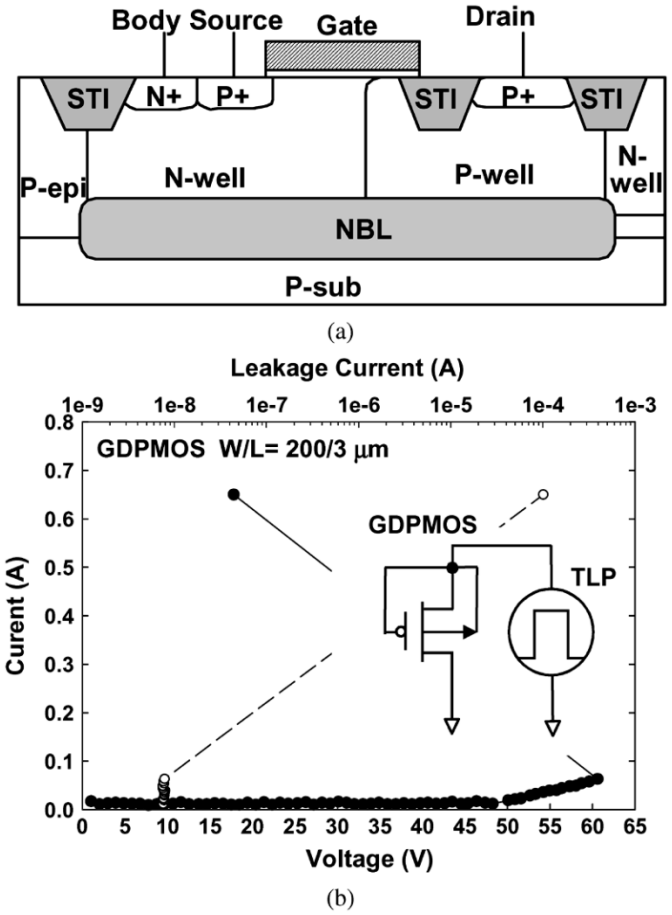


Fig. 6. (a) Cross-sectional view and (b) TLP-measured I–V characteristic of high-voltage gate–V_{DD} pMOS (GDPMOS) device fabricated in a 0.25-μm 40-V CMOS process.

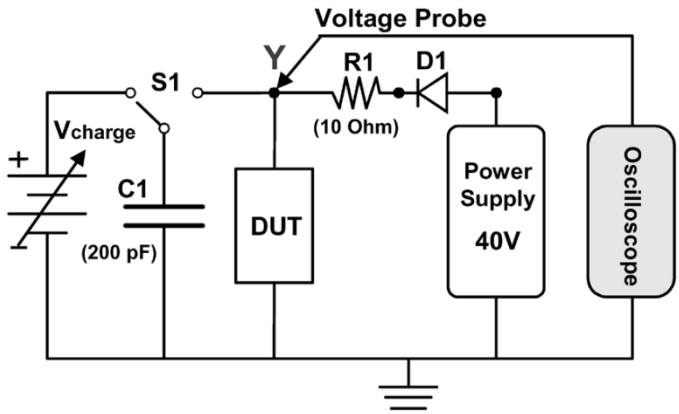


Fig. 7. Measurement setup for TLU test.

the clamped voltage level of high-voltage GGNMOS device is $\sim$7 V due to the transient triggering with the capacitor charging voltage of 55 V. The GGNMOS device is triggered into the second snapback state directly by the transient pulse. If such a high-voltage nMOSFET is used in the power-rail ESD clamp circuit, the latchup-like issue between the power rails will occur, when the high-voltage nMOSFET is triggered on by the noise transient on the power lines. In Fig. 9, the clamped voltage level of high-voltage SCR device is only $\sim$4 V due to the transient triggering with the capacitor charging voltage of only 44 V.

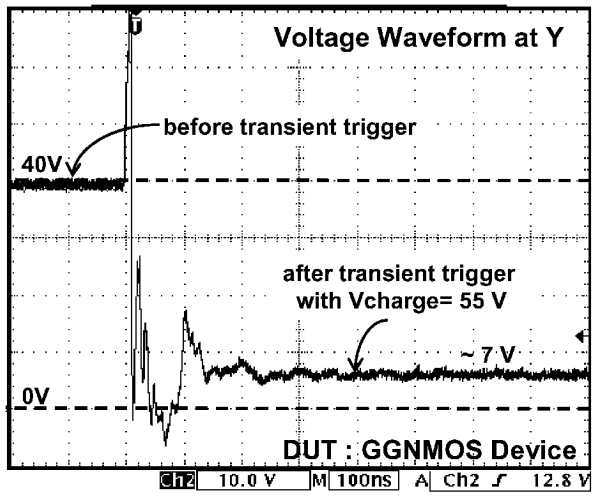


Fig. 8. Measured voltage waveform on the high-voltage GGNMOS device under TLU test. (Y axis = 10 V/Div., X axis = 100 ns/Div.)

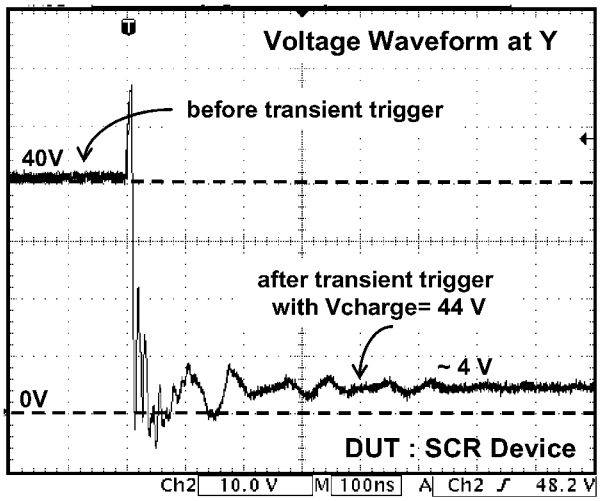
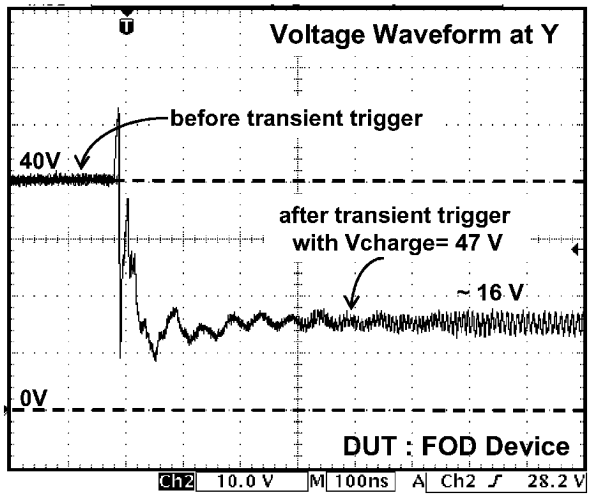


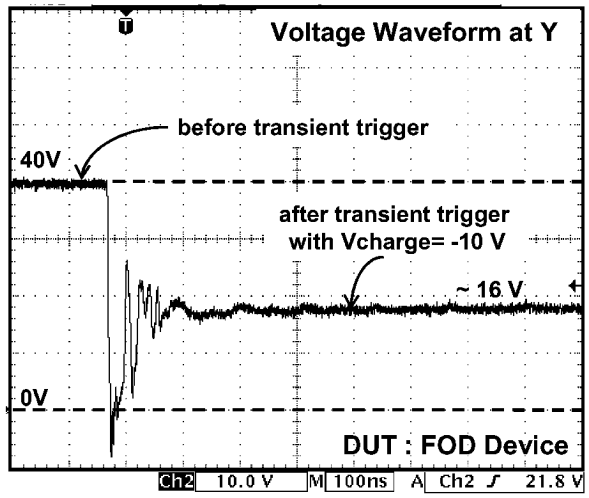
Fig. 9. Measured voltage waveform on the high-voltage SCR device under TLU test. (Y axis = 10 V/Div., X axis = 100 ns/Div.)

Although the SCR device has the advantage of high ESD robustness, the latchup issue in high-voltage CMOS ICs becomes worse. Fig. 10(a) and (b) shows the measured voltage waveforms of a high-voltage FOD device under TLU test with positive and negative charging voltages, respectively. Both positive and negative charging voltages can trigger the FOD device into the latch state. The clamped voltage level of the FOD device is $\sim$16 V due to the transient triggering with the capacitor charging voltage of 47 V or $-$10 V. For negative charging voltage, the parasitic N-well/p-substrate junction between the power rails may be turned on initially, but it is turned off quickly due to the transient ringing voltage waveform. Finally, the FOD device is triggered into the holding state. The latchup-like issue is the concern by using single FOD device as the power-rail ESD clamp in high-voltage CMOS ICs.

From the power dissipation view, the device with a lower holding voltage is helpful to sustain much higher ESD current. However, the device may be triggered on by the noise transient or glitch on the power lines during normal circuit operating condition, especially under the system-level EMC/ESD



(a)



(b)

Fig. 10. Measured voltage waveforms on the high-voltage FOD device under TLU test with (a) positive charging voltage, and (b) negative charging voltage. (Y axis $=$ 10 V/Div., X axis $=$ 100 ns/Div.)

zapping test. If the holding voltages of high-voltage ESD protection devices are smaller than the power supply voltage under normal circuit operating conditions, the high-voltage CMOS ICs will be susceptible to the latchup or latchup-like danger in the system applications, which often meet the noise or transient glitch issues.

III. Design of Latchup-Free Power-Rail ESD Clamp Circuits

The NMOS and SCR devices have higher It2 than that of the FOD device, but their holding voltages ($\sim$7 V in NMOS, $\sim$4 V in SCR) are far away from the 40-V operating voltage level. Such ESD protection devices with low holding voltage in power-rail ESD clamp circuits will cause serious latchup failure to high-voltage CMOS ICs. To overcome the latchup or latchup-like issue between the power rails in high-voltage CMOS ICs during normal circuit operating conditions, a new stacked-field-oxide structure has been designed to increase the total holding voltage. The layout top view with the corresponding schematic diagram and the cross-sectional view of the stacked-field-oxide structure with two cascaded FOD devices fabricated in a 0.25-μm 40-V CMOS process are shown in Fig. 11(a) and (b), respectively. The layout area of the stacked-field-oxide structure with a device width of 200 μm for each FOD device is 150 μm $\times$ 60 μm. The I–V characteristic and ESD robustness of the stacked-field-oxide structure has been investigated by the TLP stress. The susceptibility of the stacked-field-oxide structure to the noise transient during normal circuit operating conditions has also been performed by the TLU test. Finally, a latchup-free power-rail ESD clamp circuit with a stacked-field-oxide structure is proposed and verified.

A. TLP I–V Characteristics

The measurement setup of a single high-voltage FOD device and a stacked-field-oxide structure under TLP stress is shown in Fig. 12(a). The TLP-measured I–V characteristics of these devices with different device widths are compared in Fig. 12(b). From the measured results, the holding voltage of the stacked-field-oxide structure in the snapback region is double of that of a single FOD device. It is important to note that the each FOD device in stacked-field-oxide structure is isolated by the NBL from the common p-type substrate. The turn-on current can flow through the cascaded parasitic bipolar transistor of each FOD device and the accumulation property in the holding voltage for the stacked-field-oxide structure can be achieved. Therefore, the holding voltage of the stacked-field-oxide structure can be linearly increased by increasing the numbers of cascaded FOD devices. The It2 currents of the single FOD device and the stacked-field-oxide structure as a function of device channel width are compared in Fig. 13. The It2 current of the stacked-field-oxide structure is linearly increased while the device channel width increases. In addition, the It2 current of the stacked-field-oxide structure is only slightly degraded as compared with that of the single FOD device. The relation between the It2 and HBM ESD level, $V_{\rm ESD}$, can be approximated as

$$V_{\rm ESD} \cong (1500 + R_{\rm ON}) \times {\rm It2} \tag{1}$$

where $R_{\rm ON}$ is the dynamic turn-on resistance of the device under test. From Fig. 13, the stacked-field-oxide structure with a device width of $\sim$650 μm for each FOD device can sustain the typical 2-kV (It2 of $\sim$1.33 A) HBM ESD stress. To meet the specified ESD level of driver ICs, it can be achieved by adjusting the device width of the stacked-field-oxide devices.

To investigate the temperature-dependent behavior of the stacked-field-oxide structure, the TLP-measured I–V characteristics of stacked-field-oxide structure under different temperatures (25 °C, 75 °C, and 125 °C) are compared in Fig. 14. The measured result shows no significant difference on the holding voltage of the stacked-field-oxide structure when the temperature increases. Therefore, the holding voltage of the stacked-field-oxide structure can be successfully controlled by the cascaded FOD devices even at high temperature.

Under ESD stress conditions, the ESD clamp device should turn on quickly to bypass the ESD current before the internal

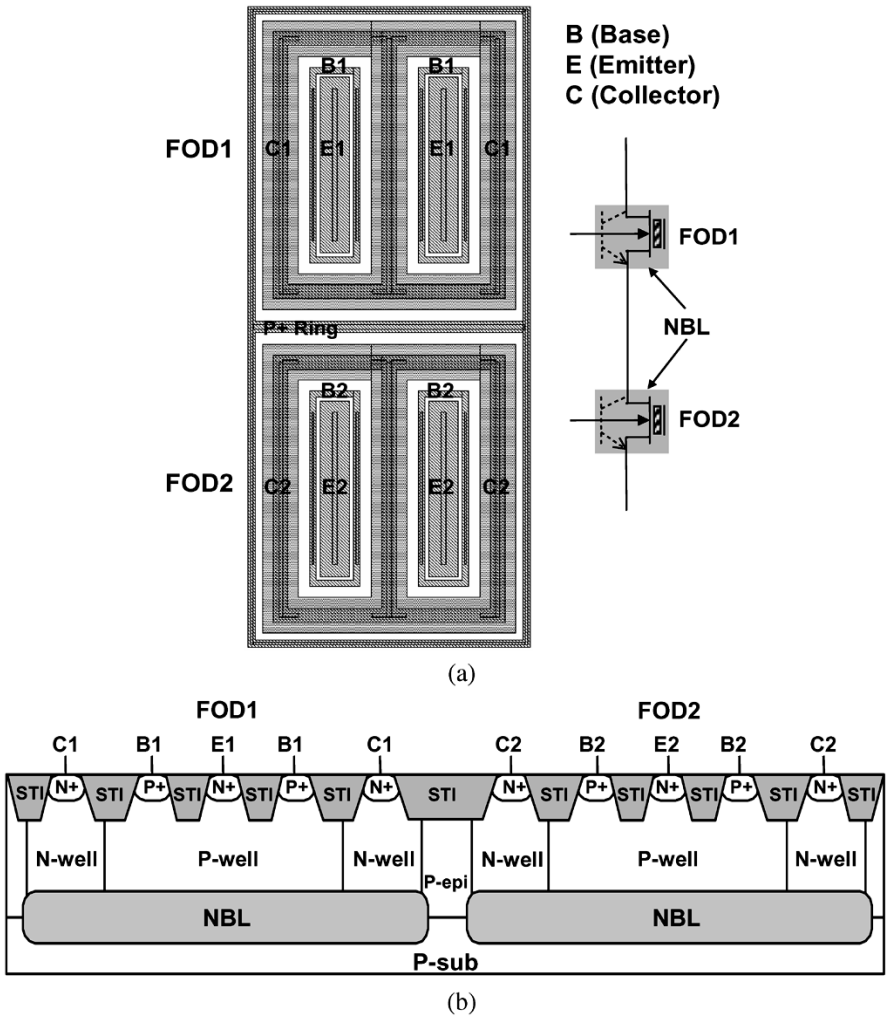


Fig. 11. (a) Layout view with the corresponding schematic diagram and (b) the cross-sectional view of the stacked-field-oxide structure with two cascaded FOD devices. Each FOD device in the stacked-field-oxide structure is isolated by the NBL from the common p-type substrate. The metal connections between the FOD devices are not shown.

circuits are damaged by the ESD energy. From Fig. 12, the trigger voltage of the stacked-field-oxide structure is increased as compared with that of a single FOD device. The substrate-triggered technique [18]–[21] can be applied to lower the trigger voltage of the device to ensure effective ESD protection. The TLP-measured I–V curves of the stacked-field-oxide structure with different substrate-triggered currents (Itrig) are shown in Fig. 15. From the measured results, the trigger voltage of the stacked-field-oxide structure is obviously decreased while the substrate-triggered current is applied. The trigger voltage can be reduced to only 17 V when the substrate-triggered current is 10 mA. Therefore, the trigger voltage of the stacked-field-oxide structure can be effectively reduced lower than the breakdown voltage of internal circuits by the substrate-triggered technique. Moreover, the $\mathrm{It2}$ level of the stacked-field-oxide structure with substrate-triggered current can be improved.

B. Transient Latchup Test

The measured voltage waveforms of stacked-field-oxide structure under TLU test with the transient triggering of positive and negative charging voltages are shown in Fig. 16(a) and (b), respectively. From the observed voltage waveforms, the stacked-field-oxide structure is triggered on due to the transient triggering with the capacitor charging voltages of 80 V or -50 V. But, the clamped voltage waveform quickly comes back to the original supply voltage level of 40 V, without keeping in the latch state after the triggering. The measured result is consistent with TLP-measured I–V curves, as those shown in Fig. 12(b). The total holding voltage of the stacked-field-oxide structure with two cascaded FOD devices is near the supply voltage of 40 V. After the stacked-field-oxide structure is triggered on during the TLU test, the clamped voltage level can quickly restore to the supply voltage. Therefore, no latchup or latchup-like issue is occurred. In addition, a higher charging voltage stored in the capacitor (C1) is needed to trigger on the stacked-field-oxide structure during the TLU test. Therefore, the latchup immunity of the stacked-field-oxide structure to the noise transient on the power lines in high-voltage CMOS ICs has been significantly improved.

C. Latchup-Free Power-Rail ESD Clamp Circuits

The proposed power-rail ESD clamp circuits with two cascaded FOD devices and three cascaded FOD devices in high-voltage CMOS ICs are shown in Fig. 17(a) and (b), respectively.

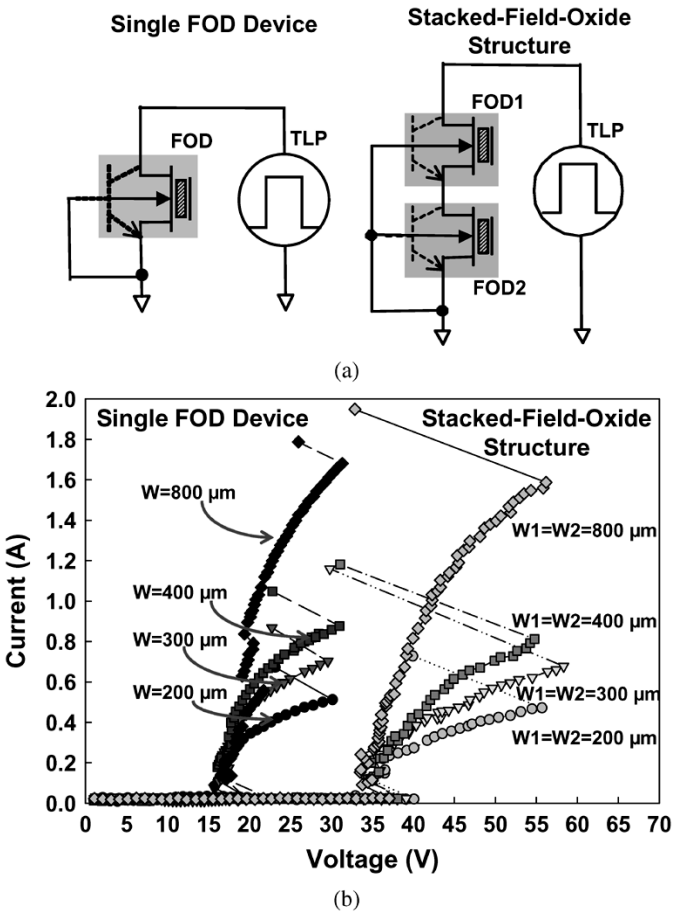


Fig. 12. (a) Measurement setup of single high-voltage FOD device and stacked-field-oxide structure under TLP stress. (b) The TLP-measured I–V characteristics of these devices with different device widths. W1 is the channel width of FOD1, and W2 is the channel width of FOD2.

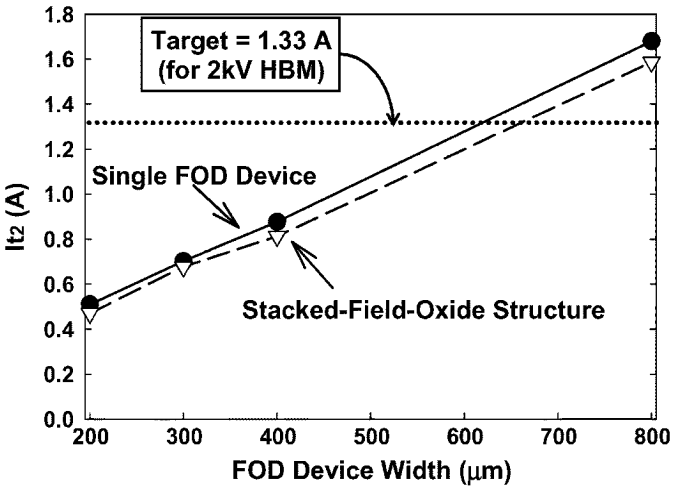


Fig. 13. It2 currents of single FOD device and stacked-field-oxide structure as a function of device channel width.

Each FOD device in the stacked-field-oxide structure is isolated by the NBL from the common p-type substrate. With two cascaded FOD devices in Fig. 17(a), the total holding voltage of stacked-field-oxide structure in the snapback region is double of that of single FOD device. The latchup immunity of the power-rail ESD clamp circuit to the noise transient during normal circuit operating conditions can be highly increased. With three cascaded FOD devices in Fig. 17(b), the total holding voltage of the stacked-field-oxide structure can be designed higher than the supply voltage. The blocking diodes Db are used to block the current flowing through the metals connected among the trigger nodes (base nodes) of the stacked FOD devices [22]. Therefore, the unexpected current path can be avoided and the accumulation property in holding voltage for the three cascaded FOD devices can be achieved. In addition, if the total holding voltage of the stacked structure can be designed higher than the supply voltage, FOD3 in Fig. 17(b) can be even replaced by other type of ESD device. So, by adjusting different numbers or even different types of stacked ESD devices (NMOS, SCR, or FOD) in the power-rail ESD clamp circuits, the total holding voltage of the stacked structure can be designed higher than the supply voltage. With the total holding voltage of the stacked structure higher than the supply voltage, the latchup or latchup-like issue will not occur even though the stacked structure is mistriggered by the noise transient or glitch on the power lines during

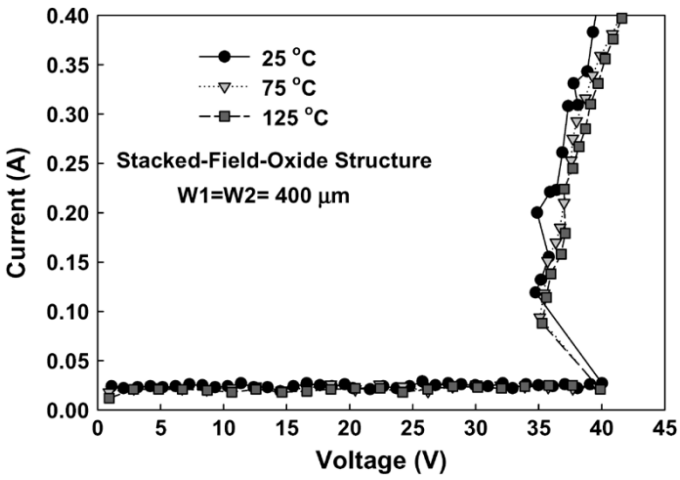


Fig. 14. Holding voltage of the stacked-field-oxide structure (two cascaded FOD devices) under different temperatures measured by TLP.

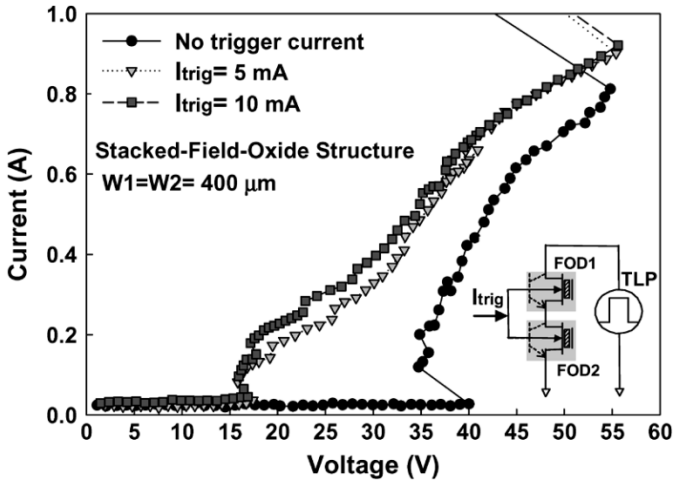
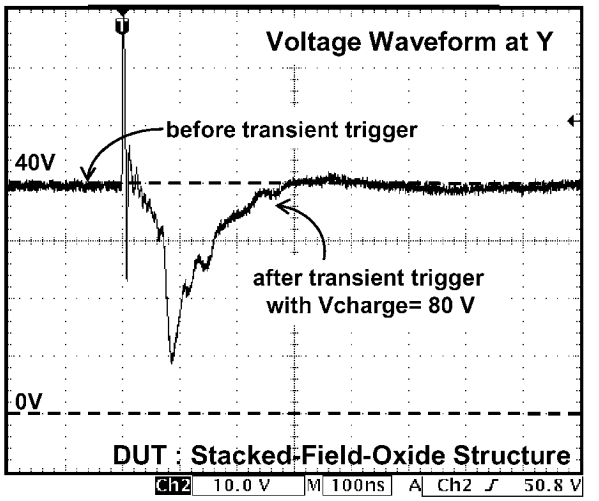
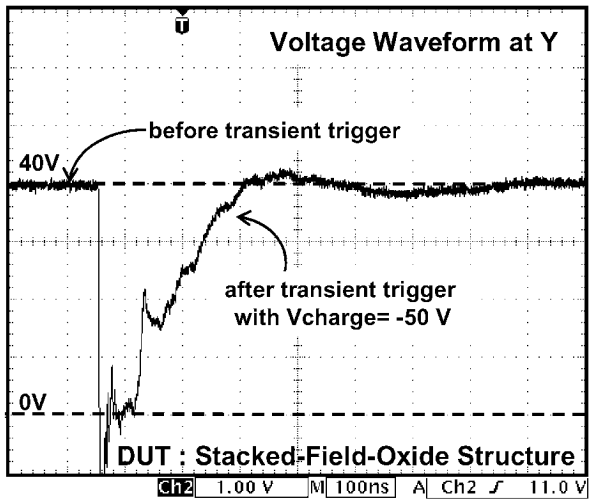


Fig. 15. TLP-measured I–V curves of the stacked-field-oxide structure with different substrate-triggered currents.

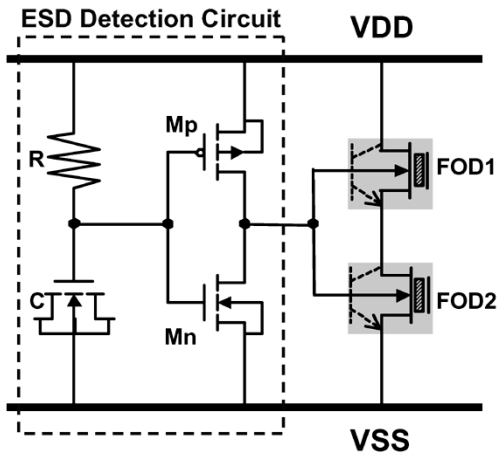


(a)

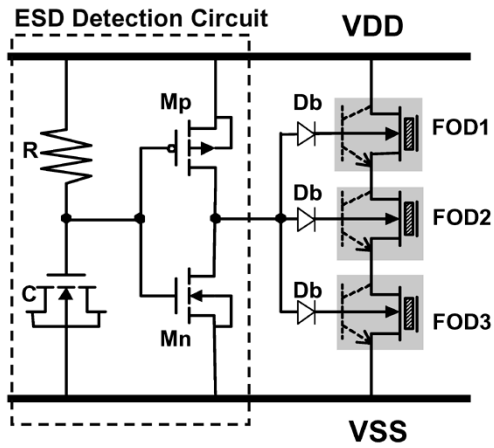


(b)

Fig. 16. Measured voltage waveforms on the stacked-field-oxide structure under TLU test with (a) positive charging voltage and (b) negative charging voltage. (Y axis = 10 V/Div., X axis = 100 ns/Div.)



(a)



(b)

Fig. 17. Proposed power-rail ESD clamp circuits in high-voltage CMOS ICs with (a) two cascaded FOD devices and (b) three cascaded FOD devices. The blocking diodes Db are used to block the current flowing through the metals connected among the trigger nodes (base nodes) of the stacked FOD devices [22].

normal circuit operating conditions. Therefore, the transient-induced latchup issue can be successfully overcome without modifying the high-voltage CMOS process. To provide effective ESD protection to the internal circuits during ESD stress, the substrate-triggered technique is achieved by the *RC*-based ESD detection circuit [18]. The *RC*-based ESD detection circuit can detect the ESD pulse to provide trigger current into the stacked structure, and then the stacked structure can turn on quickly to discharge the ESD current.

IV. Conclusion

Latchup or latchup-like issue of ESD protection devices in high-voltage CMOS ICs has been clearly investigated by TLP stress and TLU test. The impact of low holding voltage of ESD protection devices to cause the LCD driver ICs to be susceptible to latchup or latchup-like danger during normal circuit operating conditions has been shown. By adjusting different numbers or different types of stacked ESD devices in the power-rail ESD clamp circuits, the total holding voltage of the stacked structure can be designed to be higher than the supply voltage without using extra process modification in high-voltage CMOS technology. For the IC applications with power supply of 40 V, a new latchup-free power-rail ESD clamp circuit with stacked-field-oxide structure has been designed and successfully verified in a 0.25-μm 40-V CMOS process to meet the desired ESD level.

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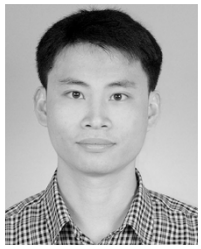

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