UNIVERSITY OF AMSTERDAM

UvA-DARE (Digital Academic Repository)

The silicon microvertex detector

Acciarri, M.; Bobbink, G.J.; Duinker, P.

Publication date
1994

Published in
Nuclear Instruments & Methods in Physics Research Section A - Accelerators Spectrometers Detectors and Associated Equipment

Link to publication

Citation for published version (APA):
Acciarri, M., Bobbink, G. J., & Duinker, P. (1994). The silicon microvertex detector. *Nuclear Instruments & Methods in Physics Research Section A - Accelerators Spectrometers Detectors and Associated Equipment*, *531*(a), 300-312.

General rights
It is not permitted to download or to forward/distribute the text or part of it without the consent of the author(s) and/or copyright holder(s), other than for strictly personal, individual use, unless the work is under an open content license (like Creative Commons).

Disclaimer/Complaints regulations
If you believe that digital publication of certain material infringes any of your rights or (privacy) interests, please let the Library know, stating your reasons. In case of a legitimate complaint, the Library will make the material inaccessible and/or remove it from the website. Please Ask the Library: https://uba.uva.nl/en/contact, or a letter to: Library of the University of Amsterdam, Secretariat, Singel 425, 1012 WP Amsterdam, The Netherlands. You will be contacted as soon as possible.

UvA-DARE is a service provided by the library of the University of Amsterdam (https://dare.uva.nl)

Download date:25 Aug 2022

ELSEVIER

Nuclear Instruments and Methods in Physics Research A 351 (1994) 300–312

NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH
Section A

The L3 silicon microvertex detector

Dedicated to the memory of Vanko Krastev and his family.

M. Acciarri [l], A. Adam [e], O. Adriani [f], S. Ahlen [d], J. Alcaraz [h], G. Ambrosi [m], E. Babucci [m], L. Baksay [p], A. Baschirotto [l], R. Battiston [h,m], W. Baur [r], A. Bay [i], Gy.L. Bencze [e], B. Bertucci [m], M. Biasini [m], G.M. Bilei [m], G.J. Bobbink [b], J.G. Boissevain [k], M. Bosetti [l], M.L. Brooks [k], W.J. Burger [i], J. Busenitz [p], C. Camps [a], M. Caria [m], G. Castellini [g], R. Castello [l], B. Checcuccl [m], A. Chen [n], T.E. Coan [k,*], V. Commichau [a], D. DiBitonto [p], J. Ding [m], P. Duinker [b], L. Djambazov [r], S. Easo [m], P. Extermann [i], E. Fiandrini [m], A. Gabbanini [g], J. Goldstein [d], A. Gougas [c], K. Hangarter [a], C. Hauviller [h], A. Herve [h], M. Hofer [r], T. Hofer [r], S. Hou [n], M.I. Josa [h], J.S. Kapustinsky [k], D. Kim [o], W.W. Kinnison [k], H. Kirst [q], J. Kornis [e], V.R. Krastev [m,†], P. Ladron [h], G. Landi [f], M. Lebeau [1], P. Lecomte [r], D.M. Lee [k], R. Leiste [h,q], E. Lejeune [i], W.T. Lin [n], W. Lohmann [q], A. Marin [d], R. Massetti [m], G.B. Mills [k], H. Nowak [q], M. Okle [r], G. Passaleva [f,n], T. Paul [c], M. Pauluzzi [m], S. Pensotti [l], E. Perrin [d], N. Produit [i], P.G. Rancoita [l], M. Rattaggi [l], J.-P. Richeux [i], A. Santocchia [m], R. Siedling [a], M. Sachwitz [q], P. Schmitz [q], B. Schöneich [q], L. Servoli [m], K. Subham [p], G.F. Susinno [i], G. Terza [l], M. Tesi [g], T. Thompson [k], F. Tonisch [q], J. Toth [e], G. Trowitzsch [q], G. Viertel [r], H. Tuchscherer [p], H. Vogt [q], S. Wang [m], S. Waldmeier [r], R. Weill [j], J. Xu [a], S.C. Yeh [p], B. Zhou [d], G. Zilizi [p,2]

[a] *I. Physikalisches Institut, RWTH, D-52056 Aachen, FRG; III Physikalisches Institut, RWTH, D-52056 Aachen, Germany*
[b] *National Institute for High Energy Physics, NIKHEF, NL-1009 DB Amsterdam, The Netherlands*
[c] *Johns Hopkins University, Baltimore, MD 21218, USA*
[d] *Boston University, Boston, MA 02215, USA*
[e] *Central Research Institute for Physics of the Hungarian Academy of Sciences, H-1525 Budapest 114, Hungary*
[f] *INFN Sezione di Firenze and University of Florence, I-50125 Florence, Italy*
[g] *INFN Sezione di Firenze and Instituto Ricerca Onde Elettromagnetiche, I-50125 Florence, Italy*
[h] *European Laboratory for Particle Physics, CERN, CH-1211 Geneva 23, Switzerland*
[i] *DPNC l'Université de Genève, CH-1211 Genève 4, Switzerland*
[j] *University of Lausanne, CH-1015 Lausanne, Switzerland*
[k] *Los Alamos National Laboratory, Los Alamos, NM 87545, USA*
[l] *INFN-Sezione di Milano, I-20133 Milan, Italy*
[m] *INFN-Sezione di Perugia and Università Degli Studi di Perugia, I-06100 Perugia, Italy*
[n] *National Central University, Chung-li 32054, Taiwan*
[o] *National Tsing Hua University, Hsinchu 30043, Taiwan*
[p] *University of Alabama, Tuscaloosa, AL 35486, USA*
[q] *DESY-Institut für Hochenergiephysik, D-15738 Zeuthen, Germany*
[r] *Eidgenössische Technische Hochschule, ETH Zürich, CH-8093 Zürich, Switzerland*

Received 3 June 1994

* Corresponding author. E-mail coan@mail.physics.smu.edu.

† Deceased.

[1] Permanent address: Laboratoire d'Annecy-le-Vieux de Physique des Particules, LAPP, IN2P3-CNRS, BP 110, F-74941 Annecy-le-Vieux Cedex, France.

[2] Permanent address: Kiserleti Fizika, Kossuth Egyetem, Debrecen, Hungary.

0168-9002/94/$07.00 © 1994 Elsevier Science B.V. All rights reserved
SSDI 0168-9002(94)00709-G

Abstract

The design and construction of the silicon strip microvertex detector (SMD) of the L3 experiment at LEP are described. We present the sensors, readout electronics, data acquisition system, mechanical assembly and support, displacement monitoring systems and radiation monitoring system of the recently installed double-sided, double-layered SMD. This detector utilizes novel and sophisticated techniques for its readout.

1. Introduction

At the beginning of 1991, the radius of the LEP beam pipe at its four interaction points was reduced from 8.0 cm to 5.5 cm. L3 decided to take advantage of this newly acquired space by installing a silicon microstrip detector (SMD) to upgrade its central tracking capability. The intention was to design, build and install the SMD in a period of just two years so that this new detector would be taking data by 1993. Consequently, our general design philosophy was to use existing technology as much as possible to guide our choices for such key items as sensor design, readout electronics, data acquisition system, cooling techniques and displacement monitoring systems.

The advantages of placing a tracking system with a coordinate resolution of ~ 10 μm close to the beam pipe are well known [1]. For L3, the SMD will significantly improve transverse momentum and impact parameter resolution for studying W-pair production physics at LEP200 ($\sqrt{s} \sim 200$ GeV), and to provide enhanced b-quark tagging capability to aid a potential Higgs detection in this energy regime. Installation during LEP100 ($\sqrt{s} \sim m_z$) facilitates detector debugging due to the large reaction cross section at the Z resonance.

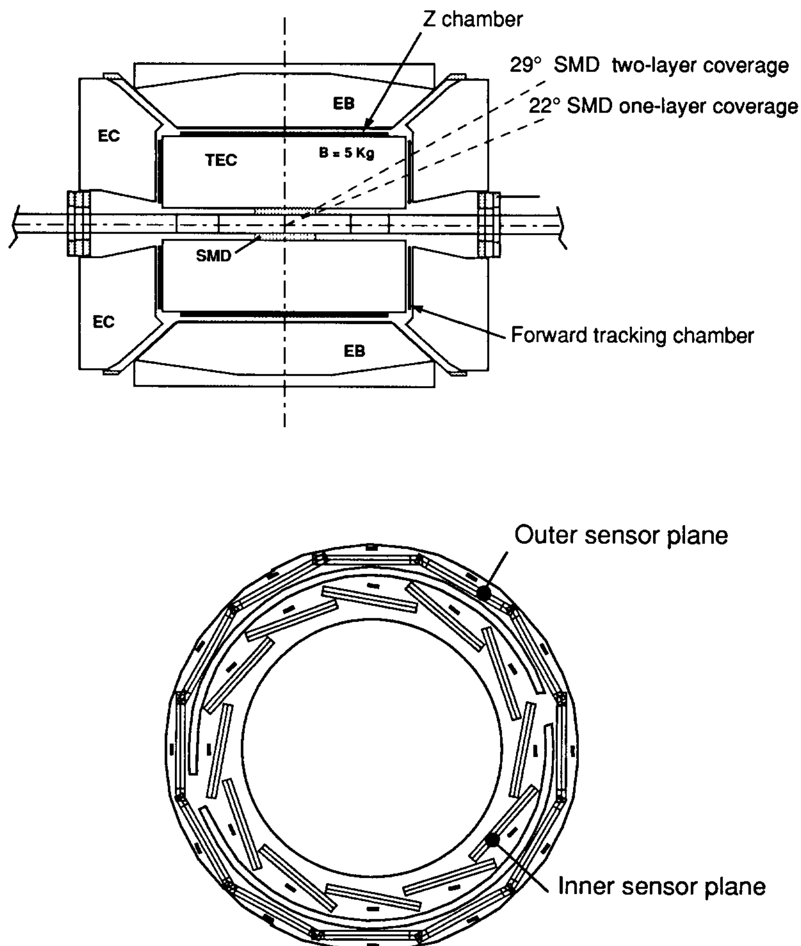

Fig. 1. The top view shows the SMD positioned inside the L3 central tracking system. The bottom view shows a transverse view of the SMD's two radial planes.

The SMD is built from two radial layers of double-sided silicon strip detectors and is capable of providing $r-\phi$ and $r-z$ coordinate measurements over the polar angle range $|\cos\theta| \leq 0.93$ and over the full azimuth. Its principal components are 0.25 m^2 of double-sided silicon strip sensors, front end readout electronics utilizing an application specific integrated circuit (ASIC), a novel cabling scheme for half of its ~73000 readout channels, a low-mass mechanical support structure, custom fiber optic communication with a custom VME-based data acquisition system, dual displacement monitoring systems and a radiation monitoring system for detector safety.

The SMD is designed to be installed inside the existing central tracker of L3, which consists of a cylindrical time expansion chamber wire chamber providing 62 radial measurements, a layer of plastic scintillating fibers and a "Z-chamber" providing four z-coordinate measurements [2]. The top of Fig. 1 shows a side view of the SMD inside the central tracker and the bottom shows an orthogonal view of the two radial planes of the SMD.

2. SMD ladder

The basic detector element of the SMD is a "ladder". There are in total 24 ladders, each of which is built from two separate "half-ladders". Each half-ladder is, in turn, built from two electrically and mechanically joined double-sided silicon sensors, a special low-mass Kapton cable attached to one side of a sensor pair and a front end readout electronics packet. Fig. 2 shows an inner SMD ladder.

2.1. Silicon sensors

Our silicon strip sensor design is a modification of the INFN-Pisa design [3]. Each SMD sensor is 70 mm long and 40 mm wide and made from 300 μm thick high purity ($\rho \geq 8$ kΩcm) n-type silicon. The junction side of each sensor has implantation strips every 25 μm and a readout pitch of 50 μm. The strips run parallel to the long side of a sensor and are intended to measure an $r-\phi$ coordinate.

On the sensor's ohmic side and perpendicular to the junction side strips, are n^+ implantation strips every 50 μm with interspersing p^+ blocking strips designed to interrupt the accumulated surface charge between the n^+ strips. The readout pitch is 200 μm over the polar angle θ range $|\cos\theta| = 0.93 \rightarrow 0.53$ and 150 μm over the range $|\cos\theta| = 0.53 \rightarrow 0$, where θ is measured with respect to the beam line. These strips are intended to measure an $r-z$ coordinate.

Guard rings surround the strips on both the junction and ohmic side. The active area of the strips is 70×38.3 mm^2. The total interstrip capacitance is approximately 1.3 pF/cm.

Before incorporation into a ladder, all silicon sensors are tested for leakage current and interstrip resistance. A sensor is accepted if it satisfies the three following criteria:

- The total leakage current measured at the junction side guard ring is less than 2 μA;
- No more than two junction side strips have an individual leakage current exceeding 50 nA;
- The interstrip resistance on the ohmic side exceeds 2 MΩ.

The acceptance yield for 187 sensors is 75%. Typical sensor leakage current is 5 nA/cm^2. These sensors are fabricated by CSEM [4].

2.2. Readout electronics

The front end readout chip for the SMD is the SVX-H3. This CMOS VLSI circuit [5] is an ASIC originally developed for the CDF silicon strip tracker [6] at Fermilab and chosen for the SMD because of its overall functionality

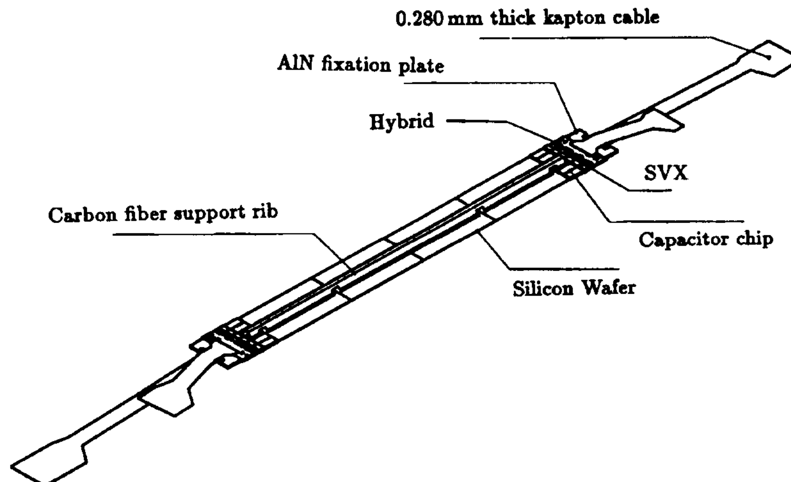

Fig. 2. An inner SMD ladder. The $r-\phi$ side with its carbon fiber stiffening rib is the top surface.

and the low power consumption of CMOS circuitry. Each of the chip's 128 channels comprises a high-gain (19 mV/fC) charge sensitive preamplifier, followed by a sample-and-hold circuit, comparator and latch. Common to the entire chip is a digital section which controls the multiplexed serial readout of all channels through a single analog output line. Up to 128 such chips can be daisy-chained together without peripheral circuitry.

The SVX chips are manufactured [7] in a 1.25 μm feature size CMOS technology. After manufacturing, the chips are tested for general functionality, gain, response linearity and noise. Only chips passing these tests are accepted for detector construction. A total of 596 SVX chips are required for the entire SMD and our acceptance yield for 1248 manufactured chips was 63%.

Each SVX chip is capacitively coupled to the silicon sensors by a custom 128 channel capacitor chip built on a quartz substrate. Each channel comprises a 150 pF capacitor and protection diodes designed to short circuit the capacitor in case of a 20 V overvoltage which may, for example, be produced by an accidental beam loss into the silicon. The capacitor chips are produced at CSEM.

The SVX chips are glued and ultrasonically bonded to an aluminum nitride (AlN) substrate. This substrate serves as a mechanical support, a low thermal impedance conduction path and as the base for standard thick film hybrid processing. The processed substrate contains surface mount resistors and capacitors for distributing chip power and sensor bias voltages and for filtering. All hybrids are subjected to extensive electrical continuity testing with the result that 114 out of 125 originally manufactured hybrid substrates [8] were considered acceptable for detector construction.

An intermediate electronics "converter" board is positioned close to each set of 12 hybrids and is electrically connected to them by thin Kapton cables. The converter contains line drivers and receivers for transmitting digital and analog signals between the hybrids and the external world. It converts TTL signals on the hybrid side to differential signals on the external world side and vice versa. The converters also pass the sensor bias voltage, hybrid power and provide voltage filtering. There are two converter boards for each pair of adjacent half-ladders, with one board for the sensor junction side and another for its ohmic side. A block diagram of the converter is shown in Fig. 3.

Analog and digital signals are sent to and from the SVX through the use of a custom optical transceiver board [9]. This "optoboard" electrically isolates the SMD front end electronics from the data acquisition system (DAQ) electronics, dramatically reducing ground loop problems and accommodating the different electric potentials of the two sensor sides. The optoboard contains an 8-bit flash analog to digital converter (FADC) to digitize the analog data from the SVX, a digital-to-analog converter (DAC) to set the threshold for the ADC and another 8-bit DAC to

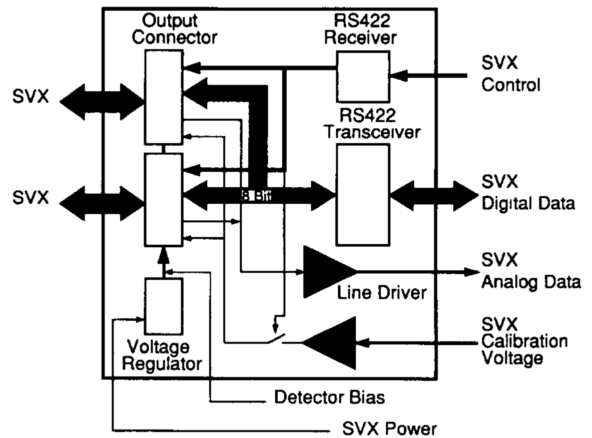

Fig. 3. Block diagram of the SMD converter.

provide an input calibration signal for the SVX. The digitized signals are then sent by Fiber Distributed Data Interface (FDDI) protocol through a 120 m long optical fiber to the optical receiver at the DAQ front end. This optical receiver contains an FDDI receiver chip which converts the light signals back into electrical ones before passing them to the remainder of the DAQ. The essential elements of the optoboard are shown in Fig. 4.

2.3. Low-mass cable

The signals from a sensor's ohmic (z-coordinate) side are rerouted from the sensor's long edge to the readout electronics by a flexible low-mass cable of novel design [10] etched from copper-plated Kapton foil. This cable allows the ohmic side front end readout electronics to be removed from the sensor's active region and thereby minimizes multiple scattering in this region, facilitates heat removal from the detector and simplifies cable routing to the external world.

Each finished cable has planar dimensions 39 mm × 143 mm. The cable substrate is commercially available [11] 50 μm thick type E Kapton foil, plated on both sides with a 2.5 μm thick copper layer. Kapton was selected because of

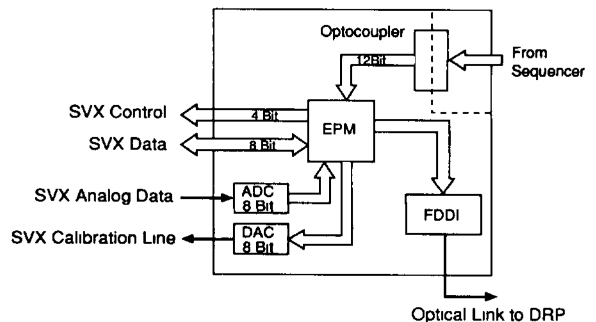

Fig. 4. Block diagram of the SMD optoboard.

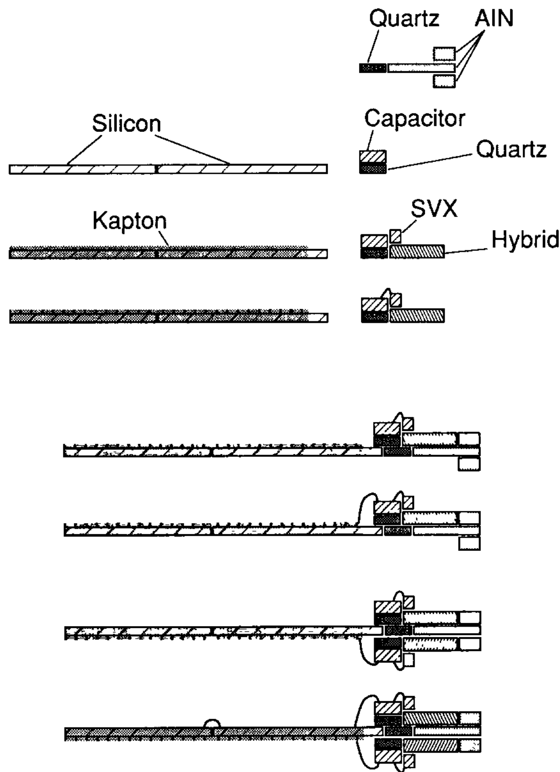

Fig. 5. The SMD half-ladder assembly sequence. The sequence flows from top to bottom.

its low dielectric constant ($\epsilon \sim 3$) which minimizes capacitive coupling between adjacent channels compared to, say, a glass substrate. Type E Kapton is desirable due to its relatively low coefficients of thermal and hygroscopic expansion. The 2.5 μm Cu thickness is a practical compromise, consistent with current etching procedures, between too thin a plating which leads to broken traces and too thick a plating which leads to short circuits. Double-sided copper plated foil is not strictly necessary but was selected as the cable substrate due to its ready availability.

After etching of the foil, L-shaped traces run the entire 143 mm length of the cable and are typically 11 μm wide. Gold-plated bonding pads for bonding between the cable and the silicon and between the cable and the front end electronics are distributed along the cable edges. Mirror bonding pads are also on the cable for conducting test bonds. Each cable reroutes a total of 744 silicon strip signals to the front end readout electronics. The average radiation thickness of the cable is 0.02% X_0.

A cable is considered electrically viable if no more than 1.5% of it traces have either a short or open circuit. In addition, the test bonds on the cable must pass certain strength tests. Applying plating and bond quality criteria, the average production yield for 48 cables was 50%. (The yield from plating alone was 90%.) Of the approximately 72000 total bonds made on the 48 low-mass cables, 0.7% were faulty.

3. Ladder assembly sequence

The basic functional unit of the SMD for both detector operation and assembly is the half-ladder. Each half-ladder is fabricated from four subunits: a silicon sensor pair, including its low-mass Kapton z side cable; two hybrid-capacitor electronic units; and the structural support of the half-ladder composed of AlN and quartz plates.

Fig. 5 details the assembly steps from the subunit level to the completed half-ladder. The precision placement and gluing of the various elements is done under a microscope

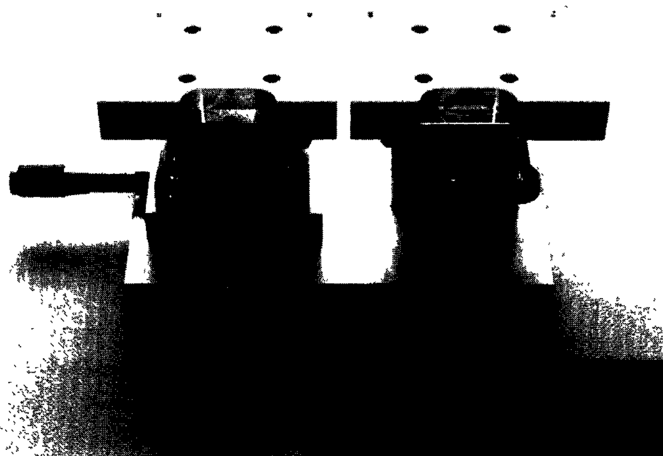

Fig. 6. Jig used for edge gluing two silicon sensors together.

with custom made vacuum jigs and mechanical displacement tables. The positional accuracy of the various elements of the half-ladder is typically better than 10 μm when precision is required for either detector assembly or installation, and in no case is worse than 25 μm.

Fig. 6 shows the jig used to edge glue the two silicon sensors of a half-ladder. Fig. 7 shows the jigs needed to glue together the half-ladder sensor pair with the AlN support piece and the z side hybrid unit. The jigs pictured in Fig. 7 include a positioning jig for the hybrid (foreground left), a hybrid transfer jig (foreground right) and the half-ladder gluing jig (background center) which allows alignment of the sensor pair with the AlN support piece. The first jig positions the hybrid with respect to the transfer jig. After application of the glue, the hybrid is then placed with the transfer jig on the half-ladder gluing jig, thus joining together the sensor pair, the hybrid, and the AlN support piece.

Two glues are used to contruct the SMD ladders. Araldite AW106 (hardener HV953U) is used for most of the structural joints and for all applications involved with the microbonding, i.e., the Kapton z side cable and capacitor chips. A good thermal conducting glue, Stycast 2850FT (hardener 24LV) [12], is used to join the pieces of the AlN support subunit and to glue this subunit to the hybrids. This glue ensures a good thermal path between readout electronics and the cooling provided on the support structure. The quartz composing the capacitor chips and their premounting plate and the quartz piece between the AlN support and the silicon sensor thermally isolate the latter from the readout electronics.

Particular care was taken during the gluing to control thickness and uniformity, both of which are vital for the microbonding and for achieving the final precision of the half-ladder dimensions. This was accomplished due to the high precision of the assembly jigs (a planarity tolerance ≤ 5 μm) and the use of a pressurized automatic glue dispensing system.

A total of 4564 microbonds are needed to make the electrical connections on each half-ladder. Fig. 5 shows the location of the microbonds between capacitor chips and SVX, between the silicon wafer output pads (z side) and the z side cable, between the z side cable and capacitor chips, between silicon output pads (ϕ side) and capacitor chips, and between the two silicon wafers (ϕ side). A second series of vacuum jigs was constructed to support the half-ladder and the different subunits on the bonding machine [13].

Full SMD ladders are formed by joining two half-ladders with a molded carbon fiber/epoxy support rib of 300 μm thickness and an overall length of 314 mm. The rib is glued to the ϕ surface of the four silicon sensors of the ladder as well as to the surface of the quartz capacitor chips. It is isolated from the ladder components by a 0.50 mm thick kapton sheet and grounded to the r–ϕ side readout of the detector. The overall length of the completed ladders is 400 mm.

4. Sensor biasing and detector power supply system

The sensor strips are biased by applying voltages to the guard rings on both the junction and ohmic sides, through the punchthrough and electron accumulation layer channeling mechanisms, respectively. The potential difference between sensor sides varies from 30 to 50 V. The r–ϕ measuring strips, parallel to the beam and the longitudinal magnetic field of L3, are biased to collect the holes, minimizing the effects of Lorentz drift on spatial resolution.

Fig. 7. Jigs used for gluing hybrids, AlN support piece and sensors together. See text for an explanation.

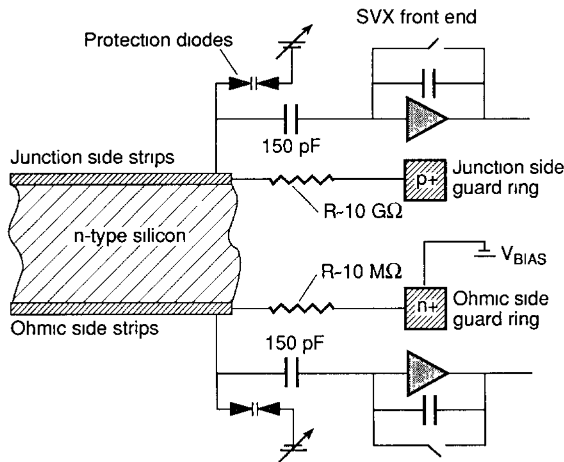

Fig. 8. Equivalent circuit for biased SMD sensors.

The power and bias voltages supplied to the sensors, SVX chips, converters and optoboards are provided by a custom computer controlled modular power supply system [14]. In this system, the potentials applied to the z side and $r-\phi$ side electronics float independently of one another. Floating the z side electronics, referenced to the silicon bias potential, decouples it from the working potential of the data acquisition system. Floating the $r-\phi$ side electronics, although not strictly necessary, is done to reduce potential ground loop problems. The sensors and front end electronics of each pair of adjacent half-ladders require 19 distinct voltage channels. Each channel has its voltage magnitude, polarity, ramp rate and permissible overcurrent separately adjustable and all parameters can be continuously monitored by a dedicated personal computer. A total of six power supply crates bias and power the SMD.

Fig. 8 shows the equivalent electrical circuit of a biased sensor, including protection diodes, effective capacitances and the front end of the readout electronics.

5. Data acquisition

Readout of the SMD silicon strips is done in a semi-parallel fashion. The 48 pairs of hybrids are read out simultaneously while the strips in the 12 SVX chips of each hybrid pair are read out serially by a token passing scheme at an adjustable rate of ~ 0.5–1.5 MHz. All SMD strips are read out and no zero suppression is done at the level of the SVX chip. For each of the 128 channels of an SVX chip, the analog value of the collected charge for that channel, along with the strip ID and the chip ID of the strip are first transferred as TTL signals to the converter, converted to differential signals and driven to the optoboard where all data are converted to digital light signals. The signals are then sent to the optical receiver at the DAQ system front end where they are eventually received by a custom VME-based data reduction processor (DRP).

Fig. 9 shows a block diagram of the DRP. This module is a hardware filter which uses one of two user selectable algorithms to suppress signals unlikely to be due to charged particle passage through the silicon. Only signals from candidate hit strips are transferred to the general L3 data stream. The total set of the 48 single-width DRPs required for the SMD are grouped together into three crates of 16 DRPs each. Each VME crate is controlled by a custom crate master which transfers the sensor data from the DRPs to the L3 data stream and downloads programs to the DRPs.

The DRP version used for the SMD is a modification of the design used elsewhere in the DAQ of L3's central tracker [2] and is built around a Texas Instrument microprocessor TMS 99105. It has a 32 kiloword random access memory (RAM) for programs, data and multi-event buffering, and two bus systems for internal data handling and connection to the outside world. One is the standard VME data and access bus system and the other is a special bus system which distributes various control signals (clock, sample, fast clear and trigger level 1 data). During run time, a dual port memory of 4 kilowords is used for communication and data transfer between the DRP and its crate master.

A DRP's front end is a fast direct memory access (DMA) port specially designed for the SMD readout. Two different DMA transfer modes can be used. First, one can run the port in full readout mode so that two words per sensor strip are written into the DRP main memory. The high byte of the first word contains the SVX chip identifier

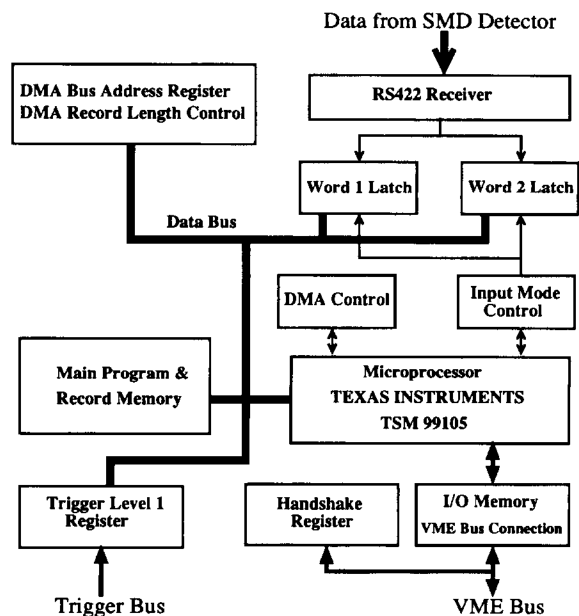

Fig. 9. Block diagram of the SMD data reduction processor.

while the low byte is not used. The high byte of the second word is the strip address and the low byte contains the ADC amplitude of the corresponding strip. In the second or "reduced input mode", the chip identifier and the strip address are skipped by the DMA hardware and two consecutive strip ADC amplitudes are assembled into one 16 bit word and written into the DRP memory. This mode allows a buffering of up to 18 triggers and saves considerable memory. The DMA mode is set during DRP initialization.

Prior to data taking, a run of several hundred internally generated triggers is done to determine common mode noise (*CMN*) for each SVX chip, along with pedestal values (*Ped*) and their variance for each SVX strip. In addition, multiple pedestal taking with different injected test charges to each strip is done to determine a linear gain fit for each strip. These parameters are stored in the DRP for use by its data reduction algorithms and are also written to external data base memories.

Each DRP uses one of two algorithms to filter the raw data before passing it through its crate master to the general L3 data stream. The algorithm is set during module initialization and can be set on an individual DRP basis:

Neighbor mode. In a first pass through the raw data, the DRP computes a common mode noise for each SVX. In the second pass, only strips with an ADC amplitude > $(Ped + CMN + Thr)$ are inserted with their neighbors into the output record. Here *Thr* is an experimentally adjustable threshold which varies from DRP to DRP and typically corresponds to about 1/10 the size of a signal from a minimum ionizing particle. A zero record is generated if no hit is present. A typical data reduction factor of 8–10 is achieved.

Differential mode. A local background (β) is calculated for each SVX strip using 2^{δ} strips, where $\delta (1 \leq \delta \leq 5)$ is the number of strips on each side of the strip in consideration. All strips with an ADC amplitude $> (Ped + Thr + \beta)$, along with their neighbors, are inserted into the output record. A zero record is generated if no hit is present. A typical data reduction factor of 8–10 is achieved.

All data reduction algorithms take care to appropriately handle defective strips. For test purposes, any DRP can be used in a mode with no filtering algorithm applied to the raw data before it is passed unchanged to the general L3 data stream.

The synchronization between the readout of the SMD and the external L3 triggers is controlled by a specially designed VME compatible "sequencer" module which produces the appropriate signals to control the transfer of the SVX data to the DRPs and communicates to a standard VME bus and the optoboards. The sequencer has a one level pipeline structure and is built around a microprogram controller and a 32-kilobit × 64 bit fast RAM. The lower 32 bits of the RAM contain the microcode that controls the internal operations of the sequencer. An 8-to-1 multiplexer allows sequencer address branching based on the condition

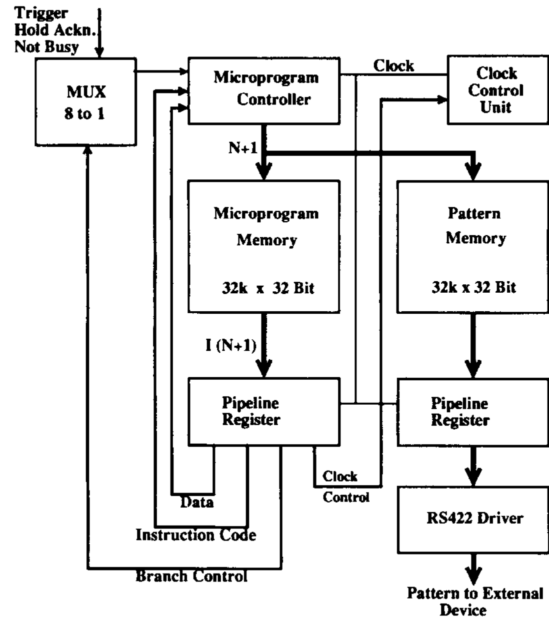

Fig. 10. Block diagram of the SMD sequencer module.

of up to eight external signals. The upper 32 RAM bits contain the bit patterns sent to the outside world and the 32-kbit RAM depth allows up to eight microprograms to be stored. These microprograms contain the patterns necessary for pedestal taking, calibration and data taking. A block diagram of the sequencer is shown in Fig. 10.

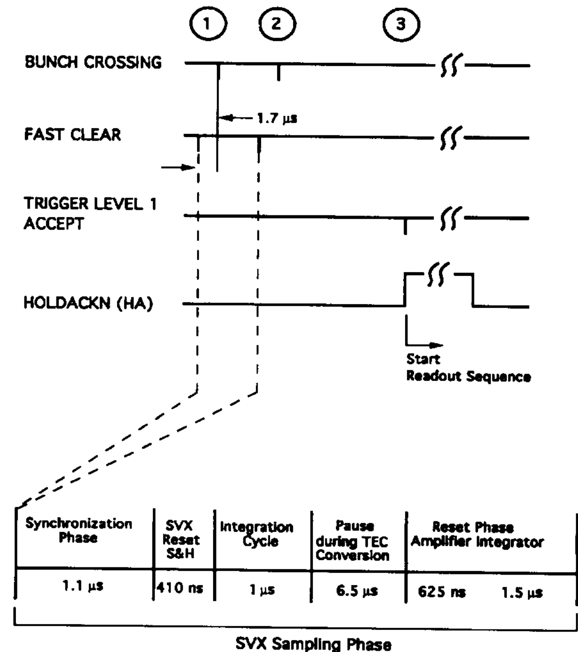

Fig. 11. Simplified timing diagram for the SVX sampling phase. See text for an explanation.

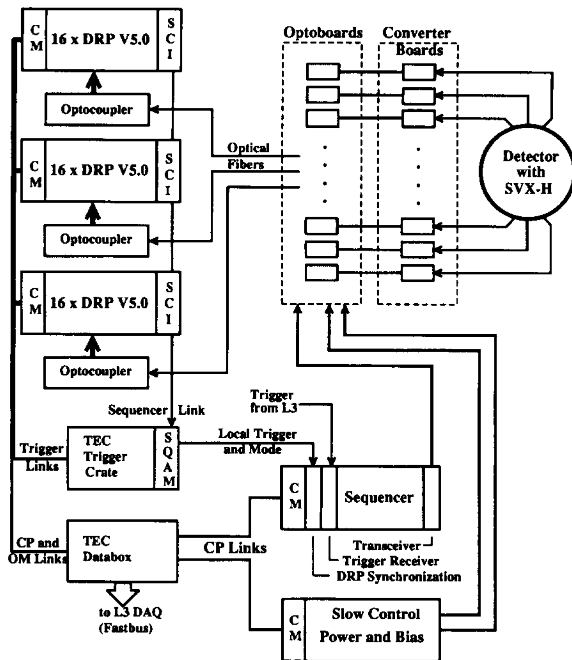

Fig. 12. Block diagram of the SMD readout chain.

A simplified timing diagram of the SVX sampling phase as supervised by the sequencer is shown in Fig. 11. Each cycle starts with a fast clear signal which arrives from the L3 trigger system at the sequencer 1.7 μs before the LEP bunch crossing of 11.1 μs period (case 1). The sequencer responds and dispatches its appropriate bit patterns over a long cable to the SVX, a process taking 1.1 μs. An additional 410 ns is required to reset the sample and hold (S&H) circuitry of the SVX. Next, the 1 μs long integration cycle of the SVX begins. The system then pauses for 6.5 μs during the TEC conversion phase to avoid generating noise in the remainder of the central tracking system. Afterwards, one of the two possibilities labeled as 2 or 3 in the figure will occur. In case 2, a fast clear dispatched from the L3 trigger system arrives at the sequencer before the next bunch crossing and the SVX sampling phase begins all over again. In case 3, no fast clear arrives so the sampling phase finishes without interruption and the sequencer then awaits a "trigger level 1 accept" signal. When the sequencer receives the trigger level 1 accept, it begins to read out, one strip at a time, the analog sensor data via the converter to the FADC stored in the optoboard. During this time, a "hold acknowledge" signal is sent to the sequencer by the DRPs for the duration of time the DRPs are processing raw data. Fig. 12 summarizes the overall SMD readout chain.

6. Mechanical support

The mechanical support structure for the ladders and the converters is a 1 m long cylindrical tube split lengthwise into two symmetric halves. The tube is made from a laminate of 3 mm thick NOMEX honeycomb core glued between 315 μm thick aluminized carbon fiber skins. The skins are layed up from individual sheets in a manner to minimize the support structure's coefficient of thermal expansion.

The split tube construction permits easy mounting of the inner layer ladders and the installation of the SMD around the beam pipe at the interaction point. Each half-tube is made from three separate carbon fiber sections joined by two aluminium alloy half-rings. Similar half-rings are at the far ends of the split tube. The interior half-rings provide the ladder mechanical fixation and contain cooling channels. The outer two half-rings are used for attaching the SMD to the inner wall of the TEC.

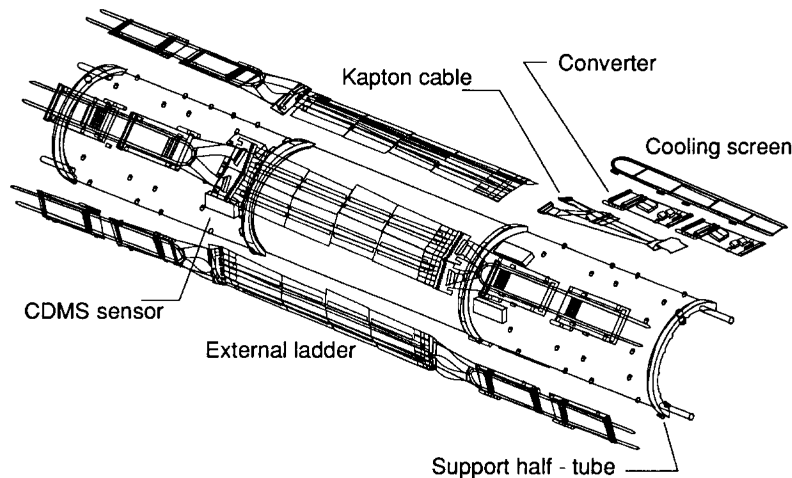

Fig. 13. Partially exploded view of an SMD instrumented half-tube.

A thin hemi-cylindrical laminate built from a 0.5 mm thick cardboard core glued between 30 μm sheets of aluminized mylar serves as an electromagnetic and thermal screen. One such screen is attached to the outside of each half-tube prior to installation of the SMD inside the TEC.

After installation around the beam pipe, the half-rings of the split tube are pinned together so that the support structure recovers almost completely the full mechanical properties of an unsplit tube. A finite element calculation predicts that the maximum deflection of the support tube under load is 20 μm. The tube is positioned inside the inner flange of the TEC by electrically insulating ruby spheres placed at three equidistant points around each of the tube's end rings.

The radiation thickness of the tube for normally incident particles is 0.3% X_0. By comparison, the 1.5 mm thick beryllium beam pipe is 0.4% X_0 thick.

The ladders are attached to the split tube at two mean radii, $r = 60.7$ mm and $r = 77.5$ mm, with the carbon fiber material positioned between the two ladder layers. The inner ladders are mounted with their axes parallel to the beam direction but are crenellated with a 5% overlap as an alignment aid. The outer ladders are mounted so that their half-ladders are tilted with a stereo angle of 2° with respect

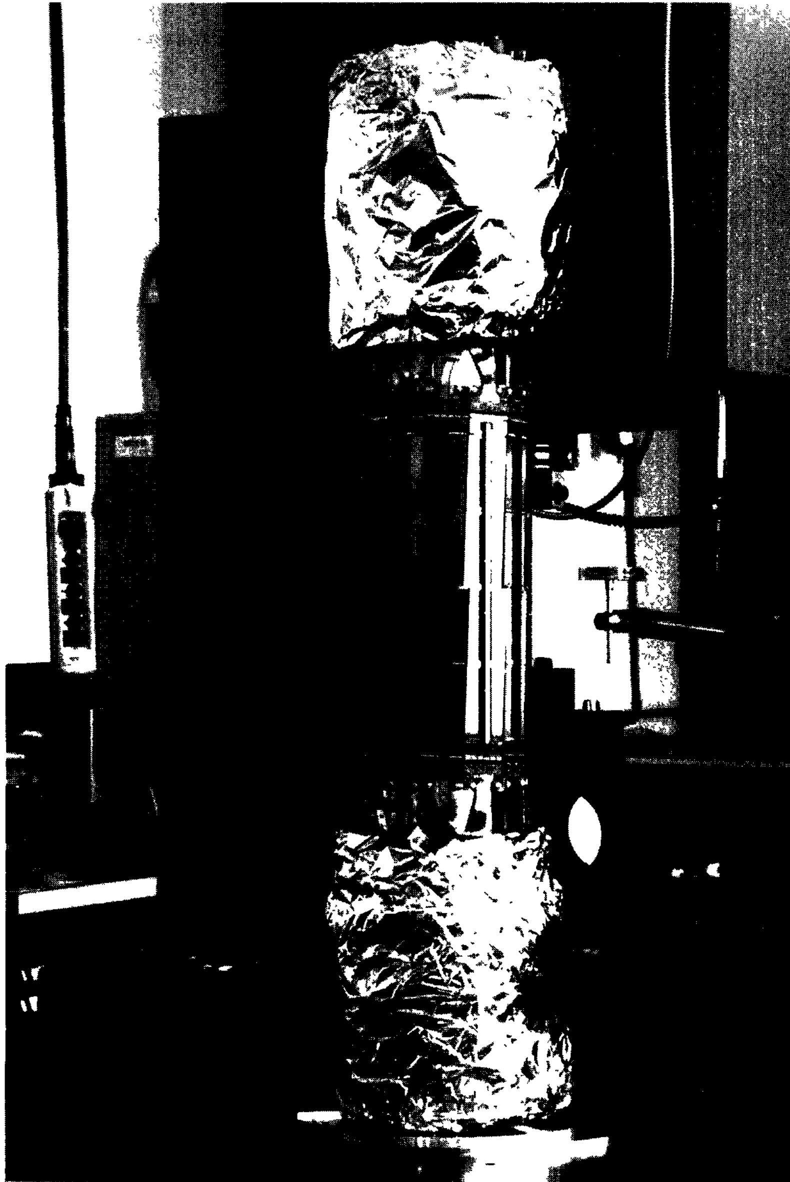

Fig. 14. The SMD positioned vertically prior to installation.

to the beam direction to facilitate pattern recognition. These ladders are not crenellated.

Fig. 13 shows a partially exploded view of one-half of the support tube. Three exterior ladders with their associated readout electronics are visible. Fig. 14 shows the SMD positioned vertically on a metrology table. The exterior ladders are visible while a protective foil covers the converters.

7. Detector cooling

To optimize track position resolution, thermally induced disturbances to the mechanical stability of the silicon sensors and to the temperature stability of the TEC drift gas must be minimized by efficiently exhausting the 200 W of heat dissipated by those SMD components inside the TEC envelope. This heat is generated equally between the hybrid circuits and the converters and is approximately uniformly in azimuth.

The hybrids are cooled by a special, chilled water-based coolant [15] flowing through a channel machined into the aluminum alloy ladder support rings. The rings are in good thermal contact with the AlN hybrids, directly at the ladder fixation points and through heat sink compound [16] applied closer to the SVX chips. The converters are cooled by chilled thin aluminum alloy sheets positioned about 1 mm above them. Each sheet is chilled by flowing coolant through 2.5 mm diameter aluminum alloy pipes attached along its circumference. The coolant for the sheets is the same as for the hybrids and a total flow of about 300 l/hour cools the entire SMD. Common supply manifolds mounted on the support tube simplify the plumbing and equalize the coolant flow to the four parallel flange and 24 parallel converter cooling circuits. All circuits are under partial vacuum to prevent fluid loss if a leak develops.

The SMD cooling system is designed to maintain the TEC inner wall temperature at a stable working point (18 ± 0.1°C) and the readout electronics temperature at some constant arbitrary temperature less than about 45°C. The SMD temperature is monitored by 26 platinum wire resistance thermometers [17] distributed over the support structure. These thermometer readings are digitized by an ADC and monitored. The temperature stability of the SMD during data taking is better than 0.2°C. Temperature sensors on the inner wall of the TEC indicate a TEC temperature stability of 0.1°C during data taking periods.

8. Displacement monitoring systems

Since a reconstructed track in the central tracker will be formed from information derived from both the SMD and the TEC, accurate and efficient reconstruction requires a knowledge of the time-dependent relative displacements between these two tracking detectors. Hence, we have built two independent systems to measure the relative angular and translational displacements of the SMD with respect to the TEC. One system is a laser displacement monitoring system (LDMS) and the other is a capacitive displacement monitoring system (CDMS). These two measuring systems provide a degree of complementarity and redundancy in both measurement technology and coordinate sensitivity. Systems based on the same principles of operation as the CDMS and LDMS have been designed and implemented in other experiments [18].

The LDMS is built from a laser diode which produces 50 ns long pulses of infrared ($\lambda = 905$ nm) light and a light transmission system which includes an optical fiber of core diameter 400 μm that transmits the laser light to a set of 50 μm core diameter fibers. These fibers transmit the light to optical heads, glued rigidly to the inner wall of the TEC. Each optical head redirects the light through holes in the SMD's external shield onto the silicon sensors, striking the sensors at both normal and 45° incidence, illuminating several neighboring readout strips. The resulting signal is read out by the normal front end electronics. A total of 44 light spots strike the outer sensor layer.

Test beam results [19] show that this scheme allows reconstruction of the light spot centroid to an accuracy of a few microns. A change in the centroid of the light spot indicates relative transverse motion between the SMD silicon sensors and the TEC.

The CDMS is an alternative technology to the LDMS and is more sensitive to radial than to transverse displacements. A single channel of the CDMS utilizes a sensor mounted on the SMD facing a grounded electrode ("ground target") mounted on the TEC inner wall. The sensor is excited by an AC current of constant magnitude and a 15 kHz frequency and the voltage drop between the sensor and ground target is amplified, rectified and filtered to produce a nearly DC voltage which varies inversely with the capacitance of the sensor and the ground target. The amplifier gain is set and the ground target contoured in such a way as to achieve a typical sensitivity to radial displacements of 2.5 mV/μm and of 0.7 mV/μm for transverse displacements. The detailed dependence of output voltage on displacements between the sensor and ground target is determined by calibration prior to installation. The sensors and associated electronics are obtained commercially [20].

For the entire SMD, six triplets of sensors are used. These triplets are mounted on the SMD support tube and are located in z between the end of the SMD ladders and the converter boards. Two triplets are sensitive to displacements Δr and Δz and four triplets are sensitive to displacements in Δr and $r\Delta\phi$. Using three sensors to measure displacements in two dimensions provides redundancy for reducing the effects of electronics noise and drift. In addition, two channels, for which the sensor–ground target geometry is fixed, are used to monitor and correct for electronics drift. The DC voltage output from each CDMS

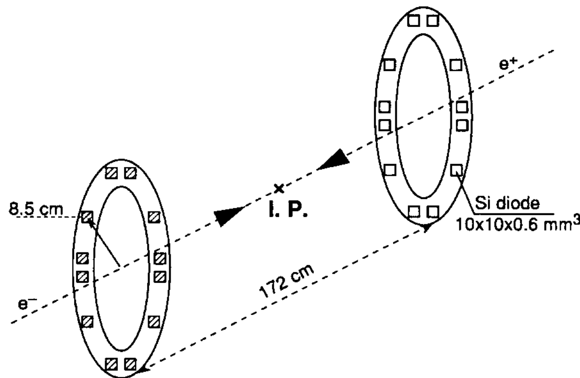

Fig. 15. Schematic diagram of the SMD radiation monitoring system surrounding the L3 interaction point (IP).

channel is digitized using a CAMAC ADC/MUX system [21] and read out once per minute. The long-term resolution of a typical triplet, as achieved in prototype bench tests and under actual experimental conditions, is 1–2 μm in the radial direction and 5–10 μm in the transverse direction.

9. Radiation monitoring system

To help protect the SMD against a potentially catastrophic beam loss into the silicon sensors, we have installed a set of radiation monitoring silicon diodes [22] in the vicinity of the SMD designed to send a beam dump signal to LEP control if the radiation dose rate in the diodes exceeds a pre-defined threshold. This system also allows an online monitoring of the dose rate.

At 86 cm on each side of the interaction point are 12 1cm × 1cm × 600 μm thick silicon diodes distributed in a circle of radius 85 mm coaxial with the beam direction (see Fig. 15). The radiation dose for each sensor is recorded continuously at various gains such that the dynamic range for the full set of sensors is 3 mrad/hour to 20 Mrad/hour. A beam dump signal is generated if the dose rate from sensors on both sides of the interaction point exceeds 0.6 rad/s for at least 300 μs.

Table 1
General SMD characteristics

Number of double-sided radial layers	2
Total area of instrumented silicon	0.25 m^2 (×2)
Polar angle coverage	$\|\cos\theta\| \le 0.93$
Azimuthal angle coverage	2π
Total number of readout channels	72576
Front end readout ASIC	SVX-H3
Front end power consumption	1.3 mW /channel
Front end noise	1360 ENC
Front end readout rate	0.5–1.5 MHz
Front end integration time	1–1.5 μs
Readout buffer size	18 triggers maximum
Expected $r-\phi$ side single-track resolution	7 μm
Expected $r-z$ side single-track resolution	14 μm
Radiation thickness at normal incidence	1.2% X_0
Total power dissipated	~ 200 W
Cooling fluid and flow rate	H_2O at 300 l/h
Relative displacement monitoring systems	capacitive and light spot
Expected radial displacement sensitivity	~ 5 μm
Expected transverse displacement sensitivity	~ 5–10 μm

10. Conclusion

We have described the design and construction of the L3 silicon microvertex detector installed at the beginning of the 1993 LEP data taking year. A summary of the principal design parameters of this detector are listed in Table 1. The SMD will be debugged during running at the Z resonance in 1994 and will significantly improve L3's tracking capability for W-pair physics at LEP200.

Acknowledgements

This work is dedicated to the memory of Vanko Krastev and his family.

We are indebted to P. Baehler, P. Béné, D. Bernier, S. Bizzaglia, L. Bosisio, P. Bouvier, A. Christinet, B. Clerc, A. Diforni, P. Emonet, A. Folley, C. Gingu, C. Haber, F. Masciocchi, R. Morino, J.R. Moser, P. Petiot, M. Plasse, V. Postolachi, A. Roulet (EPFL), H. Suter, G. Viollat, J. Wear, M. Weber, P. Weilhammer, M. Willenbrock and the NIKHEF Workshop who provided valuable technical assistance. This work was supported by the Fonds National Suisse pour la Recherche Scientifique, the German Bundesministerium für Forschung und Technologie, the Hungarian OTKA fund (contract no. 2970), the Istituto Italiano di Fisica Nucleare, the National Science Council (Republic of China), the US Department of Energy and the US National Science Foundation.

References

[1] L3 Collaboration, CERN-LEPC 91-5, LEPC P4-Add. 1 (1991); and A.S. Schwarz, Phys. Rep.238 (1994) 1.
[2] F. Beissel et al., Nucl. Instr. and Meth. A 332 (1993) 33.
[3] G. Batignani et al., Nucl. Instr. and Meth. A 277 (1989) 147.
[4] Centre Suisse d'Electronique et de Microtechnique S.A., Maladière 71, Case Postale 41, CH-2007 Neuchâtel, Switzerland
[5] S. Kleinfelder et al., IEEE Trans. Nucl. Sci. NS-35 (1988) 171.
[6] W.C. Carithers et al., Nucl. Instr. and Meth. A 289 (1990) 388.

[7] United Technologies Microelectronics Center, 1575 Garden of the Gods Road, Colorado Springs, CO 80907, USA.
[8] Promex Inc., 3075 OakMead Village Drive, Santa Clara, CA 95051, USA.
[9] O. Adriani et al., Nucl. Phys. B. (Proc. Suppl.) 32 (1993) 480.
[10] D. DiBitonto et al., Nucl. Instr. and Meth. A 338 (1994) 404.
[11] Polyonics Corp., 112 Parker St., Newbury, MA 01950, USA.
[12] Araldite AW106 (HV953U), Ciba-Geigy, S.A., CH-4002 Basel, Switzerland.Stycast 2850FT (24LV), W.R. Grace Co., 77 Dragon Ct., Woburn, MA 01888, USA. Thermal conductivity $\kappa = 1.44$ W/m K.
[13] Model 4123. Kulicke and Soffa Industries, Inc. 507 Prudential Road, Horsham, PA 19044 USA.
[14] SY527 power supply system, CAEN, Via Vetraia 11, 55049 Viareggia, Italy.
[15] Kemazur 1636, Degrémont S.A., 183 Avenue du 18 Juin 1940, 92508 Rueil-Malmaison, Cedex, France.
[16] Dow Corning Compound 340, Dow Corning, Inc., PO Box 994, Midland, MI 48686–0994, USA.
[17] Part No. PT1000, Minco Products Inc., 7800 Commerce Lane, Minneapolis, MN 55432, USA.
[18] N. Bingefors et al., Nucl. Instr. and Meth. A 328 (1993) 447; M. Caccia et al., Nucl. Instr. and Meth. A 315 (1992) 143; A. Breakstone, Nucl. Instr. and Meth. A 305 (1991) 39.
[19] A. Adam et al., Nucl. Instr. and Meth. A 344 (1994) 521.
[20] Capacitec, Inc., 87 Fitchburg Rd., Ayer, MA 01432, USA.
[21] ADC (part No. E205) and MUX (part No. E220), DSP Technology Inc., 48500 Kato Road, Fremont, CA 94538, USA.
[22] Hamamatsu S1723–06, Hamamatsu, Inc., 360 Foothill Rd., PO Box 6910, Bridgewater, NJ 08807–0910, USA.