The Medipix3 Prototype, a Pixel Readout Chip Working in Single Photon Counting Mode with Improved Spectrometric Performance

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***Abstract*–A prototype pixel detector readout chip has been developed with a new front-end architecture aimed at eliminating the spectral distortion produced by charge diffusion in highly segmented semiconductor detectors. In the new architecture neighbouring pixels communicate with one another. Charges can be summed event-by-event and the incoming quantum can be assigned as a single hit to the pixel with the biggest charge deposit. In the case where incoming X-ray photons produce fluorescence – a particular issue in high-Z materials – the charge deposited by those fluorescent photons will be included in the charge sum provided that the deposition takes place within the volume of the pixels neighbouring the initial impact point. The chip is configurable such that either the dimensions of each detector pixel match those of one readout pixel or detector pixels are 4 times greater in area than the readout pixels. In the latter case event-by-event summing is still possible between the larger pixels.**

As well as this innovative analog front-end circuit, each pixel contains comparators, logic circuits and two 15-bit counters. When the larger detector pixels are used these counters can be configured to permit multiple thresholds in a pixel providing colour information.

The prototype chip has been designed and manufactured in an 8-metal 0.13µm CMOS technology. First measurements show an electronic pixel noise of ~ 72 e- rms (Single Pixel Mode) and ~ 140 e- rms (Charge Summing Mode).

I. Introduction

PIXEL detector advances open up new possibilities in many fields of science. Modern High Energy Physics (HEP) experiments use pixel detectors for tracking systems where excellent spatial resolution and high signal-to-noise ratio are required for accurate track reconstruction. Many groups are working worldwide to adapt the hybrid pixel technology to other fields such as medical X-ray radiography, protein structure analysis or neutron imaging.

The innovation in monolithic and hybrid semiconductor 'micropattern' pixel detectors for tracking in particle physics was actually to fit pulse processing electronics and associated digital circuitry on a pixel area of much less than 1 mm^2, with a power consumption in the µW range while retaining the characteristics of a traditional nuclear amplifier chain [1]. The evolution of hybrid pixel detectors is intimately related to CMOS technology advances following Moore's Law [2]. The driving force behind this close relationship is continuously improving performance, high integration density, low power consumption and reasonable cost using an industry standard technology. This allows pixel detector Application Specific Integrated Circuit (ASIC) designers to implement more functionality per pixel while maintaining the compact pixel area when a more downscaled process is used.

Two generations of the Medipix chip have been successfully developed. The Medipix1 chip [3] demonstrated the principle of the photon counting approach, which provides a high dynamic range and is practically free of nonphotonic noise. The pixel dimensions were 170µm x 170µm and each pixel contained approximately 400 transistors. It was implemented in 1µm CMOS process. The Medipix2 [4] pixel dimensions are 55µm x 55µm. It is implemented in a 0.25µm CMOS technology. It contains approximately 500 transistors per pixel.

The performance of the Medipix2 imaging system is limited by the sharing of charge between neighbouring pixels. The Medipix3 prototype chip implements an architecture aimed at eliminating the spectral distortion produced by the charge sharing process. It has been developed in an 8-metal 0.13µm CMOS technology. The chip includes an 8x8 matrix of pixels Each pixel contains around 1100 transistors and occupies a total area of 55µm x 55µm.

Section II discusses the motivation to develop a new Medipix architecture and presents simulation results that validate the new system. Section III shows the architecture in detail. Section IV presents the measurements and electrical characterization of the chip.

II. Motivation

Charge diffusion in segmented semiconductor detectors produces a distortion in the energy spectrum seen by an individual pixel [5]. The influence of this effect on the spectrum increases as the pixel pitch is decreased with respect to the thickness of the detector material. As a consequence, there is a trade-off between spatial resolution and energy resolution in single particle counting systems. Fig. 1 shows the simulation of a 300µm thick silicon sensor bump bonded to a 55µm pitch pixel detector readout chip. The simulation has been done with a 10keV monochromatic photon beam. The spectrum seen by one pixel using a traditional readout architecture with a front-end electronics noise of 100e^- rms is

Manuscript received November 17, 2006. This project has been undertaken in the framework of the Medipix2 Collaboration, http://www.cern.ch/MEDIPIX

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shown in blue. Many photons deposit charge at or near the pixel borders. This charge then diffuses during collection and is shared between adjacent pixels resulting in a low energy tail that limits the energy resolving potential of the system. The spectrum seen by one pixel with the new architecture is shown in red. In this new architecture, the charge information is reconstructed by grouping pixels into clusters of four, summing the charge collected in each cluster, and associating the photon with the summing circuit with the largest charge deposition.

The "charge sharing" tail means that any residual threshold variation between pixels produces a fixed pattern image noise which varies dependent on energy spectrum [6].

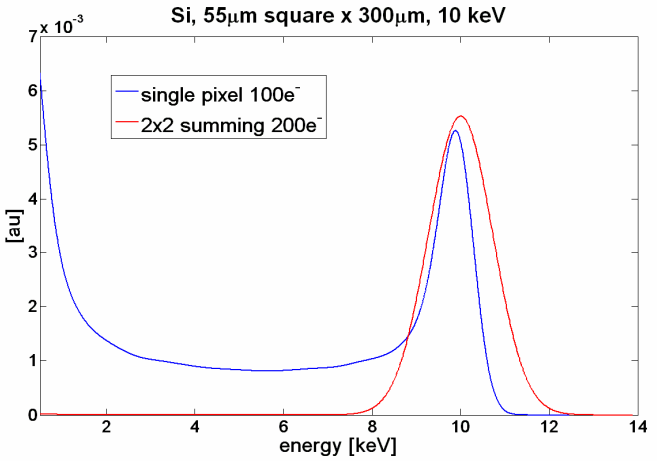

Fig. 1. Simulation of a 300µm thick Si sensor bump bonded to a 55µm pixel pitch detector readout. The spectrum seen by one pixel in a traditional system (pixel front-end with 100e$^-$ rms noise independent of neighbouring pixels) is shown in blue. In red, the spectrum observed with the new electronics whereby 4 pixels contribute to the total charge sum is shown. The noise of the individual pixels is added in quadrature.

When high-Z materials are used to detect X-rays in the 10's of keV region, fluorescent photons are often produced and they deposit charge at some distance from the primary interaction [7]. Fig. 2 shows simulation results of a 300µm thick GaAs sensor bonded to a 55µm pixel pitch detector readout circuit. The simulation in this case has been done with a 20KeV monochromatic photon beam. The influence of the fluorescence photons of Ga (9.2KeV) and As (10.5KeV) in the spectrum is shown. The mean free path of these is comparable to the pixel pitch being 42.62µm for Ga, and 15.62µm for As. The effect of these photons on the energy spectrum seen using the traditional architecture is clearly evident in the blue curve. The new architecture includes in the reconstructed energy, the charge deposited by the fluorescence photons provided the deposition takes place within the sensor volume of the pixels neighbouring the impact point. This has a beneficial impact on the spectrum seen using the new architecture (red curve).

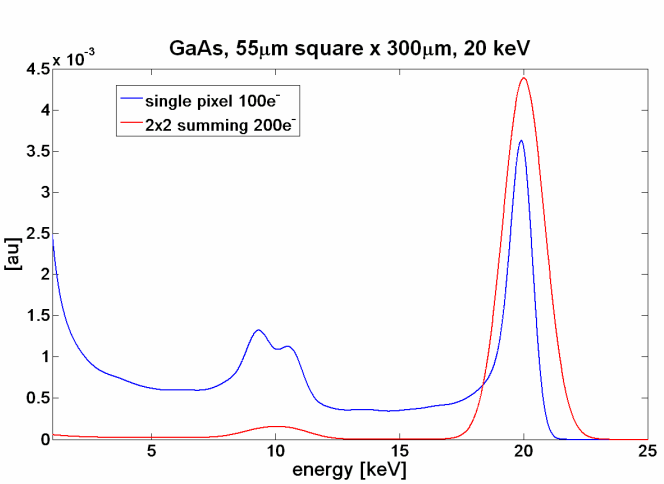

Fig. 2. Simulation of a 300µm thick GaAs sensor bump bonded to a 55µm pixel pitch detector readout. The two bumps in the spectrum for the traditional architecture show the effect of the fluorescence photons: Ga (9.2KeV) and As (10.5KeV). The mean free path of these is comparable to the pixel pitch being 42.62µm for Ga, and 15.62µm for As. In the new architecture the charge deposited by the fluorescence photon will be included in the charge sum provided the deposition takes place in the sensor volume of the pixels neighbouring the initial conversion.

III. Chip and Pixel Description

The Medipix3 prototype chip (Fig. 3) has been designed and manufactured in 0.13µm CMOS technology with eight metal layers. This allows a high degree of interconnectivity between pixels and the implementation of more functionality while maintaining a compact pixel area. Two pixel matrices have been implemented: an 8x8 pixel matrix and a small test matrix for circuit debugging purposes. Two pixels with a different layout design have been implemented to test special transistors offered by the foundry. The analog and the digital circuitry have been designed to operate with independent 1.5-V power supplies.

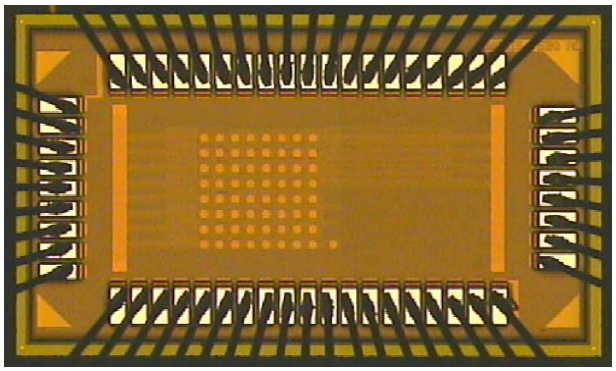

Fig. 3. Medipix3 prototype chip die. The 8x8 matrix is implemented in the left hand side of the die. In the right hand side of the chip a small matrix for digital debug is implemented.

The block diagram of the pixel schematic is shown in Fig. 4. The charge collected on a pixel is integrated by a Charge Sensitive Amplifier (CSA) on a feedback capacitance whose design value is 14fF (gain of 11.44mV/Ke$^-$). The CSA is based

on the Krummenacher architecture [8] and can handle both positive and negative input charges. A test injection capacitance of 4.8fF is provided in each pixel in order to permit full testing of the chip functionality. Seven different test pulses are available to allow injection of different charges in adjacent pixels. Those allow the testing of the all the modes of operation of the system. The output of the CSA is filtered by means of a first order semi-gaussian shaper with a time constant of ~ 100 ns, which acts both as a transconductance and as a noise filter. The shaper also AC couples the output of the preamplifier to the rest of the circuit (eliminating the offset produced by the mismatch of the transistors in the preamplifier feedback loop and thus relaxing the dimensions of those transistors) and makes the system less sensitive to the variations of the preamplifier characteristics. Furthermore the shaper generates eight currents whose amplitudes are proportional to the charge collected on the input electrode.

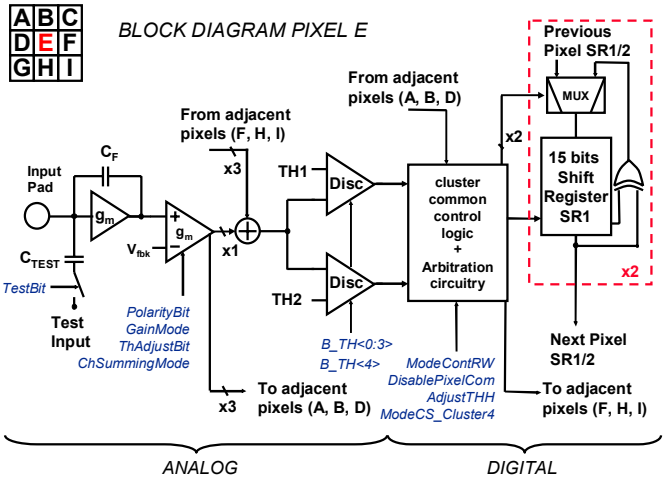

Fig. 4. Medipix3 pixel cell schematic.

The currents generated in the shaper are sent to nodes common to a cluster of four pixels, the adding nodes being located effectively at each pixel corner. As there are two discriminators associated with each pixel, there are two adding nodes per pixel corner.

Note that the chip can be used either in *Single Pixel Mode*, *Charge Summing Mode* or *Colour Mode* (Table I). In *Single Pixel Mode* the summing nodes are fed with the output of a single pixel only.

The discrimination process is done by applying an offset (threshold) to the sum of the four currents. Each summing node is connected to its own independent discriminator. Each discriminator has a 4-bit Digital-to-Analog Converter (DAC) to reduce the threshold dispersion caused by mismatch in the transistors that provide the threshold and the summing currents. Once the discriminator signal is active the charge is assigned to the summing circuit with the largest charge sum in the local neighborhood. The charge assignment decision is based on the operation of a system of arbitrators. Arbiter circuits decide between two requests (inputs), activating an acknowledgement for only one request even when they arrive simultaneously. The typical arbiter structure is based on a RS flip-flop with a simple structure to eliminate glitches at the output and filter the metastable state caused when two inputs arrive closely spaced in time.

TABLE I
FRONT END OPERATING MODES

Front End Operating Mode	Pixel Size	Area of charge collection	Number of Thresholds
Single Pixel Mode	55μmx55μm	55μmx55μm	2 (1 in Sim RW)
Charge Summing Mode	55μmx55μm	110μmx110μm	2 (1 in Sim RW)
Colour Mode	110μmx110μm	220μmx220μm	5 (implemented in prototype)

When a given discriminator wins the arbitration decision, a pulse is fed to a shift register which is controlled by the *Shutter* signal. When the *Shutter* is high the shift register is configured as a 15-bit pseudo-random counter which counts the discriminator pulses (with a dynamic range of 32768 counts). When the *Shutter* is low the data can be shifted from pixel to pixel and read out externally.

Because the pixel contains two shift registers (one associated with each threshold) the pixel readout can be configured for *Simultaneous Read-Write* operation whereby the *Shutter* signal seen by one shift register is inverted with respect to the *Shutter* seen by the other shift register for a given pixel. This makes simultaneous counting and readout possible, providing dead-time-free operation. In this case one of the thresholds is ignored (Table I).

The pixel contains 19 configuration bits to provide a highly configurable system.

The layout of the pixel cell is shown in Fig. 5.

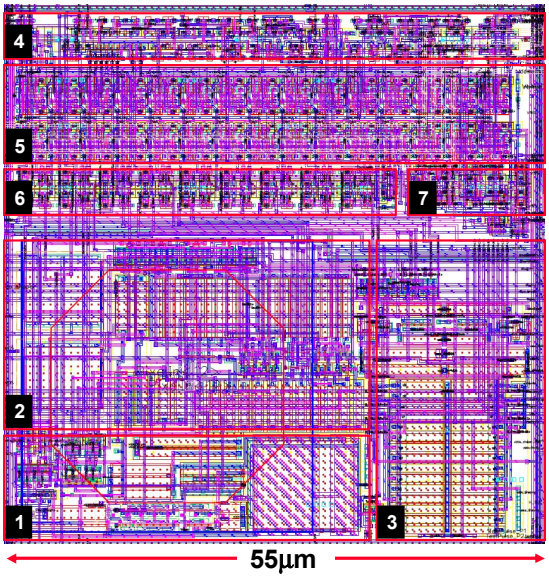

Fig. 5. Medipix3 pixel cell layout. 1. Preamplifier. 2. Shaper. 3. Two discriminators containing a 4-bit DAC each for threshold adjustment. 4. Control Logic. 5. Two 15-bit counters. 6. Nineteen configuration bits. 7. Arbitration logic for charge allocation.

IV. Measurements

Measurements have been performed using an *IMS ATS* digital IC tester [9]. Special routines have been programmed in LabVIEW in order to test the chip functionality. Two of the pixels (one in the regular matrix, the other in the test matrix) contain analog buffers which permit external monitoring of the preamplifier output, two differential nodes of the shaper and the discriminator output. Fig. 6 shows the single shot oscilloscope traces of the analog part of one pixel to an input charge of 3.7 ke$^-$.

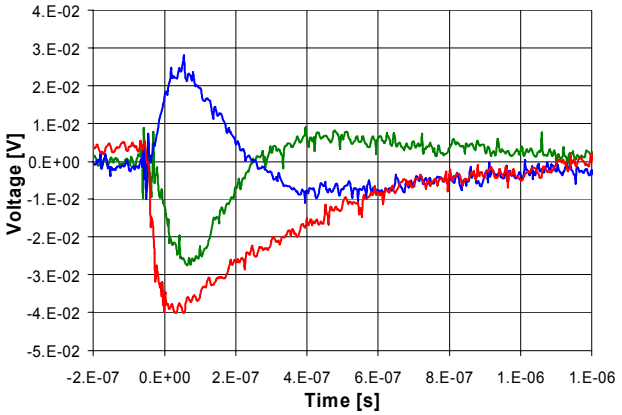

Fig. 6. Oscilloscope screen with the monitored waveforms for a 3.7ke$^-$ input charge. The preamplifier output is shown (red). Two nodes of the differential shaper are also monitored (blue and green). Operation in nominal conditions.

The noise has been measured electrically using the s-curve method. In this method a threshold scan is done through the signal passing from no counts (signal below the threshold) to 100% counts. The resulting shape is fitted with the error function providing information about the effective charge collected (mean) and the signal's noise (sigma). The measured Electronic Noise Charge is ~ 72 e$^-$ rms in *Single Pixel Mode* and ~ 140 e$^-$ rms in *Charge Summing Mode*. The same results are obtained by scanning the threshold through the noise and fitting the pedestal with a Gaussian probability distribution (no signal is injected in the preamplifier). The threshold dispersion in the matrix has also been measured. It is caused mainly by the mismatch between transistors in the shaper. The measured value for the threshold dispersion is 1875e$^-$ r.m.s. before adjustment when the system is working in *Charge Summing Mode*. A 4+1 bit DAC is implemented per summing circuit in order to correct for this dispersion. The thresholds, after applying a correction algorithm, have a uniform distribution with ~ 110e$^-$ r.m.s. When the system operates in *Single Pixel Mode* the threshold dispersion after adjustment is ~ 55e$^-$ r.m.s.

Some tests reproducing the effects of a charge shared event have been performed. Fig. 7. shows the results of a test in which a total of 4000 pulses are sent simultaneously to four pixels. The charge is correctly reconstructed and assigned to the summing circuitry (1,1). The total number of counts recorded in the nine summing circuits is also plotted. Fig. 8 shows the reproduction of a charge sharing event in which the signal is induced in two pixels. The hits are assigned to the summing circuits (1,1) and (2,1). Fig. 9 represents the worst case for this architecture where the charge is deposited completely within one pixel. In this case the charge should be assigned randomly to one of the four corners. However one observes an increase in the total number of counts at low energy thresholds. This comes from charge being injected into sensitive analog nodes as a result of arbitrator activity. Extensive simulations using parasitic components have demonstrated that the falling edges of the digital lines can inject some current into the charge summing nodes due to coupling from metal to metal parasitic capacitances. This effect is seen as double counting for the same hit and finds its worst case in the situation where the full charge is induced in a single pixel. There is also some evidence of the same phenomenon in Fig. 7. Design techniques can be applied to minimize the effect. Shielding of the analog sensitive lines and current starving techniques for the digital circuitry are possible solutions to eliminate the coupling.

TABLE II
ELECTRICAL MEASUREMENTS

Front End Operating Mode	Single Pixel Mode	Charge Summing Mode
CSA Gain (C_F)	11.4mV/Ke$^-$ (C_F=14fF)	
CSA-Shaper Gain	65nA/Ke- (High Gain Mode)	
	30nA/Ke- (Low Gain Mode)	
Non linearity	<5% 9Ke- (High Gain Mode)	
	<2% 22Ke- (Low Gain Mode)	
Peaking time	~100ns	
Return to baseline	<1µs for 4Ke- (nominal conditions)	
	<300ns (tuning R_F)	
Electronic noise	72e$^-$ r.m.s.	144e$^-$ r.m.s.
Analog power dissipation	16.2µW (nominal conditions)	

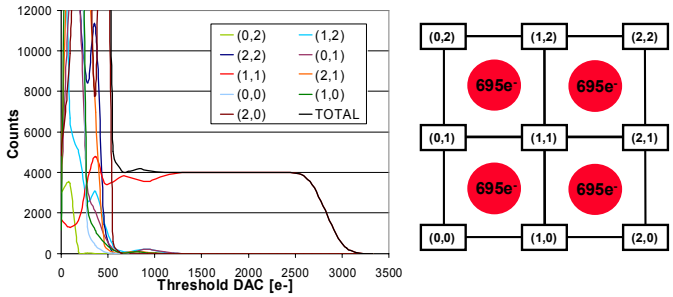

Fig. 7. Reproduction of a charge shared event by means of controlled charge injection in adjacent pixels. The sum of the hits on all counters is shown in black. The reconstructed charge is assigned to the summing circuit (1,1). The small increase in the number of total counts is an effect of the coupling from digital lines to the analog node where the charge summing is performed.

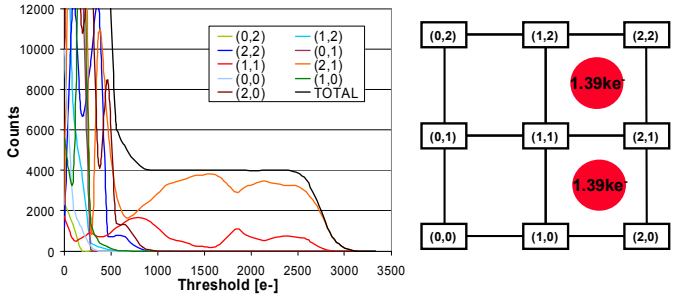

Fig. 8. Reproduction of a charge shared event. The reconstructed charge is randomly assigned to the summing circuits (1,1) and (2,1).

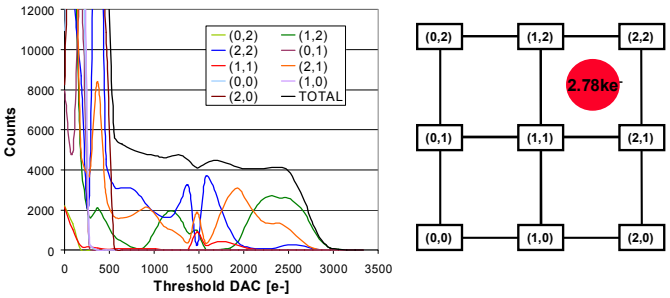

Fig. 9. The charge is fully injected in one of the pixels. This is the worst case of the arbitration circuits operation which have to randomly assign the charge to summing circuits (1,2), (2,2), (1,1) and (2,1). The coupling from the digital to the analog lines produces the shapes which represent the number of counts of each summing circuit. Layout design techniques can solve the effect of the coupling.

V. Conclusion

The Medipix3 prototype chip has been designed using a commercial 0.13µm CMOS technology. The prototype chip implements a novel architecture aimed at eliminating the spectral distortion produced by charge diffusion. Measurements show an electronic pixel noise of ~ 72 e^- rms in *Single Pixel Mode* and ~ 140 e^- rms in *Charge Summing Mode*. The threshold dispersion is ~ 55 e^- rms for the pixel operating in *Single Pixel Mode* and ~ 110 e^- rms in Charge Summing Mode.

The prototype chip has provided very useful information for the Medipix3 full imaging system.

Acknowledgment

The authors would like to thank the support and encouragement of the Medipix2 and Medipix3 collaborations.

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