The MiniSDD-Based 1-Mpixel Camera of the DSSC Project for the European XFEL

Matteo Porro, *Member, IEEE*, Ladislav Andricek, Stefan Aschauer, Andrea Castoldi, *Member, IEEE*, Mattia Donato, Jan Engelke, Florian Erdinger, Carlo Fiorini, *Senior Member, IEEE*, Peter Fischer, Heinz Graafsma, Andrea Grande, Chiara Guazzoni, *Senior Member, IEEE*, Karsten Hansen, *Senior Member, IEEE*, Steffen Hauf, Pradeep Kalavakuru, Helmut Klaer, Manfred Tangl, Andreas Kugel, *Member, IEEE*, Markus Kuster, Peter Lechner, David Lomidze, Stefano Maffessanti, Massimo Manghisoni, *Senior Member, IEEE*, Sneha Nidhi, Frank Okrent, Valerio Re, Christian Reckleben, Elisa Riceputi, Rainer Richter, Andrey Samartsev, Stephan Schlee, Jan Soldat, Lothar Strüder, Janusz Szymanski, Monica Turcato, Georg Weidenspointner, and Cornelia B. Wunderer

***Abstract*— The first DSSC 1-Mpixel camera became available at the European XFEL (EuXFEL) in the Hamburg area in February 2019. It was successfully tested, installed, and commissioned at the Spectroscopy and Coherent Scattering Instrument. DSSC is a high-speed, large-area, 2-D imaging detector system optimized for photon science applications in the energy range between 0.25 and 6 keV. The camera is based on direct conversion Si sensors and is composed of 1024 × 1024 pixels of hexagonal shape with a side length of 136 μm. The 256 application-specific integrated circuits (ASICs) provide full parallel readout, comprising analog filtering, digitization, and in-pixel data storage. In order to cope with the demanding X-ray pulse time structure of the EuXFEL, the DSSC provides a peak frame rate of 4.5 MHz. The first Mpixel camera is equipped with miniaturized silicon drift detector (MiniSDD) pixel arrays. The intrinsic response of the pixels and the linear readout limit the dynamic range but allow one to achieve noise values of about 60 electrons r.m.s. at the highest frame rate. The challenge of providing high-dynamic range (∼10^4 photons/pixel/pulse) and single-photon detection simultaneously requires a nonlinear system front end, which will be obtained with the DEPFET active pixel technology foreseen for the advanced version of the camera. This technology will provide lower noise and a nonlinear response at the sensor level. This article describes the architecture of the whole detector system together with the main experimental results achieved up to now.**

***Index Terms*— High-speed readout, miniaturized silicon drift detector (MiniSDD), Si detectors, X-ray detectors, X-ray free electron lasers.**

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Matteo Porro, Jan Engelke, Steffen Hauf, Helmut Klaer, Markus Kuster, David Lomidze, Andrey Samartsev, and Monica Turcato are with European XFEL GmbH, 22869 Schenefeld, Germany (e-mail: matteo.porro@xfel.eu).

Ladislav Andricek, Peter Lechner, and Rainer Richter are with the Semiconductor Laboratory of the Max-Planck-Society, 81739 Munich, Germany.

Stefan Aschauer and Lothar Strüder are with PNSensor GmbH, 81739 Munich, Germany.

Andrea Castoldi, Carlo Fiorini, and Chiara Guazzoni are with the Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, 20133 Milan, Italy, and also with INFN, Sezione di Milano, 20133 Milano, Italy.

Mattia Donato was with European XFEL, 22869 Schenefeld, Germany. He is now with Molecular Microscopy and Spectroscopy, Istituto Italiano di Tecnologia, 16152 Genoa, Italy.

Florian Erdinger was with the Institute for Computer Engineering (ZITI), Heidelberg University, 69120 Heidelberg, Germany. He is now with EXTOLL GmbH, 68159 Mannheim, Germany.

Peter Fischer and Andreas Kugel are with the Institute for Computer Engineering (ZITI), Heidelberg University, 69120 Heidelberg, Germany.

Heinz Graafsma, Karsten Hansen, Pradeep Kalavakuru, Stefano Maffessanti, Frank Okrent, Christian Reckleben, Janusz Szymanski, and Cornelia B. Wunderer are with Deutsches Elektronen-Synchrotron DESY, 22607 Hamburg, Germany.

Andrea Grande was with the Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, 20133 Milan, Italy, and also with INFN, Sezione di Milano, Italy. He is now with the Data Storage and Custom Power Management Division, STMicroelectronics, 20864 Agrate Brianza, Italy.

Manfred Tangl and Jan Soldat were with the Institute for Computer Engineering (ZITI), Heidelberg University, 69120 Heidelberg, Germany.

Massimo Manghisoni, Valerio Re, and Elisa Riceputi are with the Dipartimento di Ingegneria e Scienze Applicate, Università di Bergamo, I-24044 Dalmine, Italy, and also with INFN, Sezione di Pavia, I-27100 Pavia, Italy.

Sneha Nidhi, Stephan Schlee, and Georg Weidenspointner were with European XFEL, 22869 Schenefeld, Germany.

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I. Introduction

THE aim of the DEPFET Sensor with Signal Compression (DSSC) project [1], [2] is to develop large-area ultrafast X-ray camera systems for photon science applications in the energy range between 0.25 and 6 keV at the European XFEL (EuXFEL) in the Hamburg area in Germany [3]. In particular, the DSSC detectors are foreseen to operate at the soft-X-ray instruments of the EuXFEL, the small quantum system (SQS) [4], and the spectroscopy and coherent scattering (SCS) instrument [5].

The first complete 1-Mpixel DSSC camera became available in February 2019; it was fully tested, installed, and commissioned at the SCS instrument.

The camera operates with a peak frame rate of 4.5 MHz, matching the very demanding X-ray delivery time structure of the EuXFEL, as shown in Fig. 1. The free electron laser (FEL) source delivers X-rays in pulse trains with a repetition rate of 10 Hz. Every train consists of up to 2700 X-ray pulses with

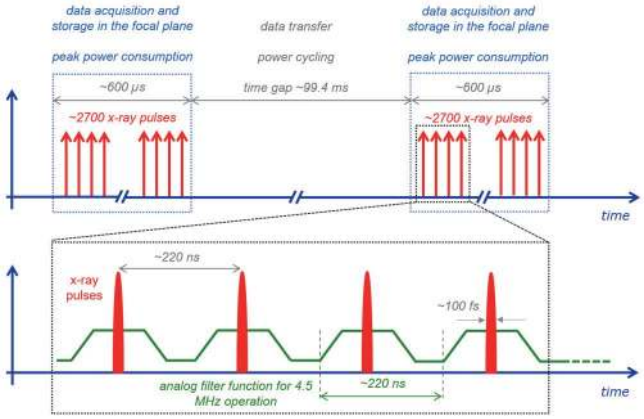

Fig. 1. Schematic representation of the EuXFEL X-ray delivery time structure. The FEL source delivers X-rays in pulse trains with a repetition rate of 10 Hz. Every pulse train consists of up to 2700 X-ray pulses with a temporal separation of 220 ns. The green trapezoidal shapes at the bottom represent the weighting function of the analog filter of the readout ASIC. For every train, 800 images can be stored in the memory of the ASICs. The data are then transferred to the EuXFEL DAQ during the ~99.4-ms time gap between two consecutive pulse trains. Major parts of the chips are powered only during the bursts.

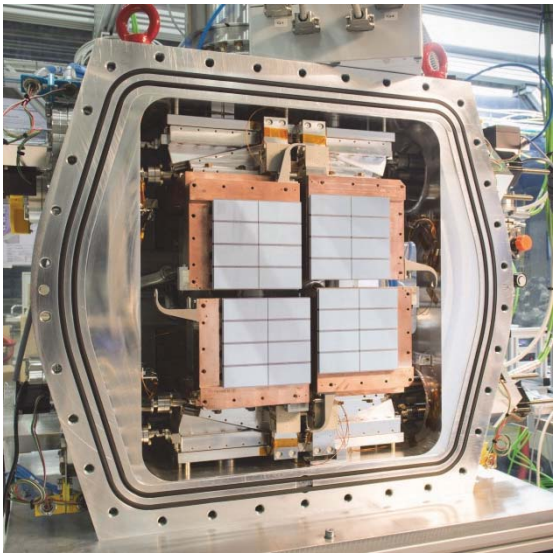

Fig. 2. Front view of the completely assembled DSSC 1-Mpixel camera during the system integration period in February 2019. The vacuum vessel with its hexagonal front flange, the mechanics and cooling system components, and the sensor plane are visible. The camera is composed of four quadrants, each comprising four ladders, each containing two monolithic MiniSDD pixel arrays. In the photograph, the quadrants are moved apart in the service position.

a temporal separation of 220 ns. The DSSC camera is able to acquire a 1-Mpixel image every 220 ns, storing 800 frames before sending out the data during the time gap between two trains. The DSSC camera system is currently the fastest 2-D imaging detector for soft X-rays.

The two other 1-Mpixel cameras specifically developed for the unique X-ray pulse structure of the EuXFEL, the adaptive gain integrating pixel detector (AGIPD) [6] and the large pixel detector (LPD) [7], target the higher photon energy range 7–15 keV. In addition, among the other differences in the readout architecture, both systems have no on-application-specific integrated circuit (ASIC) ADCs and therefore store the pixel output amplitudes as analog values, limiting the number of frames per train to 512 for LPD and to 352 for AGIPD. For the same photon energy range of the DSSC, there are 2-D detectors with uniform readout rate based both on charge coupled device (CCD) sensors, for example, the pnCDD [8], [9] and the multi-port CCD (MPCCD) [10], and on hybrid pixel sensors, for example, ePix100k [11] and Jungfrau [12]. The existing CCD-based systems can be operated with a maximum frame rate of ~100 Hz and the hybrid-pixel detectors can achieve ~1 kHz.

The DSSC detector system is based on Si sensors and is composed of 1024×1024 hexagonal pixels covering a total active area of ~505 cm^2 (Fig. 2). The pixel arrays are subdivided into 16 modules, named "ladders." Each ladder comprises two monolithic sensors with 128×256 pixels each. Four ladders form a quadrant. The quadrants are movable and arranged such that a central hole of variable size lets the un-scattered photons pass through. The maximum focal plane[1] fill-factor is 85% with the present mechanical design. Each sensor is bump-bonded to eight mixed signal readout ASICs [13]. The ASICs are designed using 130-nm IBM CMOS technology and provide full parallel readout of 64×64 sensor pixels. Each ASIC channel provides signal shaping, analog-to-digital conversion (8 bit at $f = 4.5$ MHz, 9 bit at $f \leq 2.2$ MHz), and data storage for 800 frames per X-ray train. Images stored in the memory can be overwritten in real-time when tagged as nonvalid by a signal provided by a veto source, for example, the EuXFEL machine. The camera head and the peripheral electronics [14], [15] have to cope with a total data peak transfer rate of 144 Gbit/s for the 1-Mpixel device. Table I summarizes the key properties of the system. Some of the reported parameters depend on the different operating conditions offered by the DSSC and are discussed in detail in the following sections.

This first 1-Mpixel camera uses miniaturized silicon drift detector (MiniSDD) pixel sensors coupled to a linear readout electronics front end. It provides a very low noise level of about 60 el. r.m.s. at the full speed of 4.5 mega-frames/s but a limited dynamic range due to the linear response of the readout chain.

In this article, we describe the main building blocks, the features, and the experimental results of the first complete camera system. Section II describes the properties of the MiniSDD sensor arrays. Section III is devoted to the ASIC description with special focus on the functionalities, on the different operating modes, and on the flexibility of the integrated readout electronics. In particular, the fine level of pixel-wise trimming capability, both a need and a feature of the system, has a direct impact on the overall performance. Section IV summarizes the main elements of the camera electronics that provide power regulation, control, and data transfer from the focal plane up to the EuXFEL back-end. The description of the hardware blocks

[1]We intend the detection/sensor plane of the camera. We kept the expression "focal plane" for consistency with older publications, even if DSSC is conceived for scattering experiments.

TABLE I
SUMMARY OF THE DSSC MAIN PROPERTIES

Parameter		Value
Target energy range		0.25 keV – 6 keV
Pixel count		1024 × 1024
Pixel shape		hexagonal
Sensor pixel pitch		~204 μm × 236 μm
Active area		~ 505 cm^2
Input photon range / pixel / pulse (*)	MiniSDD	$2^n \times N - 1$
	DEPFET	$>10^4$
Achievable noise	MiniSDD	~ 60 el. r.m.s.
	DEPFET	~30 el. r.m.s.
Peak frame rate		4.5 MHz
Stored frames per X-ray train		800
Average / peak data rate		134/ 144 Gbit / s
Average power consumption		~ 260 W
Operating temperature		-20° C optimum, room T possible

Performance figures refer to measurements with the MiniSDD 1-megapixel camera. In the case of DEPFET, the values represent expectations based on measurements with small format prototypes. (*) n is the number of ADC bits and N is the number of photons encoded with a single ADU. For readout frequency f≤2.2 MHz n=9, while n=8 for f >2.5 MHz. For single photon detection capability N≤1 is necessary.

ends in Section V with the mechanics. The entire Section VI is dedicated to the calibration and trimming strategy of the camera. In fact, the use of an 8-bit ADC and the need to cope with several different photon energies require pixel-wise gain and offset trimming tailored to the needs of each individual experiment. The results of a first experimental characterization of the DSSC camera installed at the beamline are summarized in Section VII.

A short outlook on the second-generation DSSC camera and other possible future developments is given in Section VIII. In the second camera, the use of nonlinear DEPFET sensors [16]–[18], instead of the MiniSDDs, will enable lower noise and higher dynamic range.

II. MINISDD SENSORS

Each detector ladder is equipped with two monolithic sensors with a size of 3 cm × 6.2 cm and a format of 128 × 256 pixels. The sensor chips are designed and fabricated at the Semiconductor Laboratory of the Max Planck Society (MPI-HLL, Munich, Germany) on 450-μm-thick, high-resistivity n-type Si wafers. The dimensions, the geometry, and the interconnection technology of the sensors are compatible with the DEPFET pixel arrays that will be used for the upgraded version of the camera.

During operation, the sensor volume is fully depleted and X-rays impinge on the backside uniform entrance window realized with an ultrathin p-n junction and covered with a thin aluminum layer of about 30 nm, used to filter optical light. The properties of the technology used to realize the entrance window have been modeled and experimentally verified [19], [20]. The model has been applied to extrapolate the quantum efficiency (QE) provided by the specific layout and layer stack of the DSSC MiniSDD arrays. The calculated QE

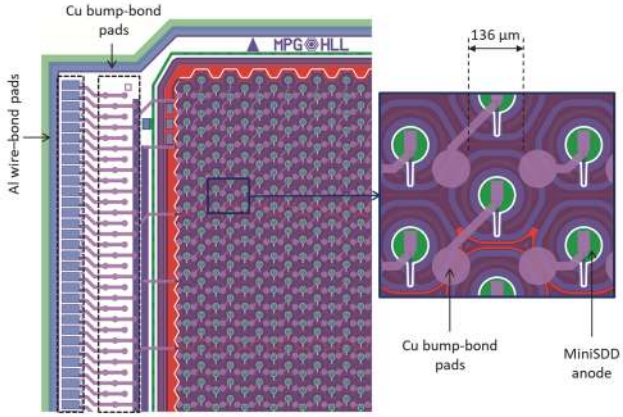

Fig. 3. Detail of the layout of the front side of one monolithic sensor. The corners are cut and shaped in order to facilitate the wire bonding of the backside contact (not visible in the photograph) to the focal plane main board. The right photograph shows a zoomed-in-view of the hexagonal pixels. The collecting anode (in green) is in the center of two drift rings, while the Cu landing pad (purple) is displaced in order to make it possible to flip the readout ASICs having a rectangular pad pitch.

is >52%, >88%, and >97% for $E = 250$ eV, $E = 500$ eV, and $E = 1$ keV, respectively.

The pixel structure is realized on the front-side of the sensor chip. Each pixel is a MiniSDD of hexagonal shape with two drift rings and a conventional collecting anode in the center, as shown in Fig. 3.

Due to the requirement of fast signal charge collection, the pixel has in good approximation the shape of a regular hexagon with a side length of 136 μm. Compared to a square pixel of similar area, the hexagon has, on average, a shorter distance from the center to the edge, resulting in a shorter charge collection time. In addition, the hexagonal shape minimizes the fraction of split events, that is, photons absorbed close to the pixel border resulting in charge sharing between two or more neighboring pixels. The hexagonal mesh results in different pixel pitches in x- (204 μm) and y-directions (236 μm). The charge collecting anode is enclosed by two drift rings that have an increasing negative bias from the inner to the outer ring and define a funnel-like potential distribution guiding signal electrons toward the center of the pixel. The hexagonal shape of the drift rings provides a more homogeneous drift field with respect to a conventional squared pixel.

The anode of each pixel is connected through a metal via to a Cu track ending with a circular bump-pad for the flip-chip solder connection to the readout pixel.

The use of MiniSDD cells instead of simple pixelated pin diodes offers the advantage of a smaller overall output capacitance for low-noise operation and also of a reduced crosstalk among adjacent pixels due to a smaller coupling capacitance. In fact, as it can be seen from Fig. 3, the bump-pads are displaced with respect to the collecting anode and can partially overlap a neighboring pixel. The MiniSDD structure avoids the overlap of the bump pad with the anode of an adjacent pixel. The displacement of the bump pad with respect to the anode is necessary in order to make the hexagonal shape of the sensor pixels compatible with the rectangular pixels of the readout ASICs to be bump-bonded.

The 32k pixels of each individual sensor are read out in parallel by eight bump-bonded ASICs. The power, the control, and the data connections are provided by the ladder electronics to the readout ASICs through the sensor chip. For this purpose, rows of wire-bond and bump-bond pads are located at the edge of the sensor (Fig. 3). The wire-bonds connect the sensor to the focal plane main board (see Section IV-A), while the bump-bonds are used for the flipped-chip connection of the ASICs. In order to maximize the yield of the flip-chip process, redundant bump connections are used at the periphery. Some wire bonds provide the biasing voltages for the pixel drift-rings. A wire bond connection, facilitated by the cut corners of the chip, biases the backside [15].

The charge collection time within one pixel has been experimentally investigated as a function of the deposited energy and resulted below 15 ns up to 2-MeV equivalent deposited energy with a backside voltage of -120 V [21]. This is compatible with the target frame rate of 4.5 MHz.

The fabrication process achieves sensor leakage current densities of few nA/cm^2 at room temperature. These values may change during the assembly phases of the detector due to mechanical stress and annealing processes. All possible precautions have been taken during the mounting of the sensors and the final leakage current has been carefully investigated [15]. An average leakage current of about 20 nA/cm^2 at room temperature has been measured for 40 sensors after full assembly. Considering the ASIC filter function and the readout time at 4.5 MHz, this leakage current gives a noise contribution <5 el. r.m.s. at pixel level, which is completely negligible with respect to the other noise sources of the system.

III. Readout ASIC

The focal plane comprises a total of 256 readout ASICs bump-bonded to 32 monolithic sensors. Each ASIC can process the signals of 64×64 pixels in parallel and has a size of 14.9 mm $\times$ 14 mm. The chips were designed and using IBM CMOS 130-nm technology, providing C4 bumps. The ASIC pixels, which have a rectangular shape with a size of 229 μm $\times$ 204 μm, are mated to the hexagonal sensor pixels. Every readout channel contains two different front ends (one for the MiniSDD and one for the DEPFET sensors), a time-variant filter with trapezoidal weighting function, a single-slope ADC, and an SRAM with a storage capability of 800 words of 9 bits, as shown in Fig. 4. In a first chip submission, the MiniSDD or the DEPFET front end could be selected electronically, but this led to increased noise and limited some voltage ranges. The choice between front ends is now done with few hard-wired modifications in one metal layer. This means that we need two different ASIC fabrications for MiniSDD and DEPFET devices. Nevertheless, the production cost is greatly reduced because only one mask has to be replaced. Global blocks, which include a 13-bit DAC for test signal generation, a digital control block and biasing circuitry, are located at the periphery of the die. Input/output (IO) and power pads are placed on one edge of the ASIC. A detailed description of the ASIC block architecture can be found in the literature [13], [22]–[26]. Here, we summarize the main characteristics and we focus on the functionalities that determine the performance figures and the operating modes of the overall system.

The simplified schematic of a single readout channel and the full-scale chip floorplan is shown in Fig. 4.

A. Charge-Sensitive Preamplifier and Trapezoidal Filter

The signal electrons collected by the MiniSDD pixel anode are integrated on the feedback capacitor C_{CSA} of a charge-sensitive amplifier (CSA) [23]. The resulting voltage step at the output of the CSA is first converted into a current by a resistor R_{V2I} and then it is processed by a time-variant filter implementing a trapezoidal weighting function. This provides optimal noise filtering at the foreseen operating speed where the series noise component is dominant [27].

The filter is called flipped-capacitor-filter (FCF) because it is realized with a single-gated integrator stage that has the possibility to reverse (i.e., flip) its feedback capacitor [22], [24]. Fig. 4 (bottom) shows the four phases of the X-ray pulse readout cycle and the corresponding control signals for the switches of the readout channel. The switches are closed when the control signals are high. The red curves of Fig. 5 represent the filter output for two different frame rates: 4.5 and 2.25 MHz. The four phases of one readout cycle are the following.

1) *Readout Channel Reset:* The preamplifier and the filter are reset. The front end is disconnected from the filter (Sw3 is low) and the current flowing into R_{V2I} is sent to a current sink (the ideal voltage source $V_{\mathrm{REF,FILT}}$ in the schematic of Fig. 4).
2) *First Integration:* The reset switch of the CSA is opened and the filter is in the integrating configuration (Sw3 and Sw4 are high and Sw5 is low). The right terminal of R_{V2I} is connected to the virtual ground of the FCF. In this way, the filter integrates the offset/baseline current which corresponds to an empty pixel.
3) *Flat-Top:* The front end is disconnected from the filter (Sw3 is low). The X-ray pulse arrives and generates a voltage step at the output of the CSA and a current step in R_{V2I} which flows into the current sink. The filter capacitor of the filter is flipped: the terminal previously connected to the negative input of the filter amplifier is connected to the output and the terminal previously connected to the output is attached to the input (Sw4 goes low and Sw5 goes high). In this way, the polarity of the output voltage resulting from the integration of the pedestal current is inverted.
4) *Second Integration:* The front end is connected to the virtual ground input of the filter (Sw3 is high).The filter integrates the current that is now the sum of the pedestal current and the signal generated current. Since the capacitor has been flipped, the voltage at the output of the filter at the end of this second integration is the difference of the two integration phases. Due to the fact that these have equal time duration t_{filt} (Fig. 5), the contribution of the pedestal is ideally canceled.

As already mentioned, the weighting function has a trapezoidal shape in the time domain. This is very effective in

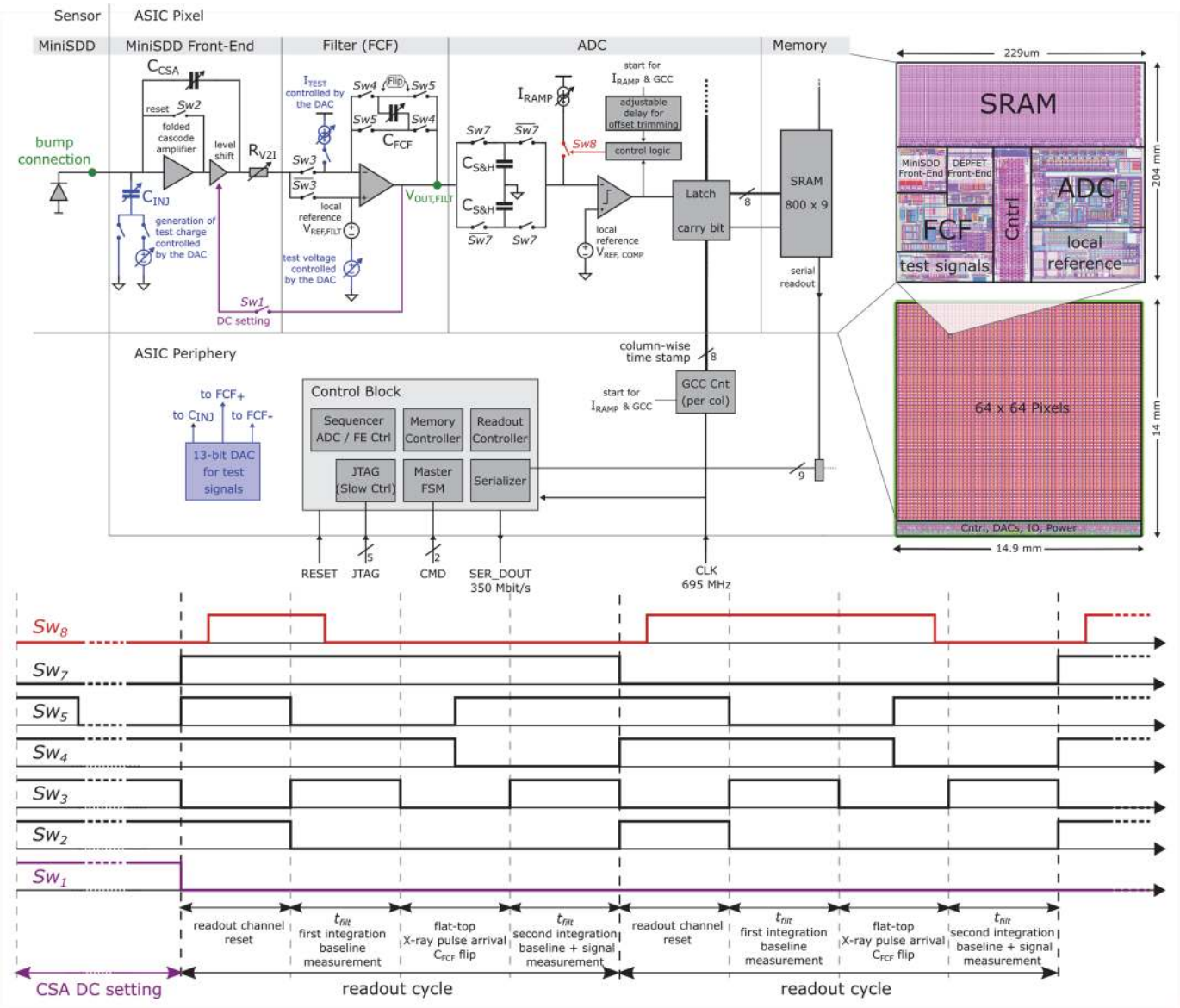

Fig. 4. Simplified schematic view of the ASIC pixel and the full-scale chip floorplan (top). The readout channel also contains a front end for the DEPFET pixel sensors, which is not shown in the schematic. The blue blocks are used for test and calibration purposes. Timing control signals for the switches of the readout channels (bottom). Two complete readout cycles are represented. The switch Sw1 for the setting of the dc output voltage of the CSA is closed only once before the beginning of an X-ray pulse train. The switch Sw8 closes (with a programmable delay) when the start signal for the GCC is given and opens soon after the comparator has triggered. Therefore, the timing of Sw8 depends on the input signal amplitude.

dumping the $1/f$ noise and is the optimal time-limited filter for the series noise. The signal-to-noise ratio (S/N) improves with the duration of the integration phases, which is limited by the arrival rate of the X-ray pulses. At the maximum foreseen frame rate of 4.5 MHz—taking into account the time needed for the reset of the electronics stages and for the flipping of the filter capacitor—the available time for each integration phase is about 50 ns. The time needed to reset the electronics stages and the flat-top of the weighting function have a similar duration. All the switches of the filter are controlled by a flexible on-chip programmable sequencer. This makes it possible to vary the duration of the current integration and flat-top phases over a wide range of values and to adapt it to the experimental frame rate. (In Fig. 5, the two integration phases are 50 ns long for 4.5-MHz operation and 160 ns for 2.25-MHz operation. The reset and the flat-top phase duration is 60 ns for both frame rates.)

The gain of the analog channel up to the filter output is

$$\text{Gain}_{\text{Analog}} = \frac{\Delta V_{\text{OUT,FILT}}}{\Delta Q_{\text{IN}}} = \frac{t_{\text{filt}}}{C_{\text{CSA}} \cdot R_{\text{V2I}} \cdot C_{\text{FCF}}} \tag{1}$$

where Q_{IN} is the charge generated by the collected photons expressed in Coulomb.

Because of the dependence on the integration time t_{filt}, in order to operate at a slower frame rate exploiting the longer available processing time and preserving the dynamic range, the other gain settings of the channel must be reduced accordingly. For this purpose, it is possible to select 15 different combinations of four feedback capacitors C_{FCF} implemented in the filter. Even for the smallest value of C_{FCF}, the KTC noise

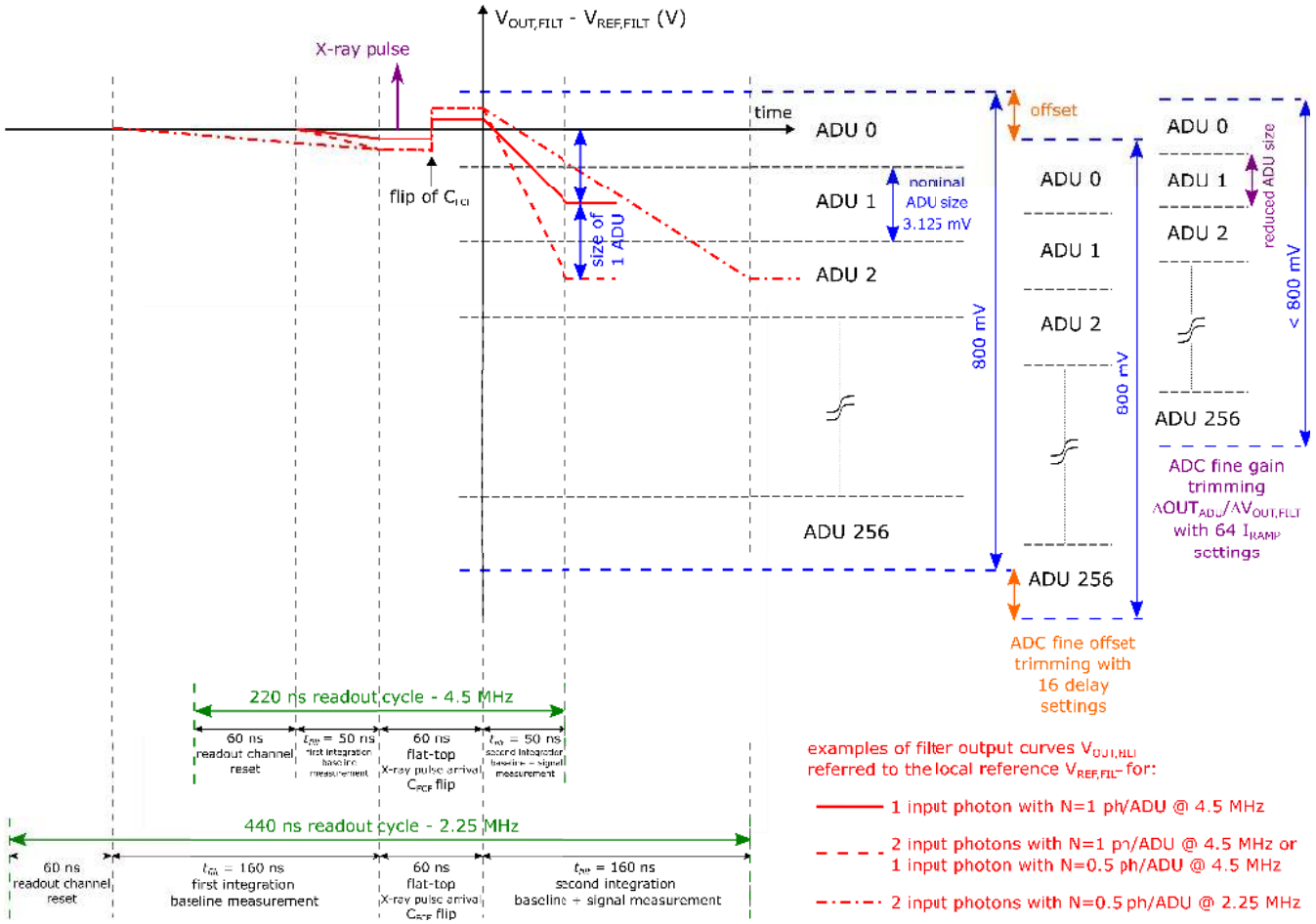

Fig. 5. Simplified timing diagram and gain setting representation for two different frame rates: 4.5 and 2.25 MHz. With 4.5-MHz operation, the red solid line represents the output of the filter $V_{OUT,FILT}$ referred to the local reference $V_{REF,FILT}$ in case the pixel has collected one photon and the gain is set such that the resulting output has an amplitude of one ADU ($N = 1$ ph/ADU). The red dashed curve can be generated by two collected photons with a setting of $N = 1$ ph/ADU or by one collected photon with $N = 0.5$ ph/ADU. The offset, adjusted by the ADC, should be such that the signal produced by one photon falls in the middle of one ADC bin (ADU 1 in the example). The red dotted-and-dashed curve can represent the output of the filter when the pixel collects one photon, the frame rate is 2.25 MHz, and $N = 0.5$ ph/ADU. The number N of photons per ADU depends on the gain of the electronics, the photon energy, and the readout speed. In general, different coarse gain settings are needed to cope with different photon energies, different frame rates, and different number of ADUs attributed to the single photons. The coarse gain settings, depending on the parameters C_{CSA}, R_{V2I}, and C_{FCF} (see Fig. 4), change the voltage-to-charge gain between the input node of the CSA and the output of the filter. In order to adjust the overall ADU-to-charge gain of the chain, a fine trim of the ADU amplitude is needed. This is obtained adjusting pixel-wise the value I_{RAMP} of the ADC.

of the filter stage has been calculated to be negligible with respect to the noise of the front end. The selectable gains are also needed to cope with different photon energies. Additional gain values are available, selecting among six combinations of four C_{CSA} capacitors and seven combinations of three R_{V2I} resistors.

The static current through the resistor R_{V2I} must be as small as possible (ideally zero) to maximize the dynamic range of the filter (static current is integrated as well as the signal current). This requires the output of the CSA (for no signal) to have the same dc level as the virtual ground input level of the FCF. For reasons of power consumption and noise performance, the CSA uses the classical architecture with a single-input transistor followed by a folded cascode. In this case, the dc voltage of the input of the CSA cannot be freely chosen and also depends on process parameter variations. A reset switch across the feedback capacitor C_{CSA} would cause a macroscopic voltage drop on R_{V2I}. In order to circumvent this problem, an adjustable level shifter is integrated into the output part of the CSA [23]. Before the arrival of an X-ray pulse train (see Fig. 4, bottom: Sw1 control signal and dc CSA setting phase), the CSA is reset, the filter—after a short reset—is switched to integration mode and its output is fed back (purple connection in the schematic) to the regulation input of the level shifter. This regulation loop stabilizes the CSA output level such that—ideally—no current flows through R_{V2I}. The control voltage of the level shifter is stored during the entire X-ray pulse train and refreshed before the arrival of the following train. The noise contribution of the level shifter is negligible. In fact, its noise sources referred to the input are divided by the gain of the folded cascode amplifier. The detailed architecture of the CSA together with the measured noise performance can be found in [23].

B. Single-Slope ADC

Between the output of the filter and the ADC, there are two identical sample-and-hold capacitors $C_{S\&H}$. While one

capacitor is charged by the filter, the ADC digitizes the voltage stored on the other capacitor during the previous readout cycle and vice versa (see Sw7 in Fig. 4).

The implemented Wilkinson-type ADC [25], [26] converts the amplitude of the voltage stored on the $C_{S\&H}$ into a timing information, thanks to an 8-bit gray code counter (GCC), located at the chip periphery. One ASIC contains 64 GCCs. Each of them serves a column of pixels. A start signal synchronous to the XFEL pulse train activates the GCC. The same start signal, with a programmable delay, is used to activate an adjustable constant current source I_{RAMP} (see Fig. 4, Sw8). This current ramps up the voltage stored on the $C_{S\&H}$ until it reaches a locally generated reference voltage $V_{REF,COMP}$. At this point, the comparator triggers and latches the value of the time stamp generated by the GCC and provided to all the pixels of the column onto differential signal lines. The comparator triggers always at the same input voltage $V_{REF,COMP}$ and therefore does not need to have a good common mode rejection.

The gray code counter architecture has been chosen because the latch signal coming from the comparator is asynchronous with respect to the counter clock. With a binary counter, possible delays on transmission lines could cause false sampling of the time stamp resulting in a large error. The GCC not only reduces the switching activity, but also minimizes the possible sampling error to one LSB. Initial counting values of the GCCs can be selected for each half ASIC. Using a clock frequency $f_{clock} = 695$ MHz and dual edge clocking for the GCC, the analog to digital unit (ADU) (or "bin") size in time is 720 ps. This is a fixed parameter of the system, while the bin size in voltage can be adjusted pixel-wise by tuning the I_{RAMP} current. The maximum input range of the ADC is $\sim$800 mV. The maximum bin size with 8 bit is then 3.125 mV. With $C_{S\&H} = 1$ pF, this corresponds to a nominal value $I_{RAMP} = 4.34\ \mu$A.

An 8-bit conversion takes 183 ns and it is compatible with the highest frame rate of 4.5 MHz, leaving some margin to count beyond 256. A logic circuit monitors the most significant bit of the GCC and sets a carry bit in the case of an overflow during a single readout cycle. This effectively provides a ninth bit. Since the bin duration is fixed to 720 ps, it is possible to fully exploit the 512 bins provided by the ninth bit only by reducing the frame rate. In fact, a full 9-bit conversion would take $\sim$370 ns, exceeding the 220 ns of separation between two pulses. Since the ADC input dynamic range is constant, in the case of 9 bits, the voltage bin size must be reduced. This is obtained by halving the I_{RAMP} using a dedicated control bit. In this article, we only consider the 8-bit case and we consider only the fine I_{RAMP} trim settings. These are obtained with six control bits, providing 64 I_{RAMP} values with a granularity of $\sim$2%.

The offset can be trimmed by adjusting the delay between the start of the GCC and the I_{RAMP} current injection on the $C_{S\&H}$ (see Figs. 4 and 5). The four offset bits per pixel allow an offset granularity of 8% ($\sim$60 ps) enabling a shift over $\sim$1.3 ADC bins.

C. Input Dynamic Range and Trimming Capabilities

In order to maximize the input photon dynamic range and have the possibility to count single photons with the limited number of available ADC bits, it is convenient to encode individual photons with single ADC bins. This means that one collected photon must produce a voltage step at the output of the filter (i.e., the input of the ADC) of the size of one ADU. This is equivalent to set the conversion factor N expressed in photons/ADU (ph/ADU) to 1. Since the system is linear, the resulting dynamic range is 255 input photons for 8-bit operation (in total, 256 values including the pedestal assigned to the ADU "zero," like in Fig. 5). The dynamic range can be increased by giving up single-photon counting and assigning more photons to a single bin, for example, $N = 2$ ph/ADU, equivalent to a dynamic range of 511 photons with 8 bits. In this case, there is an intrinsic uncertainty in the number of collected photons, because, for example, the signal produced by two photons and the signal produced by three photons (or by 100 photons and 101 photons) are encoded with the same ADU value. On the other hand, improvements in terms of noise can be achieved with N factors <1, for example, 0.5 ph/ADU, obtained by an increase of the electronics gain of the readout chain. This halves the dynamic range. In general, the maximum input dynamic range in photons can be written as follows:

$$\mathrm{Max}_{\mathrm{in_{ph}}} = 2^n \cdot N - 1 \tag{2}$$

where n is the number of ADC bits and N is the number of photons that generates a signal, which has the amplitude of one ADU. For single-photon detection capability, N must obviously be ≤ 1. This assessment assumes that the pedestal, that is, the signal for no photon at all, is set to ADC bin 0, which can be achieved by globally changing the start value of the GCC. Due to component mismatch, however, some pixels may have slightly offset pedestals.

In the case of $N = 1$ ph/ADU, the offset has to be trimmed such that the signal representing zero photons, that is, the pedestal, is allocated at the center of an ADC bin [2] and the signal generated by a single-photon falls in the consecutive bin center (red lines in Fig. 5). In this way, homogeneous flat-field images with minimal pixel-error rates [28] can be achieved. As mentioned in Section III-B, the offset can be trimmed with a precision higher than one-tenth of an ADU.

According to the experimental needs, the DSSC has to cope with different photon energies and different frame rates. A large number of pixel-wise coarse and fine gain settings make it possible to achieve the required ph/ADU conversion factor for the specific operating conditions.

The coarse settings are provided by the parameters of the analog part of the readout channel (C_{CSA}, R_{V2I}, C_{FCF}; see Fig. 4 and Section III-A). These change the voltage-to-charge $\Delta V_{OUT,FILT}/\Delta Q_{IN}$ gain[2] from the collecting anode to the output of the filter. The fine trimmings are provided by the ADC, adjusting the I_{RAMP}, that is, changing the voltage size of the ADC bins (Figs. 4 and 5 and Section III-B). This trims

[2]For the sake of simplicity, we call "gain" all the ratios between output and input system variables, even if not dimensionless.

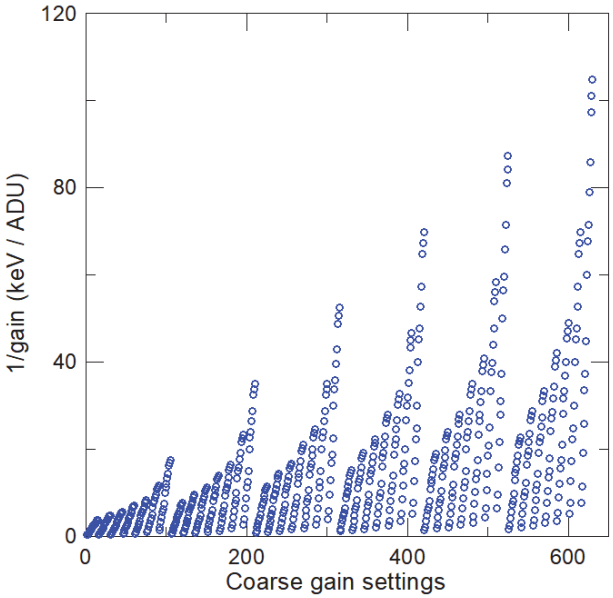

Fig. 6. Complete set of nominal coarse gain values obtained for all the possible combinations of C_{CSA}, R_{V2I}, and C_{FCF}. The integration time of the filter t_{filt} is set to 50 ns, suitable for 4.5-MHz operation.

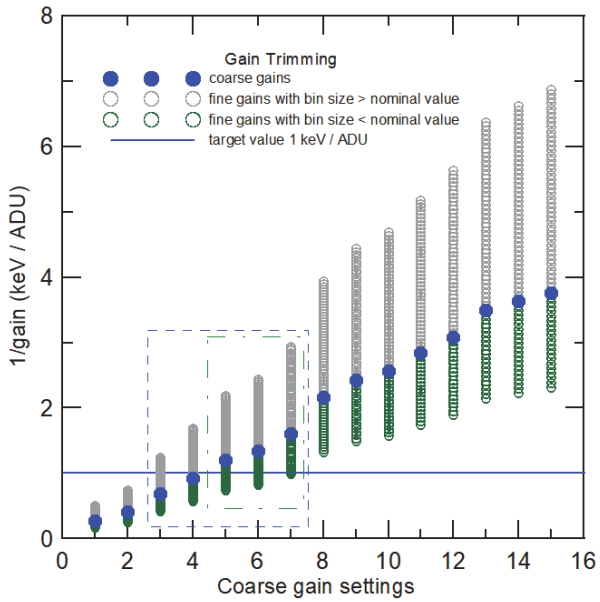

Fig. 7. Subset of coarse gain settings (blue dots) for $C_{CSA} = 60$ fF and $R_{V2I} = 3.2$ kΩ, that is, coarse gain settings obtained varying C_{FCF}. For each coarse gain setting, there are 64 fine gain values (green and gray circles). The fine gains associated with different coarse settings are overlapping. The entire energy range is continuously covered with a granularity <1%. This is true also for the other coarse settings of Fig. 6 not shown here.

the ADU-to-voltage $\Delta OUT_{ADU}/\Delta V_{OUT,FILT}$ gain. The overall gain of the chain can be written as follows:

$$\text{Gain}_{Ch} = \frac{\Delta \text{OUT}_{ADU}}{\Delta Q_{IN}} = \frac{t_{filt} \cdot C_{S\&H} \cdot 2 \cdot f_{clock}}{C_{CSA} \cdot R_{V2I} \cdot C_{FCF} \cdot I_{RAMP}}. \quad (3)$$

In (3), OUT_{ADU} is the output of the ADC expressed in ADUs. In order to better display the photon energy range and the input dynamic range, it is more convenient to use the inverse gain, typically expressed in eV/ADU.

Fig. 6 shows all the nominal inverse coarse gain settings for a filter integration time $t_{filt} = 50$ ns (4.5-MHz frame rate) and $f_{clock} = 695$ MHz. Even if the main photon energy range of interest is limited to ~6 keV, high inverse gain values can be used to set $N > 1$, achieving a high input dynamic range and sacrificing single-photon detection. For example, an inverse gain of 30 keV/ADU with a photon energy of 6 keV would result into $N = 5$ and into a corresponding input dynamic range of ~1279 photons.

The 64 fine inverse gain values (green and gray circles) associated with each individual coarse setting (blue dots) are displayed in Fig. 7. The fine gain settings have two purposes. In the first place, they allow for a precise compensation of the gain dispersion across the pixels of the ASIC with respect to the nominal value. The measured gain of each individual pixel can be trimmed in order to be as close as possible to the required target gain. The arbitrary choice of the inverse target gain keV/ADU is the second feature offered by the fine gain adjustment capability. As shown in Fig. 7, the fine gain values belonging to different coarse settings overlap (this is true also for the other settings shown in Fig. 6 and not displayed in Fig. 7) and cover the complete energy range of interest. The mean granularity of the fine inverse gain values associated with a single coarse setting is ~2%. Subpercent values of the overall granularity can be achieved considering all the fine settings belonging to different coarse values. As an example, a target inverse gain of 1 keV/ADU is indicated in Fig. 7. The closest value (<1%) must be searched among the fine inverse gains of the coarse settings in the dashed blue rectangle. Actually, it is convenient to consider only the fine inverse gains within the dotted-and-dashed green rectangle. In fact, the values represented by gray circles would require an ADU size in voltage larger than the nominal value of 3.125 mV. Therefore, 256 ADUs would exceed the physical input range of the ADC (~800 mV) and part of the dynamic range would be lost. These settings are anyway useful in reality to compensate possible deviations of I_{RAMP} from the design value.

Since the coarse gain settings are also pixel-wise, it is possible to configure different regions of the detector with different gains and different N factors. This feature can be used to choose a lower gain (higher N and therefore higher dynamic range) where a higher intensity is expected and a higher gain where a lower intensity is anticipated during an experiment. In some experiments, for example, using a solid-state sample which is not damaged by the X-ray pulses, a few probing frames could be used to determine the spatial photon intensity distribution. With this preliminary information, it is possible to generate an *ad hoc* gain map for the detector to use with the specific target, thus maximizing the resolution and dynamic range.

D. Memory, VETO Management, and Data Transfer

The output of the ADC is stored in an SRAM implemented in each pixel. While the core cell is based on a dense SRAM implementation available in the used CMOS process,

the periphery blocks have been custom-designed to optimize area occupancy, sacrificing speed performance which is not required in our application. The memory layout spans the complete width of the pixel, allowing sharing control lines between adjacent pixels. The memory of each pixel can store 800 words of 9 bits, that is, 800 frames per train of X-ray pulses. The ADC data is written to the memory in parallel and a serial readout scheme based on shift registers has been implemented to save area. Conveniently slow (<10 MHz) serial bit streams transport the data to the bottom of the columns, where it is shifted in parallel toward the output serializer. Data are sent off the chip through a serial link running at 350 Mbit/s, making use of almost the whole time gap (∼99.4 ms) between two consecutive XFEL pulse trains to send out all data. If the FEL is operated at a pulse repetition rate below 1.3 MHz, that is, pulse trains are populated with less than 800 X-ray pulses, all events of one train can be stored in the memory. For faster operating speeds, nonvalid events can be vetoed and discarded on the fly. This mechanism is implemented in the global control block in the periphery of the chip. For example, if the X-ray pulse number j of one train does not produce useful information, the global SRAM controller should receive a veto signal, at the time of the event $j + \text{lat}$, where lat is a programmable latency expressed in a number of events, provided by the EuXFEL Clock&Control System (C&C) [29]–[31]. In this case, the event number $j+\text{lat}$ can be written into the memory cell number j, replacing the noninteresting information produced by the discarded event j. The latency lat has a maximum value of 128, which represents the maximum time (in events) available to realize that an event has to be discarded. The veto logic is able to reuse discarded cells multiple times to provide a maximum of storage capacity. The last lat pulses of an X-ray train can obviously not be discarded and overwritten. If vetoes occur, the content of the memory at the end of the train of X-ray flashes is not ordered any more according to the event arrival time. There is no logic within the ASIC to reorder the memory content. This is, therefore, done during readout by the field-programmable gate array (FPGA) on the patch panel transceiver (PPT), which also manages and keeps track of the veto signals coming from the EuXFEL C&C (see Section IV-D).

E. Test and Calibration Signal Generation

It is possible to inject test signals at different stages of the readout chain of each individual pixel. In general, the amplitude of the injected signals can be set using a global 13-bit current mode DAC. Each pixel contains the circuitry needed to route the DAC output to the desired node of the readout channel and to convert it into the suitable electric signal, that is, charge, current, or voltage (see blue blocks in Fig. 4). The measured integral nonlinearity (INL) of the DAC is 0.5 LSB over 13 bits and is therefore negligible [32].

If we want to test the complete readout channel, we have to inject a charge into the input node of the CSA. In this case, the DAC current output is converted by a resistor into a voltage which is sampled on a set of capacitors C_{INJ} located in each pixel, as shown in Fig. 4. One terminal of C_{INJ} is connected to the DAC resistor, while the other terminal is connected to the virtual ground of the CSA. The terminal connected to the DAC resistor can be commuted to a dedicated ground line, discharging the capacitor and injecting the previously stored charge into the feedback capacitor of the CSA. The value of C_{INJ} can be adjusted, choosing different combinations of five capacitors (4×10 fF$+1\times 200$ fF) implemented in parallel. The smallest charge which can be injected is 6 el., allowing one to scan the ADC bins with very small steps. A maximum charge corresponding to $\sim 1.1 \times 10^6$ el. (∼4000 photons of 1 keV) can be injected to probe the full dynamic range. The charge injection mechanism is fundamental for the system calibration and trimming. As explained in Section VI, the dispersion of the C_{INJ} values over the pixels of the chip and the dispersion of DAC properties on different ASICs requires the calibration of the injected charge using X-rays.

The current output of the DAC can also be injected into the FCF through a set of current mirrors.

The gain and offset trimming capability can be tested applying a variable voltage test signal at the input of the ADC. In this case, the DAC current is converted into a voltage by a resistor. This voltage is applied to the positive input node of the FCF filter which is kept in buffer mode configuration, shorting its feedback capacitor. In this way, the FCF buffers the test voltage generated by the DAC to the input of the ADC. The minimum voltage step provided by the DAC in this configuration and the conversion resistor is only 100 μV, to be compared with the ADC nominal voltage bin size of 3.125 mV.

IV. Focal Plane Electronics and First-Level DAQ

The simplified block diagram of a complete DSSC quadrant is shown in Fig. 8. Each quadrant comprises four ladders and the focal plane electronics for 512×512 pixels.

Fig. 9 shows the photograph of one detector ladder. It consists of a focal plane module, four regulator boards, a single input–output board (IOB), a flex cable, and a module interconnection board. The latter collects all the signal, control, and power lines and sends them through a flex cable to a patch panel (PP) located outside vacuum on the other side of the back flange of the DSSC vessel.

A. Focal Plane Module

The main components of the focal plane module are two monolithic MiniSDD sensors, 16 readout ASICs, a molybdenum frame, a silicon heat-spreader and a low-temperature cofired ceramics (LTCC) main board. The readout ASICs are bump-bonded to the sensors by the commercially available IBM bumping process C4 providing bumps with a ∼100-μm diameter. All the ASICs are tested at wafer-level on a probe station with a suitable needle probe-card. This makes sure that only known good dies are bump-bonded to the sensors. The flip-chip bonding as well as the module mounting is done on a conventional flip-chip bonder adapted to the special requirements due to the highly sensitive entrance window of the back side of the sensors [15].

The sensors are connected to the main board, thanks to 1600 wire bonds at the pitch of 150 μm. In this way, all the

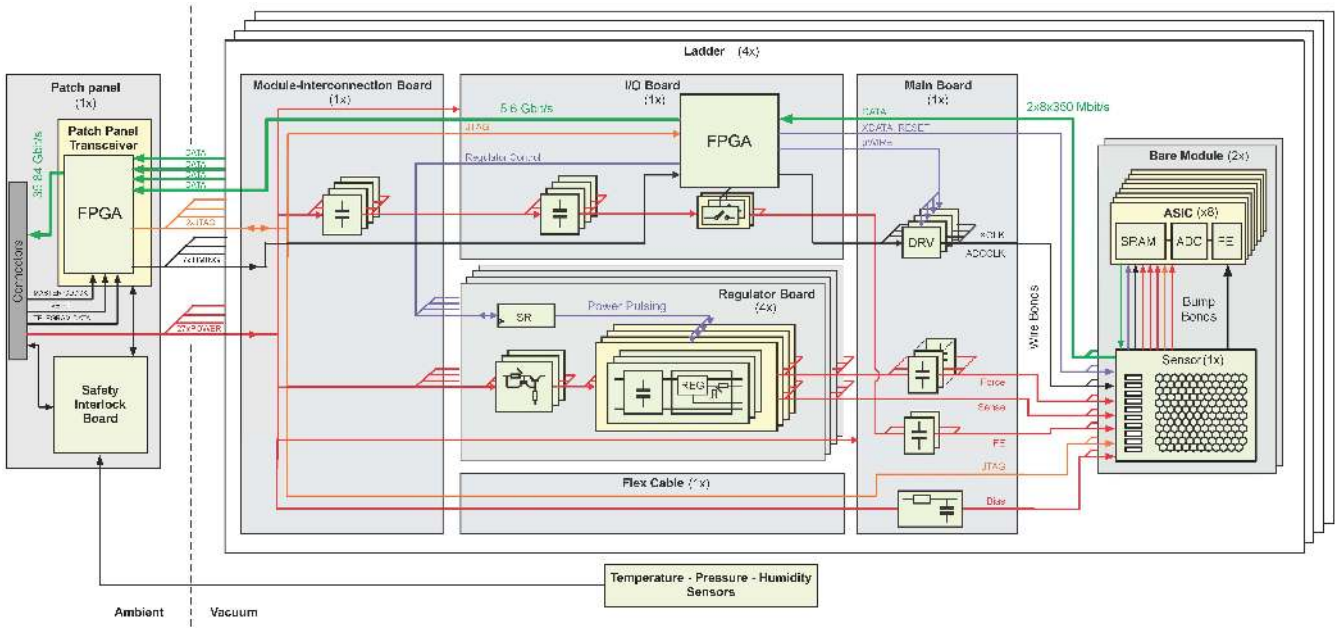

Fig. 8. Simplified block diagram of one DSSC camera quadrant. The green bold lines show the data path from the ASICs up to the EuXFEL DAQ back end. The total data rate delivered by all four quadrants is ∼144 Gbit/s. Functional blocks required for the DEPFET operation are already implemented in the ASIC and tested, but are not shown in this diagram.

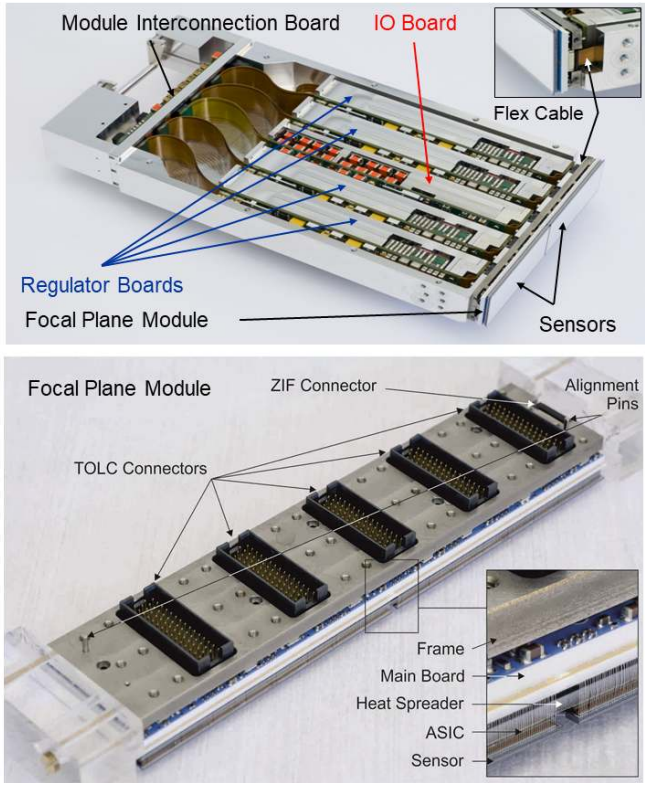

Fig. 9. Photograph of one complete detector ladder (top). Focal plane module with an enlargement of the layer stack (bottom).

power and signal lines go to the ASICs through the MiniSDD sensor chips. The ASICs are separated from the main board by a silicon heat spreader. The task of the main board is the routing of the power and of the signals. It is divided into 16 sections corresponding to the 16 ASICs. Bypass capacitors are assembled for the three supply voltages of each ASIC that are generated by the regulator boards.

The top side of the main board is equipped with low-pass filters for the supply voltages of the sensors, which are provided via the flex cable (Figs. 8 and 9).

Among the control and signal lines coming from the IOB for the ASICs, two fast clock signals are regenerated by four clock drivers placed on the main board and programed via a digital control bus. The four regulator boards and the IOBs are coupled with the main board with five 60-pin connectors. A single 24-pin connector is used for the flex cable.

B. Regulator Boards and Power Consumption

The regulator boards provide the power supply regulation for the readout ASICs. In order to minimize the power consumption, the majority of the ASIC blocks are active only during the X-ray train periods, with a power switching duty cycle of ∼1:166. This means that most stages of the ASICs are switched OFF during readout, that is, during the 99.4-ms intertrain gap of the EuXFEL machine (see Fig. 1), while only the circuitry related to data transfer is enabled. The power supply is provided to the ASICs through a set of voltage regulators with large capacitor banks. The capacitor banks are permanently charged by external power supplies. Current limiters in the charging chains ensure that the charging current does not exceed a certain value. The regulators are able to provide a constant voltage output of 1.3 V at a current request of about 3 A, which is required by the readout ASICs, for the whole 600-μs duration of the X-ray pulse train. The switching of the ASIC-supply voltages is driven by shift registers which are controlled by the FPGA of the IOB via connection though the module interconnection board.

TABLE II
MEASURED POWER CONSUMPTION OF THE DSSC CAMERA, OPERATED WITH POWER CYCLING

			Power (W)
Inside vacuum vessel	Input/Output Boards		49.45
	Regulator Boards		36.66
	Focal Plane Modules	Main Boards	40.31
		ASICs	20.25
		Sensors	2.35
Outside vacuum	Patch Panel		10.36
	Patch Panel Transceiver		97.82
	Safety Interlock Board		5.47
	Total		262.67

Table II shows the measured power consumption of the whole camera operated with power cycling. The total power dissipation is ∼263 W, that is, ∼250 μW per pixel. The coolant load in vacuum is ∼149 W.

C. Input–Output Board

Besides generating the timing signals for the regulator boards, the IOB accomplishes several tasks [14], [33]. The central element of this board is a Xilinx Spartan-6 FPGA device. The main task is to collect the data coming from the 16 readout ASICs of one ladder module and to concentrate them into three serial high-speed data streams, which are then passed to a second level of the DAQ outside vacuum. The FPGA on the IOB is programmed through a second Joint Test Action Group (JTAG) chain. Seven bunch-synchronous timing signals are brought to the FPGA to generate the above-mentioned control signals for the ASICs and the clock drivers.

D. Patch Panel

The data streams coming from the IOBs are brought via the module-interconnection board (Fig. 8) and a second flex cable to a PP outside of the vacuum vessel. All devices up to the flex cables are operated inside the vacuum housing of the detector. The PP carries a PPT on its backside [33] and interfaces to the EuXFEL experiment control system Karabo [34]. One PP with one PPT can support up to a whole quadrant consisting of four ladders.

The PPT has to provide readout and intelligent control of the DSSC detector. The overall functionality can be divided into three areas.

1) *Data Path*: The serial data from the four IOBs is merged into four 10-Gbit/s links, involving merging, multiplexing, buffering, and reformatting. In the case of vetoed frames, the PPT reorders the images stored in the memory of the ASICs and sends them out in chronological order.
2) *Timing and Fast Control:* local clock signals, for example, the ADC clock for the ASICs, are generated from the ∼99-MHz master clock distributed by the EuXFEL C&C. Thanks to an adjustable phase-locked loop (PLL), other reference clocks can be used, in case the camera is operated at another facility or in case of a machine upgrade. The control telegrams from the EuXFEL C&C are decoded, translated, and forwarded to the front-end components.
3) *Slow Control:* This includes download of configuration data to the IOBs and ASICs, initiation and execution of startup and shutdown, and monitoring and calibration sequences. For laboratory testing, standalone DAQ functionality is implemented via the Ethernet control network.

On the backside of the PP, a safety interlock board (SIB) is installed [35]. The SIB monitors the power channels and protects the quadrant by identifying anomalies and potentially hazardous operating conditions of the detector, like overheating of detector components and vacuum failures. A shutdown sequence is initiated by the SIB in the case of a critical failure of one component or if a parameter deviates from its safe operating values.

E. Data Path and Data Rate

The bold green lines in Fig. 8 show the data path across the complete readout chain. During the signal acquisition, that is, during the ∼600-μs duration of the X-ray pulse train, the output of the ADCs is stored in the on-chip SRAM which comprises 800 words of 9 bit. The complete memory content is transferred during the time gap between two X-ray trains. The data transfer rate is independent of the data acquisition rate. All the ASICs send out the data simultaneously through serial links that run at 350 Mbit/s. The serializer of the ASIC adds a tenth checksum bit to each word. Therefore, the time needed to transfer the complete memory content is 800 words × 10 bits × 4096 pixels/350 Mbit/s = 93.6 ms, which leaves some margin with respect the time gap of 99.6 ms. An individual IOB receives in parallel the data coming from the 16 ASICs of one ladder and packs them into three of the four available lanes of the Xilinx Aurora interface of the FPGA that sends the information to the PP outside vacuum. The maximum data rate of one lane of the Aurora interface is 2.5 Gbit/s, which is sufficient to cope with the minimum requirement of ∼5.6 Gbit/s (16 ASICs × 350 Mbit/s) distributed on three lanes.

Each PPT processes the output of four IOBs independently. In order to fit the data format specification of EuXFEL, the 10-bit data words are extended to 16 bit by padding with zeros. The transformation of the data words to 16-bit standard format increases data rate from 22.4 Gbit/s (5.6 Gbit/s × 4) at the input of the PPT to 35.84 Gbit/s at its output. The data are sent to the EuXFEL DAQ via four 10 Gbit Ethernet links concentrated in one 40-Gbit/s quad small form-factor pluggable (QSFP) + optical transceiver. The total peak data rate delivered by the four quadrants, considering also a small overhead of the transmission protocol, is ∼144 Gbit/s. Since almost the complete time gap is used for the data transfer, the peak rate is very close to the mean rate of 134 Gbit/s.

V. MECHANICS

The mechanics/thermal design of the DSSC system was driven by a combination of guidelines and constraints: The

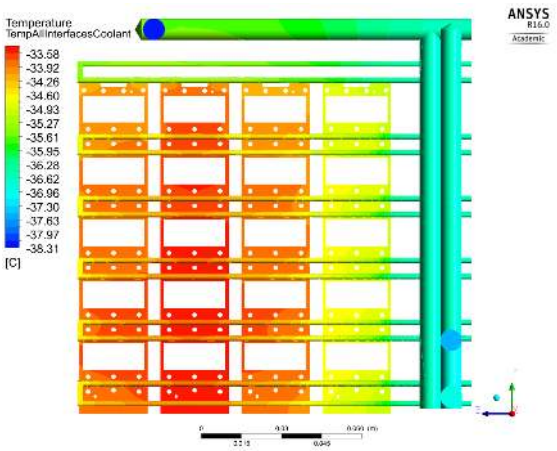

Fig. 10. Thermal situation at coolant path (horizontal lines) and interfaces of Cu cooling blocks to the module frames, based on hydrodynamic flow simulations of silicone oil coolant.

sensors have to operate at −20 °C, with a temperature spread over the full sensor array of no more than 5 °C and at a heat load (as per design estimates, actual load today is lower) of 108 W/quadrant, corresponding to 430 W/1 Mpixel. Each of the four sensor quadrants have to be movable in order to accommodate a variable-size central hole—allowing the un-scattered FEL beam to pass through under varying experimental conditions while maximizing detectable q-space. Position accuracy and—even more importantly—stability, the latter to fractions of one pixel, that is, tens of micrometers, added to the challenge. The minimum and maximum diameter of the central hole, defined as the cylinder that could be inserted between corners of the four quadrants, is ∼4 and ∼30 mm, respectively.

The cooling system uses silicone oil as coolant, requiring turbulent flow of a viscous fluid for good heat exchange. Extensive simulations (see Fig. 10) guided the design of a Cu cooling block with meandering coolant flow paths inserted immediately below the sensor module assembly attachment points. The fabrication of these blocks required an intricate combination of precision-milling and Galvano forming. The coolant is brought to the cooling blocks through double-walled flexible coolant pipes, enabling a protective vacuum in case a leak develops in the flexible coolant pipe bellows.

Thermal simulations supported the choice of materials used in the module assemblies, including printed circuit board (PCB) material, heat spreader architecture, interface frame material, and choice of adhesives—aiming to minimize mechanical stress from thermal cycles as well as good temperature uniformity in the sensor plane.

The design of the x-/y-motion system was copied from the AGIPD detector [6]—requirements were almost identical, and reuse of the same system simplifies commissioning and operation—as well as spare part philosophy—at EuXFEL.

The vacuum chamber is milled from a single aluminum (primarily motivated by weight considerations) solid block (to avoid stresses and the possibility of inaccuracies from welding), with weld-attached bimetal flanges for ease of use and durability. The vacuum level reached in the chamber with the full detector during normal operating conditions (detector cooled at −20 °C) is at the low 10^{-7} mbar level.

VI. System Calibration and Trimming

The aim of the calibration is the determination with the adequate precision of the relationship between the digital output of the readout chain expressed in ADUs and the charge, or the number of photons of a defined energy, collected by individual pixels. This corresponds to measure the gain of each of the 1-million pixels of the camera. In the case of DSSC, the mere experimental determination of the gain is not sufficient to fully exploit the features of the camera, without losing dynamic range or resolution. This is due to the limited number of bits of the ADC. After being measured, the gain must be trimmed pixel-wise in order to match the target value required by the experiment. As explained, the digitization concept of the DSSC consists in attributing a predefined number of photons N to a single ADU. Considering the linear response of the system, N is independent of the input signal. For single-photon detection, there must be a precise correspondence between the signal produced by a single photon and an integer number of ADUs.

The configuration of the camera gain settings requires an iterative process. This consists in the experimental determination of the gain of the individual pixels in a starting configuration—which can be strictly considered calibration—and the trimming of the fine gain setting in order to achieve the optimal target configuration for the requirements of a specific experiment.

The complete calibration and trimming procedure can be summarized as follows:

1) definition of a target gain suitable for the experiment;
2) identification of the nominal coarse gain settings closest to the target gain;
3) experimental search, for every individual pixel, of the fine gain setting that minimizes the difference between the target gain and the measured gain of the pixel.

Step 3 requires the iterative independent measurement and adjustment of the gain of all the individual detector pixels. The procedure is based on the acquisition of spectra of a hard X-ray line (e.g., Cu Kα or higher) with DSSC at a high-gain configuration to optimize peak-fitting precision. In fact, the limited ADC resolution combined with its nonnegligible differential nonlinearity (∼30%) restrict in practice gain determination with X-rays to few high-gain values. The gain is given by the distance of the centroids of pedestal peak and X-ray line. The charge injection circuit described in Section III-E is then required to measure all the other lower-gain values. An increasing amount of charge is injected by the circuit into the input node of the pixel readout channels ("charge injection sweep" procedure) at one of the same gain settings used for the X-ray spectra acquisition. The gain evaluated from the slope $\Delta \mathrm{OUT}_{\mathrm{ADU}}/\Delta Q_{\mathrm{INJ}}$ of the linear fit of the digital output values as a function of the injected charge is compared with the absolute gain values extracted by the X-ray spectra. This allows for the precise determination of the injected charge Q_{INJ}, that is, it provides the calibration of the injection circuit. This is necessary because of the (ASIC-to-ASIC) dispersion

of the average gain of the global 13-bit DAC (measured ∼5%) and the (pixel-to-pixel) dispersion of the injection capacitors values C_{INJ} (measured ∼1%). An automated gain trimming routine makes use of the calibrated injection circuit to iteratively measure and fine trim the gain of each pixel toward the desired target value.

A second option is to measure *a priori* the gain values of all the combinations of coarse and fine settings and produce a lookup table (LUT). The gain settings of each pixel required to set the desired target gain value are then easily searched in the LUT.

The validation of the complete gain calibration and trimming procedures has been conducted first on a single-ladder setup (128 × 512 pixels) [36]. X-ray fluorescence spectra were collected at PETRA III, beamline P64. Fitting tools specifically developed for DSSC that includes the impact of the plateau between pedestal and X-ray lines on peak centroid determination, allowed the analysis of the X-ray fluorescence spectra coping with the peculiarity of 8-bit digitization [37]. Each X-ray line is modeled by a Gaussian peak and its low-energy plateau (called "trough" in [37]) by means of two specific terms (shelf and exponential tail). The final implemented code features a custom-fit function for fluorescence spectra—able to model the photo-peaks shape and their low-energy shoulder—with a balanced number of free parameters in order to optimize precision and robustness for automated fitting at ladder level (65 536 pixels). The experimental setup with the X-ray beam at 90° with respect to the detector focal plane minimized the Compton scattering in the detector. The high-energy primary beam available at P64 beam line allowed use of Cu and Ag-pure samples (Cu Kα 8.048 keV, Ag Kα_1 22.163 keV). The ASIC was set at a high-value gain configuration in order to optimize calibration accuracy. In the specific case, the gain parameters of the ASIC were set to the nominal inverse gain of 400 eV/ADU (see Fig. 11). This provides a relatively large number of ADUs between the pedestal peak and the K lines which is beneficial to minimize the impact of the differential nonlinearity of the in-pixel ADC and of the background. At a later time and under the same conditions, we acquired a charge sweep with the injection circuit and tested the automated gain trimming procedure.

In our example, gain trimming was executed setting the target inverse gain to 700 eV/ADU. After choosing the nominal coarse inverse gain closest to the target value, the automated trimming routine launches a first charge injection sweep. The measured gain of the whole readout chain is compared with the target inverse gain (700 eV/ADU) and the ADC fine gain setting is finally modified to approach the target value. Fig. 12 shows the results achieved at convergence, nicely demonstrating the spread of DSSC inverse gain across the ladder before (5.9% r.m.s.) and after trimming (0.8% r.m.s). After trimming 99% of the pixels are within 1% of the target value. This result shows the successful equalization of the inverse gain over the ladder down to the limit of the granularity of the ADC fine settings (about 2%). In this case, we used only the fine settings belonging to a single coarse value (see Section III-C).

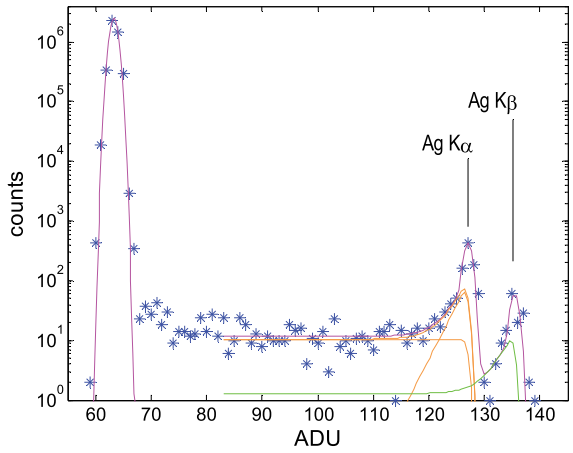

Fig. 11. Typical fluorescence spectrum of an Ag pure sample (Kα_1 22.163 keV, Kα_2 21.990 keV) on a single pixel obtained at PETRA III, P64. The global fit function of the Kα, Kβ fluorescence lines and of the pedestal peak according to the model proposed in [37] are shown in magenta. The contributions of Kα and Kβ lines (orange and green solid lines) are shown together with the two terms (shelf and exponential tail, dashed lines) modeling the low-energy shoulder of Kα line. The distance between the Kα line (weighted average) and the pedestal is 63.88 ± 0.04 ADU corresponding to a gain of 0.346 keV/ADU.

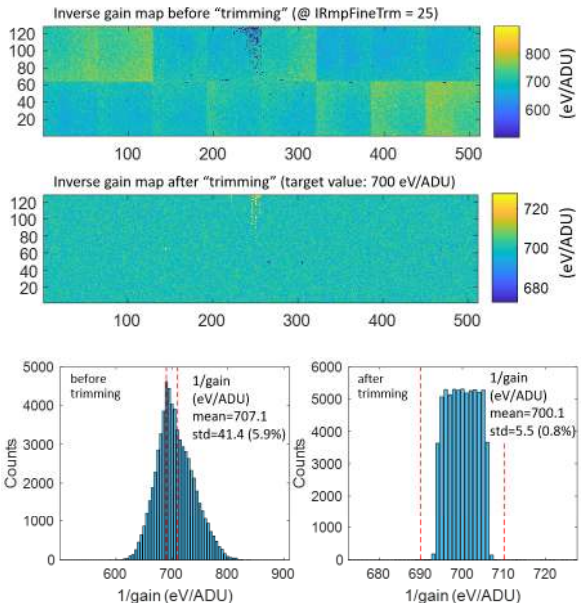

Fig. 12. Map and histogram of the inverse gain over one ladder (512 × 128 pixel) before and after gain "trimming." The starting situation is the nominal coarse setting closest to the target inverse gain (700 eV/ADU) and a nominal I_{RAMP} setting common to all the pixels. Gain data are obtained from Ag K spectra fitting. In the map and histogram after trimming, the inverse gain scale has been zoomed to appreciate the achieved uniformity. In the two histograms, the red dashed lines show the interval 690–710 eV/ADU. After trimming, 99.65% of the pixels are within ±1% of the target value (±7 eV/ADU).

A dedicated campaign for the calibration and the noise qualification of the whole MiniSDD camera was conducted at the EuXFEL detector laboratory located at the former HERA Hall South at DESY, Hamburg, Germany, in March 2019.

X-ray spectra were acquired using a pulsed X-ray source, named PulXar, based on the fast deflection of an electron beam on a metal target. This source can provide trains of X-ray pulses with duration as short as 25 ns at high burst rate (up to 4.5 MHz). The train length is limited to a few thousand pulses followed by a gap of >99 ms which mimics the time

structure of the beam at EuXFEL, clearly at lower total pulse energy. Differently from the nearly monochromatic X-ray spectra acquired at PETRA III, the X-ray spectrum produced by the PulXar source will include Bremsstrahlung having a spectral broadening related to the accelerating voltage. PulXar was operated at 20 kV with a Cu target and 4.5-MHz pulse burst rate with pulse duration matched to the $\leq$50-ns flat-top of DSSC readout. Beam filtration with an Al foil (thickness of 50 μm) was selected to achieve partial suppression of Bremsstrahlung with respect to the Cu Kα count rate. In order to have full compatibility with the operation conditions at the EuXFEL beam line, we used the timing signals from the EuXFEL C&C that were made available in the laboratory. In the experimental setup, the distance between the anode target and the DSSC camera was about 2 m in order to irradiate nearly the full quadrant through a DN160 flange. The acquisition of X-ray spectra therefore had to proceed in sequence, one quadrant at a time. Accidentally, the detector ladder #9 was not working during data taking because of unstable contact at low temperature of a board and could not acquire X-ray spectra.

The operation of this ladder could be restored only at the end of the experimental campaign, when the vacuum vessel could be opened. The spectra fitting procedure identified the pedestal and the Cu Kα line and produced calibration data. The chosen gain configuration for X-ray spectra acquisition was a relatively high value (nominal 0.4-keV/ADU inverse gain) in order to minimize binning effects due to the limited (8 bit) in-pixel ADC resolution and to optimize the peak fitting and calibration algorithms.

A global view of the results of spectra fitting of the untrimmed ladders (as mentioned above, the data of ladder #9 was missing) is given by plotting the mean value and the standard deviation of the inverse gain and noise of each ladder (see Fig. 13). The overall mean value is 382.9 eV/ADU, differing only $\sim$4% from the nominal value of 400 eV/ADU. The mean values of the inverse gain over each ladder are very close to each other, with a dispersion of only 1%. The spread of the untrimmed inverse gain within each ladder, shown in Fig. 13 (top plot) by the length of the error bars, is also very uniform for each ladder and, on average, is 4.5% of the mean value. The standard deviation of the pedestal peak (Gaussian fit) in the X-ray spectra directly provides the equivalent noise charge (ENC). The mean values of the ENC on each ladder also show a relatively uniform behavior around the average value of 57.6 el. r.m.s. The very good alignment of the results of each ladder confirms the homogeneity of the camera components and of the whole process of camera component production and integration.

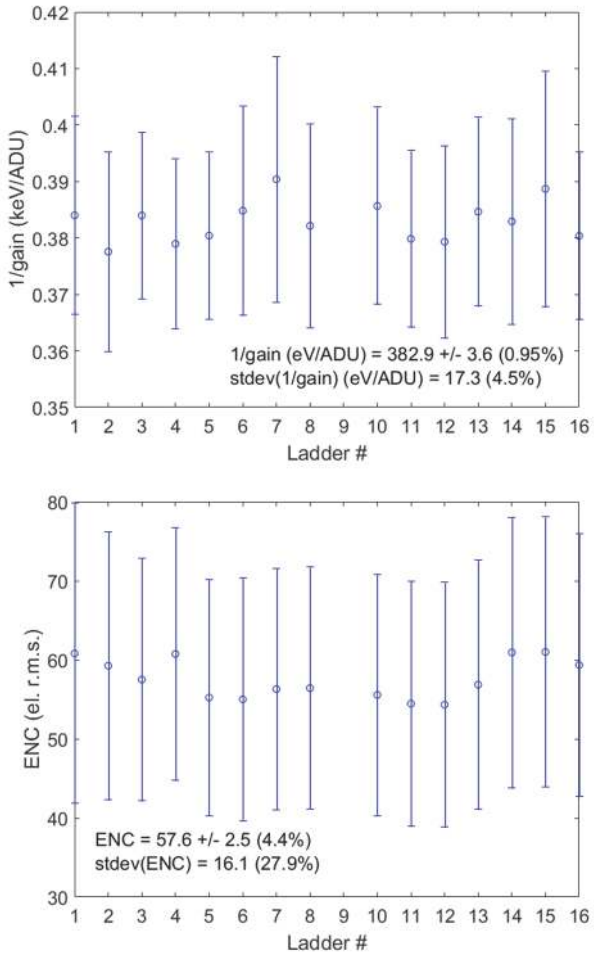

Fig. 13. Gain and noise data over the MiniSDD camera from X-ray spectra fitting. Plot of the mean (circles) and standard deviation (error bars) of the pixel gain values within each ladder (left) (top). Plot of the mean noise (ENC) within each ladder (bottom). The statistical dispersion of mean (gain) and mean (std. gain) across the 15 ladders are also given in the insets. The data of ladder #9 is missing (see text).

VII. Experimental Results With the SCS Instrument at the EuXFEL SASE III Beamline

The MiniSDD camera was successfully installed and commissioned at the SCS beam line at the end of May 2019. Fig. 14 shows a dark image of the complete camera operated at 4.5 MHz. Only three ASICs out of 256 were found to be not operational. The overall dead pixel count is $<$2%. The dark map in Fig.14 shows a mean offset (uncorrected) of 35–40 ADUs mainly caused by the ADCs. Contributions from devices connected upstream of the ADC are compensated by the FCF. The visible remaining checker-board pattern is determined by the on-chip distribution of power, ground, and reference voltages that are split into two main branches at ASIC level (left-half, right-half). Different start values of the GCCs could be set to reduce the offset in each half-ASIC. Nevertheless, the offset is not limiting the dynamic range as the ADC can count beyond the 256th ADU by setting the carry bit (see Section III-B). More details of the ADC working principle and the influence of device parameters and settings are summarized in [25].

Due to time constraints, the evaluation of the camera performance was focused on the gain configurations requested by the first user experiment scheduled to start at SCS on May 29, 2019. The EuXFEL beam was set by SCS at 1.13-MHz pulse frequency with a photon energy of 707 eV (Fe L3-edge). A representative X-ray image collected during commissioning at SCS is shown in Fig. 15. It is a single-shot diffraction image

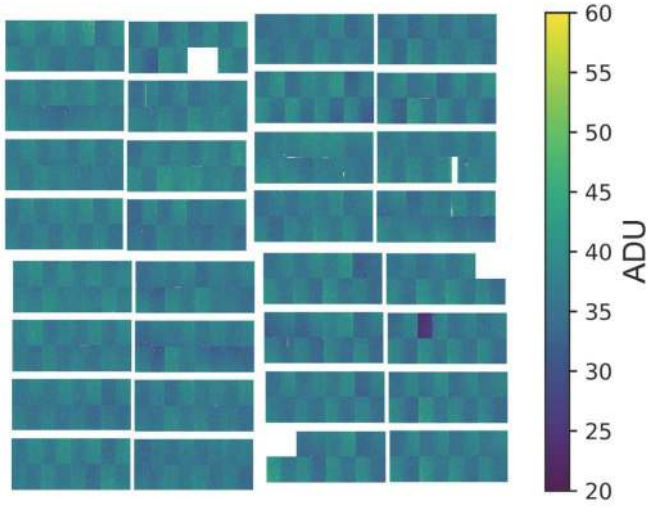

Fig. 14. Dark image of the 1-Mpixel camera installed at SCS, acquired with 4.5-MHz readout rate.

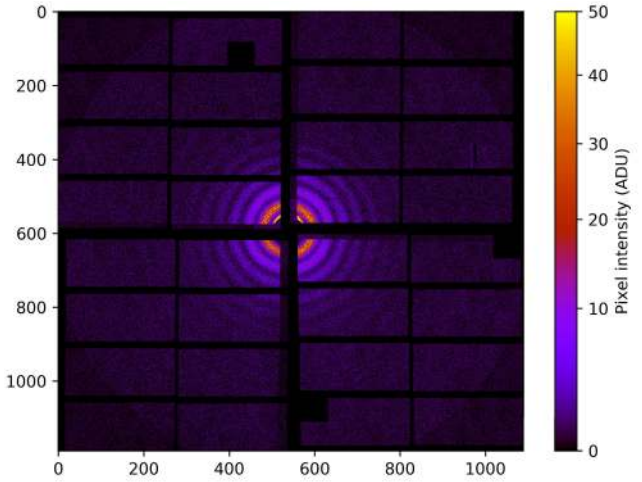

Fig. 15. Single-shot diffraction image of a pinhole mask acquired by the MiniSDD camera during commissioning at SCS beam line. The FEL delivered X-ray photons with an energy of 707 eV with a pulse repetition rate of 1.1 MHz, while the DSSC detector was operated at 4.5-MHz frame rate. The DSSC N factor is set to 0.33 ph/ADU.

of an array of pinholes with 707-eV photons, acquired by the DSSC detector operating at 4.5-MHz readout frequency and with a conversion factor N of 0.33 ph/ADU. Nonresponsive pixels are removed from the image and a gamma correction with a γ factor of 0.7 is applied. The DSSC detector therefore received one X-ray pulse every four DSSC readout cycles and a veto pattern (one every two pulses) was sent to avoid filling the 800-cell in-pixel memory with an excessive number of dark images. The camera was then considered ready for the first user experiment dedicated to X-ray holography studies. The experiment required the DSSC camera to record two X-ray images at 707-eV photon energy for different experiment conditions which are then to be compared in the data analysis. Five trimmed gain configurations, agreed with the users, were prepared for the camera: 1 ph/ADU, 2 ph/ADU, 4 ph/ADU and two higher gain modes, 0.5 ph/ADU and 0.33 ph/ADU.

The camera showed a stable operation over the whole beam time. The analysis of the dark images showed an absence of drift of the pedestal along the train number. Fitting the pedestal peak of single-pixel histograms with a Gaussian fit gave a standard deviation of 1.04 ± 0.02 ADU, equivalent to ENC $=$ 68 el. r.m.s., very close to expectations.

The analysis of single-pixel X-ray spectra showed the noise performance of the DSSC camera. In Fig. 16, the X-ray photon number distribution collected by a single pixel is shown (sum of 24 000 frames). The magenta fit line, overlaid on the histogram, is a four-Gaussian fit function with six fit variables (the four amplitudes, pedestal centroid, peak distance). The standard deviations of all four Gaussians were fixed at the value of the pedestal sigma (1.04 ADU, equivalent to ENC $=$ 68 el. r.m.s.) computed previously from dark images.

Although the Gaussian peaks are partially overlapping (at about a three sigma distance), the fitting model could discern the four individual peaks with amplitudes following a Poisson distribution ($\lambda = 0.38$, from the minimization of the sum of squared residuals). The distance between the peak centroids (xdelta) is 3.06 ± 0.2 ADU, compatible with the inverse gain calibration (0.33 ph/ADU). This spectrum nicely

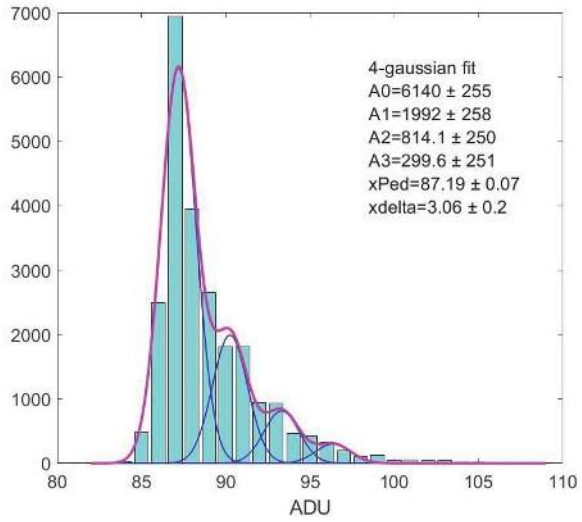

Fig. 16. X-ray photon number distribution of a central single pixel. The photon energy is 707 eV. A four-Gaussian fit is shown together with the fitting parameters (value and uncertainty). The sigma values of all the Gaussians are fixed at the values estimated from the pedestal peak in dark acquisitions. With the help of the fit curves, the pedestal and the photon multiplicity up to 3 are clearly visible.

confirms the possibility to distinguish individual photons at 707 eV with an S/N of about 3 at 4.5-MHz frame rate with the whole MiniSDD camera.

In following user experiments, gain configurations of 1, 0.5, and 0.33 ph/ADU for photon energies of 778 (Co L3-edge) [38], 1241 (Tb M-edge), and 3004 eV (Rh L3-edge) have already been employed. For all of them, the trimming precision described in Section III-C has been achieved. Fig. 17 shows the gain histogram after trimming for two of the above-mentioned gain configurations.

VIII. Outlook

A second 1-Mpixel camera is presently under construction. In this upgraded version of the camera, arrays of DEPFET active pixels will replace the MiniSDDs. The entire DSSC system is designed to be compatible with both types of

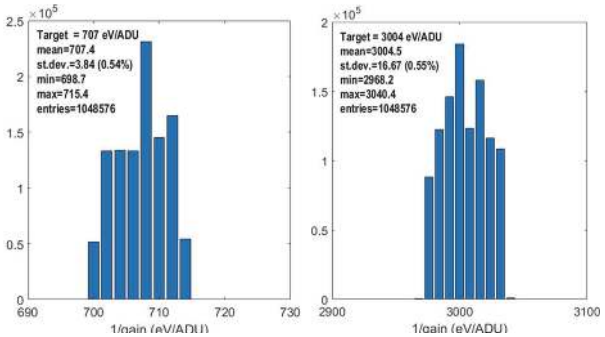

Fig. 17. Trimmed inverse gain values for the whole camera for 1 ph/ADU with $E = 707$ eV and 3004 eV.

pixelated sensors. The challenge of having high-dynamic range and single-photon detection simultaneously requires a nonlinear response of the system front end. The DEPFET pixel technology provides lower noise figures and input dynamic range compression at the sensor level, allowing the DSSC camera to reach the original design performance [1], [2]. The dynamic range per pixel can be increased to, for example, several thousand photons of 1 keV, keeping at the same time single-photon sensitivity with an $S/N > 5$.

The sensors used for the second camera are the first DEPFET devices produced with a modified commercial CMOS process [18]. A prototype ladder using large format sensors and the complete readout chain has already been assembled and is currently under test. The camera components are, to a large extent, identical to those used for the MiniSDD camera. In fact, the ASIC offers dedicated alternative front ends for the MiniSDD and the DEPFETs, while the rest of the filter processing chain and the digital blocks are common. The ladder electronics of the present camera already contains the infrastructure to provide the power regulation and the control signals for the active pixel sensors. A dedicated electronics implemented on the module interconnection boards and on the regulator boards provides fast reset pulses for the DEPFETs.

Some of the fundamental concepts of the DSSC camera can be considered a solid starting point for the development of new X-ray imagers satisfying different scientific requirements or constraints. One example could be the use with high-repetition rate X-ray FEL sources that operate in a continuous mode, like the LCLS II machine [39] in the USA or the continuous wave (CW) upgrade of the EuXFEL, which is at the moment under discussion [40]. In the continuous mode, the X-ray pulses are uniformly spaced in time and not concentrated in trains separated by macroscopic time gaps. The maximum foreseen repetition rate is 1 MHz. While this represents an increase by more than one order of magnitude with respect to the average frame rate of DSSC (27 kHz), the performance in terms of noise and—to some extent—also of dynamic range depends on the peak frame rate. This means that adapting the DSSC concept for a continuous readout mode would require a modified design concept for the cooling, the ASIC power management, and the data transfer, but should not degrade the performance figures of the detector. On the contrary, since the peak rate would be relaxed ($\leq$1 MHz versus 4.5 MHz), one can expect to achieve the same or better noise figures with the same dynamic range.

IX. Conclusion

The first 1-Mpixel camera developed in the framework of the DSSC project has been successfully completed, commissioned, and installed at the SCS instrument of the EuXFEL. The camera is optimized for soft X-rays and, since May 2019, it is regularly employed for user experiments.

The experimental results fulfill the design specifications. The system can be operated at a peak frame rate of 4.5 MHz with a mean noise of $\sim$60 el. r.m.s. The gain and offset can be trimmed pixel-wise and a gain dispersion $<$1% over the whole 1-Mpixel focal plane has been obtained. The DSSC camera digitizes and stores the pixel signals directly in the ASICs and the complete memory depth of 800 frames per X-ray train can be used. The data stored in the focal plane are transferred during the time gap of the EuXFEL machine, while the analog part of the readout electronics can be switched OFF, thus realizing the so-called power cycling. This drastically reduces the mean power consumption of the system.

In 2021, the detector will also be operated at the SQS instrument [4]. The second DSSC camera is under construction. While this system makes, to a large extent, use of the existing hardware and electronics components, the MiniSDD arrays will be substituted by matrices of nonlinear DEPFET active pixel sensors. These devices should allow one to improve the noise performance of a factor 2 and—at the same time—to increase the input dynamic range of more than one order of magnitude.

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