The Modular Multilevel Converter for High Step-Up Ratio DC-DC Conversion

Xiaotian Zhang, *Member, IEEE* and Timothy C. Green, *Senior Member, IEEE*

***Abstract*—High step-up ratio dc-dc converters with megawatt ratings are of interest in wind turbine interfaces and HVDC systems. This paper presents a modular multilevel dc-dc converter based on the standard boost converter topology but with the normal single switches replaced by a number of capacitor clamped sub-modules. The converter is operated in resonant mode with resonance between sub-module capacitors and the arm inductor. A phase-shifted switching arrangement is applied such that there is a constant number, N of sub-modules supporting the high voltage at a time. In this operation mode, the step-up ratio is dependent on the number of sub-modules and the inductor charging ratio. The converter exhibits scalability without using transformer and is capable of bidirectional power flow. An application example of a wind turbine interface with a $10:1$ conversion ratio is demonstrated in simulation. The experimental verification of the concept using a lab-scale prototype is provided.**

***Index Terms*—Modular multilevel converters, step-up dc-dc conversion, resonant conversion, HVDC converters, dc transformer.**

I. Introduction

Multilevel converters used for medium voltage and high voltage applications significantly reduce the harmonic content of the output voltage as compared to the traditional two-level converters [1]–[8]. Multilevel converter schemes for dc-dc conversion are becoming popular [9] in renewable energy applications following the success of this approach in dc-ac conversion. There are many different types of multilevel converters developed [10], [11], which can be directly or indirectly used as step-up dc-dc converters. However, none of these multilevel topologies is found to have more attractive features than the modular multilevel converter [12]. Diode clamped converters have a large number of diodes required, which will make the system impractical to implement [11]. Conventional flying capacitor converters [13] require many capacitors connected in series. The total series capacitance is much smaller than that of a single one. Therefore, the total volume of capacitors required is quite high. Generalized multilevel converters can be used for step-up dc-dc conversion [14], [15], but the topology results in a large size when the step ratio is high. Other topologies such as input-parallel-output-series (IPOS) converters [16] and switched capacitor converters have been proposed and developed for step-up dc-dc conversion [17]–[19]. The IPOS converters use resonant sub-modules to achieve high power conversion and efficiency [20], but the main disadvantage is the requirement of a large number of isolation transformers, which have high potential differences between the windings. Switched capacitor converters are widely used in low voltage applications and resonant operation can also be used to achieve high efficiency. However, the switched capacitor converters with series-parallel topologies are subject to incremental voltage stress either on the module switch or on the module capacitor. The highest voltage stress is close to the output (high-side) dc voltage. The switched capacitor converters are also subject to high charge losses and overshoot currents. This problem can be mitigated by driving MOSFETs with very high switching frequency. Therefore, switched capacitor converters are only used under low voltage condition. A power electronics based Cockcroft-Walton multiplier has been demonstrated in [21]. This is a light and cheap solution for high voltage dc experiments when only unidirectional step-up conversion is required. A bidirectional medium voltage "ladder" shaped dc-dc converter is proposed in [22] which can achieve high step ratio. The advantage is that the converter does not require synchronization of switching between sub-modules. However, the current ratings in different sub-modules are not the same and the inductor currents close to the low voltage side are high.

In medium and high voltage applications, modular multilevel converters (MMCs) used for dc-dc conversion are emerging technologies [9], [23]. These converters are based on conventional MMCs [24]–[29]. MMCs usually require a complicated balancing control scheme to maintain the voltage levels. However, they provide more than two levels and good waveform quality. Cells with fault can also be bypassed while keeping the system operational. High modularity and redundancy are the main advantages of MMCs.

Until now there has been no direct and simple solution for large step-up ratio dc-dc conversion using the MMC approach. This paper presents a new topology and control scheme of a modular multilevel bidirectional dc-dc converter with high step-up ratio. It is based on the conventional boost converter with groups of sub-modules placed in both the diode and switch positions. The proposed converter can achieve a high step ratio. Phase-shifted pulse-width-modulation (PWM) is used to achieve a high effective operating frequency for a given sub-module switching frequency. The proposed converter is bidirectional and suitable for low power dc-dc applications as it has the feature of modularity, simplicity and flexibility. The configuration of the circuit and its operation principle

The authors are with the Department of Electrical Engineering, Imperial College London, London, SW7 2AZ, UK, e-mail: xiaotian.zhang@imperial.ac.uk; t.green@imperial.ac.uk.

Manuscript received May 27, 2014; revised September 22, 2014 and November 19, 2014; accepted December 27, 2014.

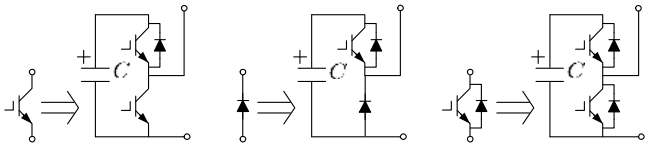


Fig. 1. Single switches and sub-modules with active clamping.

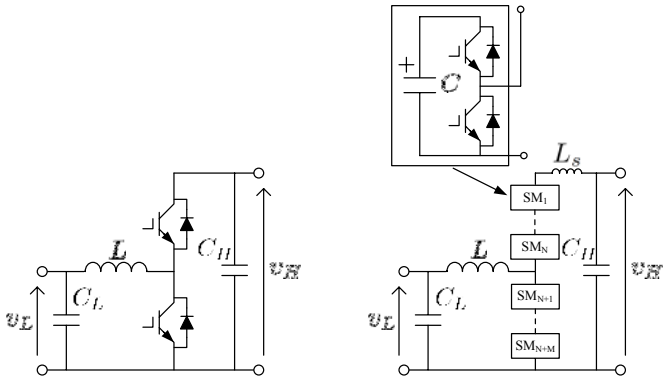


Fig. 2. Bidirectional dc-dc converters. (a) Conventional two-level dc-dc converter. (b) Novel modular multilevel dc-dc converter.

are presented, and verified by experimental results from a downscaled prototype.

II. Bidirectional Modular Multilevel DC-DC Converters

In converting a simple standard switched mode circuit to modular multilevel format, a variety of capacitor clamped sub-modules are required. Fig. 1 shows clamped single switches that use the half-bridge configuration in which replacements for a single IGBT, a diode, and an IGBT with anti-parallel diode are illustrated. The ability to clamp the off-state voltage across a switch when a stack of switches are connected in series is crucial in forming MMC topologies. Using this idea, the modular multilevel inverter topology was generated by clamping the series connected IGBTs in the conventional two-level inverter [25]. With active clamping, each switch has a well-defined voltage and good sharing between sub-modules.

The active clamping idea can also be applied to dc-dc converters. The upper IGBT in the half bridge is termed as clamping IGBT while the lower IGBT is termed as clamped IGBT. The classic bidirectional two-level dc-dc converter is shown in Fig. 2(a). It consists of an inductor on the low voltage side, two IGBTs with anti-parallel diodes and capacitors on both input and output sides. Replacing all the switches by series connected sub-modules with active clamping, the bidirectional buck-boost converter becomes the modular multilevel dc-dc converter shown in Fig. 2(b). The number of upper sub-modules is not required to be the same as the number of the lower sub-modules, however, special operation techniques are required.

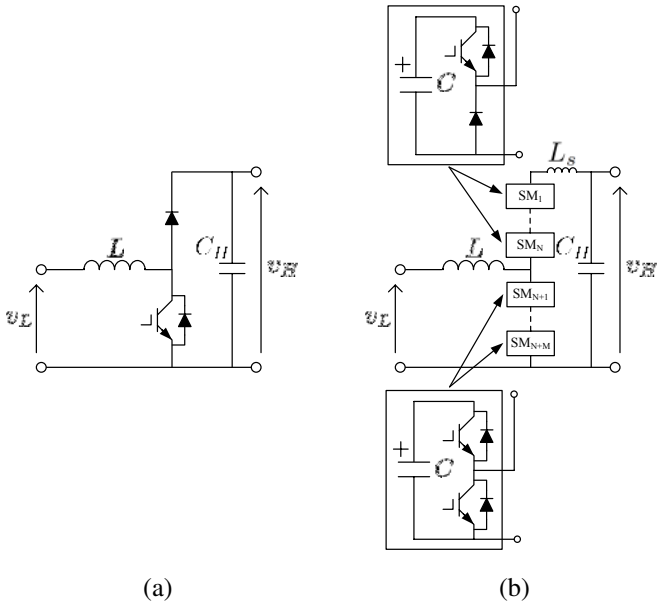


Fig. 3. Unidirectional step-up dc-dc converters. (a) Conventional boost converter. (b) Proposed modular multilevel step-up dc-dc converter.

III. High Step-Up Ratio Modular Multilevel DC-DC Converter

This section describes the operation method for the proposed dc-dc converter. The analysis focuses on step-up dc-dc conversion. To simplify the analysis, the theoretical developments are based on the following assumptions:

1) The switches are ideal and the sub-modules are identical.
2) The converter is lossless.
3) In steady-state the capacitor dc voltages are balanced.
4) The low voltage side inductor, L and high voltage side capacitor, C_H are much larger than the resonant inductor L_S and cell capacitor C.

A. System Configuration

The configuration of the step-up conversion is provided to demonstrate the concept. The most commonly used boost converter topology with a single IGBT and a single diode is shown in Fig. 3(a). The IGBT in the lower position is used for charging the input inductor L. The diode in the upper position of the circuit is automatically commutated on when the inductor discharging current to the high voltage capacitor C_H. Applying active clamping (see Fig. 1) to the two switches, the modular multilevel unidirectional step-up converter with two stacks of sub-modules is obtained as shown in Fig. 3(b). The number of the half-bridge (clamped IGBT) sub-modules in the lower position is M. The number of the chopper (clamped diode) sub-modules in the upper position is N. The output (high-side) voltage is approximately equal to the sum of capacitor voltages of the stack of sub-modules once duty-cycles are accounted for. There will be small differences between the instantaneous voltage across the stack (as sub-modules switch) and the voltage across C_H and this is accommodated by including the small inductor L_S. A large capacitor C_L would normally be present at the input (low

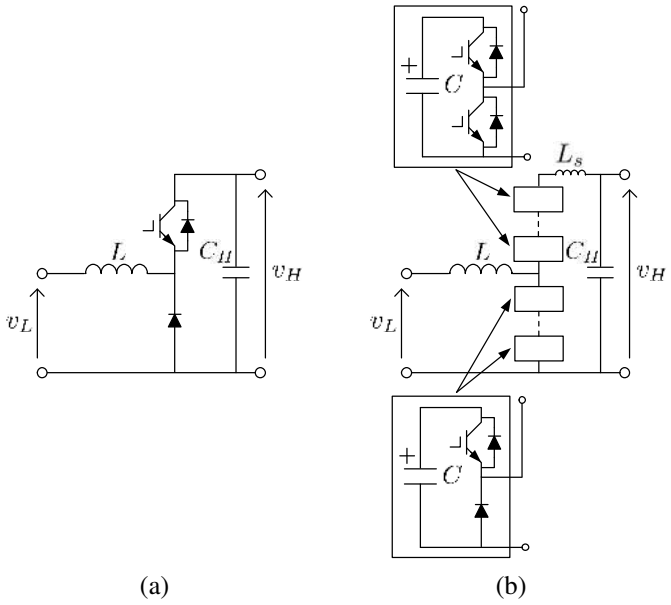


Fig. 4. Unidirectional step-down dc-dc converters. (a) Conventional buck converter. (b) Proposed modular multilevel dc-dc converter.

voltage) side. The step-down conversion is configured using the similar concept. The circuit of the proposed converter for step-down operation is shown in Fig. 4.

B. Phase-Shift Control

The proposed converter has various operating modes resulting in different operating features and step-up ratios. Apart from the high step-up ratio operation mode which is the focus of this paper, the converter can also be used for high step-down ratio dc-dc conversion providing power for auxiliary electronic circuit in medium voltage systems. Moreover, with similar numbers of sub-modules in upper stack and lower stack, the converter can also be used for low step ratio, high-voltage dc-dc conversion. Phase-shifted PWM is used to control the modular multilevel step-up dc-dc converter. Phase-shifted PWM is arranged with a high duty-cycle such that only one sub-module capacitor at a time is out of the series connection and thus the step-up ratio of the circuit becomes dependent on the number of upper cells N. The effective frequency of this excitation is much higher than the frequency of switching of an individual cell.

To demonstrate the principle of interleaved PWM, a step-up converter with four sub-modules in the diode position in the circuit of Fig. 3(b) is considered ($N = 4$). To ensure that either four or three sub-modules are injecting voltage at any time, each must be operated with a duty-cycle above 75%. For illustration, 90% is used. One module could be used in the lower position operating at four times the switching frequency of the upper modules (to give the same effective frequency). Instead, the system will be illustrated with two sub-modules in the lower position operating at twice the frequency of the upper sub-modules and with interleaved pulses. Assuming the sub-module capacitor voltages to be constant, the key waveforms of the sub-module voltages are shown in Fig. 5.

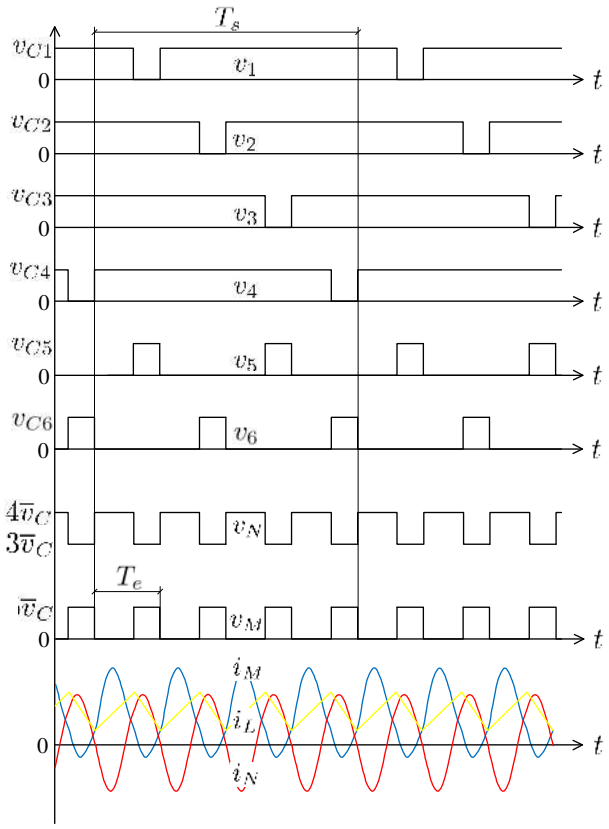


Fig. 5. Time domain key waveforms of the proposed step-up converter.

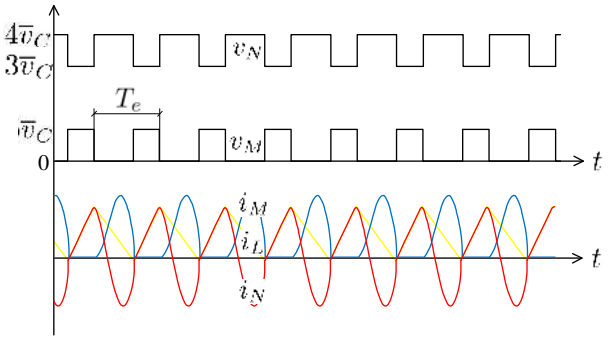


Fig. 6. Time domain key waveforms of the proposed converter with step-down operation.

It can be seen from Fig. 5 that the upper (clamped diode) cells are synchronously switched with the lower (clamped IGBT) cells so that the total voltage of the upper cells v_N and lower cells v_M are complementary. This guarantees an almost constant dc voltage with a small ripple on the high voltage side. The equivalent operating frequency is four times the switching frequency of the upper cells ($f_e = 4f_s$), and is twice the switching frequency of the lower cells. As the frequency of the ripple on the high voltage side is high, the passive components of the output filter do not need to be large. The current waveforms in Fig. 5 will be explained with the step-up operation.

The step-down operation has the same stack voltage wave-

forms as that of the step-up conversion. The voltage waveforms of the sub-modules are not shown. The time domain waveforms of the stacks are shown in Fig. 6. In the step-down operation, the current directions and waveforms are different from that in the step-down operation. The operation of step-down conversion will be analyzed in detail in the next subsection.

C. High Conversion Ratio

The proposed converter is aimed at high step-up ratio dc-dc conversion. The analysis of operation and conversion ratio will proceed by examining one equivalent cycle T_e in Fig. 5. Fig. 7 shows the detailed circuit diagrams with current paths highlighted for the two modes of the circuit. Mode 1 starts when the IGBT in Cell 4 is switched on and ends when the IGBT in Cell 1 switches off (see Fig. 7(a)). The IGBT in Cell 1 switches off when the lower IGBT in Cell 5 switches off and this defines the beginning of Mode 2, Fig. 7(b). Mode 2 ends when the IGBT of Cell 1 is switched on again. Modes 1 and 2 are analogous to the on- and off-states of the simple boost converter but with the difference that current can flow in both paths in both modes. The current flowing through the input inductor, upper cells (clamped diodes) and lower cells (clamped IGBTs) are defined as i_L, i_N and i_M, respectively.

In Mode 1, the current i_L of inductor L is directly charged by the low-side (input) voltage v_L via the IGBTs in Cell 5 and Cell 6. The capacitors C_1, C_2, C_3, and C_4 are in series with the inductor L_s and the high-side (output) capacitor C_H and together they form a resonant tank. Because C_H is large and the cell capacitors are smaller and placed in series, the resonance is dominated by the cell capacitors and C_H can be ignored. Therefore, the resonant frequency is

$$f_r = \frac{1}{2\pi\sqrt{L_s C/N}}. \tag{1}$$

In the case of $N = 4$, $f_r = 1/\pi\sqrt{L_s C}$. When the converter enters Mode 2 from Mode 1, capacitor C_5 is connected into the circuit while capacitor C_1 is out of series connection. The capacitors C_2, C_3, C_4, and C_5 are in resonant tank with L_s and C_H. As the inductor L is relatively large, the current i_L is considered as from a current source. Therefore, the resonant frequency in Mode 2 is also dependent on four series connected capacitors and the series inductor L_s. When the lower (clamped IGBT) cells and the upper (clamped diode) cells use the same capacitors, the resonant frequency in Mode 2 is the same as that in Mode 1.

From Fig. 7(b) it can be seen that the current i_N can not be negative in Mode 2 because one cell (Cell 1 in the figure) is acting as a diode. If the actual resonant frequency is slightly higher than f_e, by the end of Mode 2 the current i_N reaches zero and the circuit operates in discontinuous conduction mode (DCM).

When Mode 1 begins, the current i_L is charged directly by the low-side voltage source. Meanwhile, the current i_N starts to resonate (starting from zero) with the frequency of f_r. The current i_M is i_L minus i_N. When the circuit enters Mode 2 from Mode 1, since v_{C5} is higher than v_L, the inductor current i_L reduces. As the circuit operates in DCM, before the end of the equivalent operating cycle, the current i_N falls to zero and the current i_M is equal to i_L until a new cycle begins. The simulation result later in the paper will illustrate this.

To obtain the voltage conversion ratio, the charging ratio d is defined as the time duration of Mode 1 relative to the period, T_e of the equivalent operating cycle. In steady-state, the increase and decrease of i_L over a equivalent cycle T_e should be the same, hence,

$$\frac{v_L T_e d}{L} = \frac{(v_{Cj} - v_L) T_e (1-d)}{L} \tag{2}$$

with $j = 5$ or $j = 6$. The capacitor voltages of the lower sub-modules can be written as

$$v_{Cj} = \frac{v_L}{1-d}. \tag{3}$$

The sum of average stack voltages v_N and v_M should be equal to the high-side voltage, v_H, which yields

$$v_H = \frac{N-1+d}{N} \sum_{j=1}^{N} v_{Cj} + \frac{1-d}{M} \sum_{j=N+1}^{N+M} v_{Cj}. \tag{4}$$

Under ideal conditions, the capacitor voltages are balanced and equal to $\overline{v}_C$. The voltage conversion ratio can be derived by substituting (3) into (4)

$$\frac{v_H}{v_L} = \frac{N}{1-d}. \tag{5}$$

It can be seen that without increasing d, the conversion ratio can be increased by using higher numbers of upper sub-modules N. In the case of $N = 4$, the conversion ratio is $\frac{v_H}{v_L} = \frac{4}{1-d}$.

The current stresses in the converter should be estimated because it is important in determining the power losses and device ratings. The low-side (input) inductor current i_L comprises a dc component and a sawtooth-shaped ripple. The average current of i_L can be derived from the power consumed on the high voltage side. Here, it is assumed that the load dc current is I_o. Therefore,

$$I_L = \frac{v_H}{v_L} I_o. \tag{6}$$

The peak-to-peak ripple ΔI_L can be obtained from the charging time of inductor L

$$\Delta I_L = \frac{v_L T_e d}{L}. \tag{7}$$

The current stress on the clamped-diode (upper) stack depends on i_N. The dc component of i_N goes on to feed the load and its ac component circulates within the resonant tank. It will be assumed that the ac component of i_N is approximately sinusoidal with root mean square (RMS) value of I_{N1} at the resonant frequency. The power transferred out of the clamped-diode (upper) stack by the flow of the dc current is

$$P_1 = (N-1+d)\overline{v}_C I_o. \tag{8}$$

On the other hand, the ac voltage of the upper stack is a square-wave with a peak-to-peak value of $\overline{v}_C$. Therefore, the RMS value of this square-wave is $\overline{v}_C/2$. The power transferred into

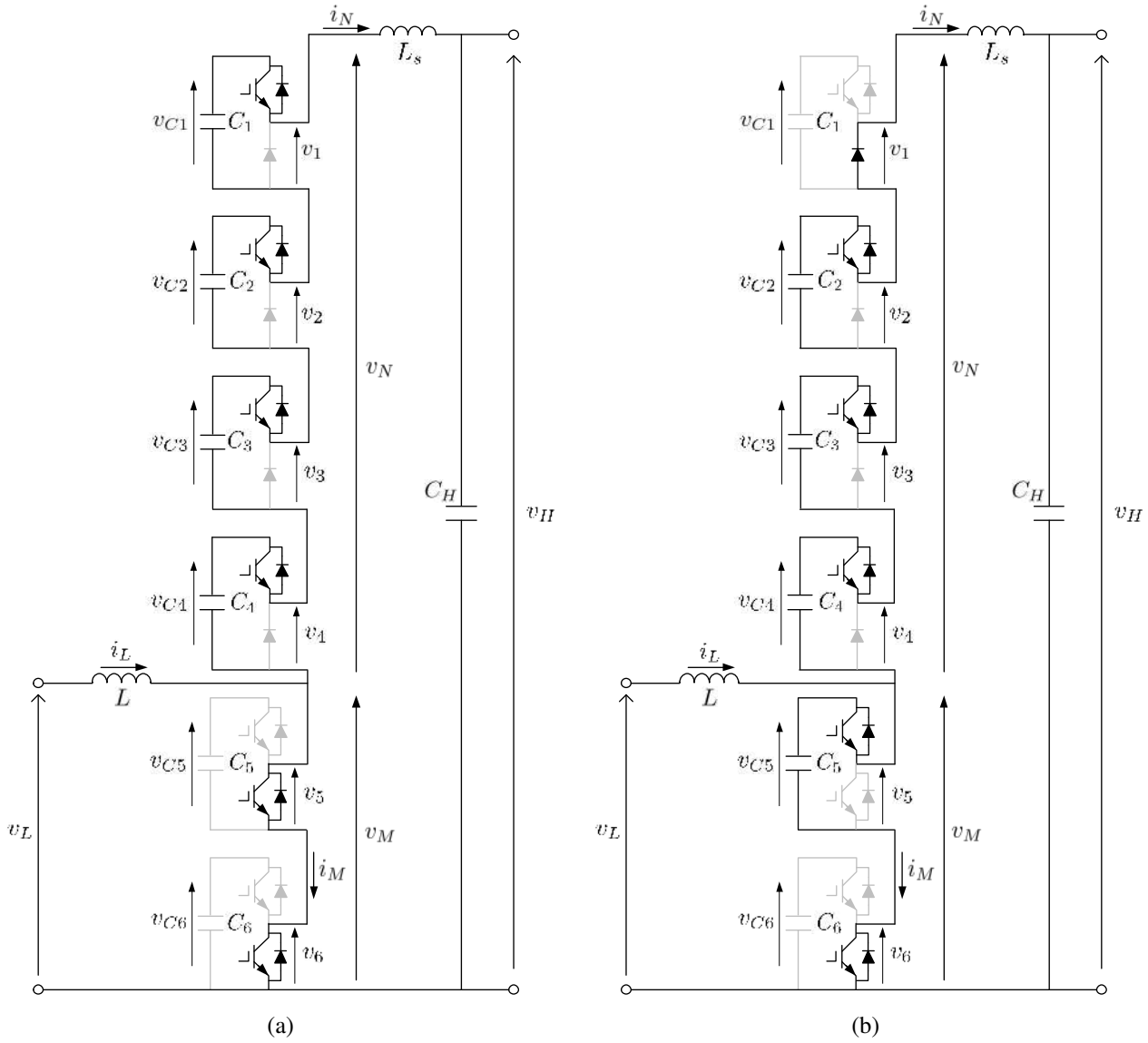


Fig. 7. Step-up operation modes in the first equivalent operating cycle (a) Mode 1. (b) Mode 2.

the stack by the sinusoidal resonant current interacting with the square-wave component of the stack voltage is

$$P_2 = \frac{\overline{v}_C}{2} I_{N1} \lambda \tag{9}$$

with λ the power factor for this voltage and current combination. The value of λ can be obtained from numerical solutions. The maximum, $\lambda = 1$, is achieved when the charging ratio is $d = 0.5$. If the converter is lossless, the dc power and ac power of the upper stack should be equal. Therefore,

$$I_{N1} = \frac{N - 1 + d}{\lambda} I_o. \tag{10}$$

In a more general case, it can be derived that

$$I_{N1} > (N - 1 + d) I_o. \tag{11}$$

After i_L and i_N are estimated, the current stress on the lower stack can be determined by $i_M = i_L - i_N$. A rough estimation of $|i_M| < |i_L| + |i_N|$ can also be used.

Although the converter is proposed for high step-up ratio dc-dc conversion, it also has the capability of step-down dc-dc conversion. Fig. 8 shows the detailed circuit diagrams with current paths highlighted for the two modes of the circuit. Mode 1 starts when the clamped IGBT in Cell 1 is switched on and ends when the clamped IGBT in Cell 1 is switched off (see Fig. 8(a)). When the clamped IGBT in Cell 1 switches off and the clamping IGBT in Cell 5 switches off, the converter begins to enter Mode 2 (see Fig. 8(b)). Mode 2 ends when the clamping IGBT of Cell 6 is switched off. For operation analysis, the current directions are defined opposite to the current directions in the step-up operation.

As the voltage on the inductor L in Mode 1 is higher than that in Mode 2, the current i_L of inductor L is charged in Mode 1 and discharged in Mode 2. During Mode 1, the inductor L_s and the capacitors C_2, C_3, and C_4 are charged, and therefore the clamped diodes in the lower cells are reverse-biased. There is no current flowing through the lower stack. If

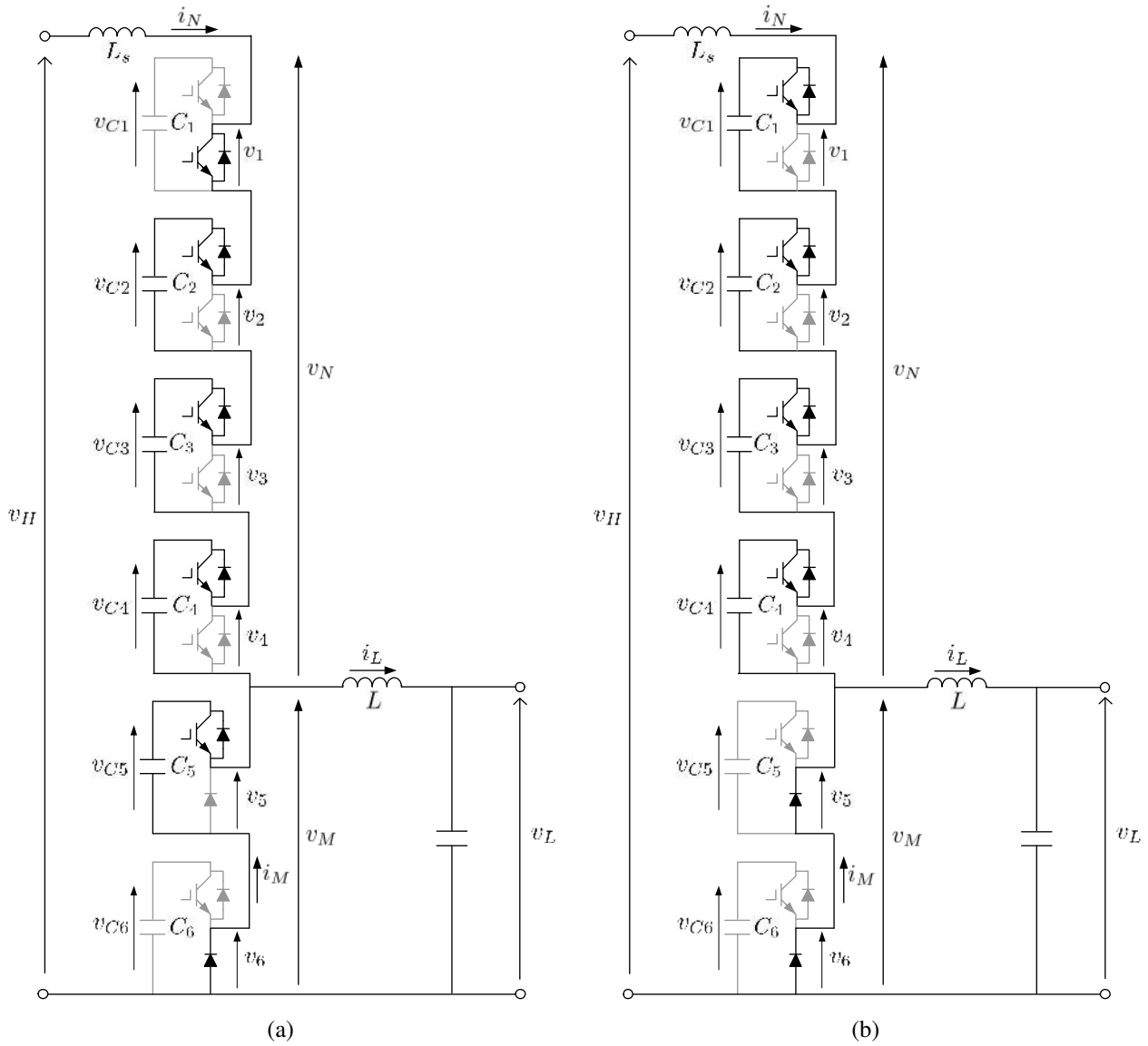


Fig. 8. Step-down operation modes in the first equivalent operating cycle (a) Mode 1. (b) Mode 2.

the capacitor voltages are assumed to be constant, the currents i_L and i_N should increase linearly in Mode 1 and i_L equals i_N. The slight increase of the cell capacitor voltages does not affect the waveshapes obviously. When the converter enters Mode 2 from Mode 1, all the cell capacitors in the upper stack are in series with the inductor L_s. The inductor L start to discharge linearly and the clamped diode in Cell 6 is commutated. Meanwhile, the capacitors C_1, C_2, C_3, and C_4 in series with the inductor L_s form a resonant tank to discharge the energy stored in the passive components from Mode 1. The resonant frequency f_r in the step-down operation is the same as that in the step-up operation. Therefore, the current i_M flowing through the lower stack can be written as

$$i_M = i_L - i_N. \tag{12}$$

This analysis for step-down operation explains the current waveforms in Fig. 6. The inductor current has a sawtooth waveshape and the lower stack current is zero during Mode 1. In Mode 1, the upper stack current is equal to the inductor current. In Mode 2, the upper stack current is discharging with a resonant waveshape, which together with the inductor current determines the lower stack current. To derive the step-down output voltage v_L as a function of charging ratio d (defined in step-up operation) and high voltage v_H, the inductor current i_L is assumed to be the same after one equivalent charging cycle. Hence,

$$\frac{(v_{Cj} - v_L)T_e(1-d)}{L} = \frac{v_L T_e d}{L}. \tag{13}$$

As a result, this cell capacitor voltage is given as $v_{Cj} = \frac{v_L}{1-d}$. On the other hand, as in Mode 2 all the upper cells are withstanding the high voltage, it can be approximated as $N v_{Cj} = v_H$. Therefore, it can be derived that

$$\frac{v_H}{v_L} = \frac{N}{1-d}. \tag{14}$$

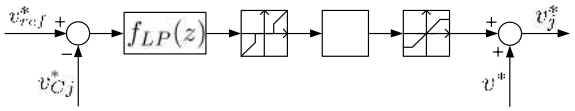


Fig. 9. Half-bridge cell voltage controller.

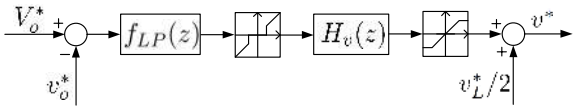


Fig. 10. General control for output voltage.

The step-down operation has the same step ratio function as that in the step-up operation. This means the proposed modular multilevel dc-dc converter is similar to the conventional bidirectional dc-dc converter in terms of step ratio. By changing the current directions, the converter achieves bidirectional power conversion and the same step ratio without modifying the switching arrangement.

D. Capacitor Voltage Clamping Mechanism

The converter has a cell capacitor voltage clamping mechanism. This property can be explained by using the step-up operation for example. As is shown in Fig. 7(a), when the low voltage side inductor is charging (Mode 1), there are capacitors of Cell 1, Cell 2, Cell 3 and Cell 4 supporting the high-side dc voltage. Since the resonant tank formed by the cell capacitors and inductor L_s has an impedance close to zero at the resonant frequency, the ac voltage drop across the resonant components is negligible. Therefore, the output high voltage is almost equal to

$$v_o = v_{C1} + v_{C2} + v_{C3} + v_{C4}. \tag{15}$$

In the next operation mode (see Fig. 7(b)), the output voltage can be expressed as

$$v_o = v_{C2} + v_{C3} + v_{C4} + v_{C5}. \tag{16}$$

Hence, by comparing (15) and (16), as the output voltage is almost constant, it can be stated that $v_{C1} = v_{C5}$. In the next operating cycle, using the same method, one can state that $v_{C2} = v_{C6}$. The following operation mode sequence in the remaining switching cycle gives $v_{C1} = v_{C3} = v_{C5}$ and $v_{C2} = v_{C4} = v_{C6}$. The capacitor voltages of the upper cells are always clamped by the capacitor voltages of the lower cells. Therefore, by balancing the two lower cell capacitors, the dc voltages of all the capacitors should be equal in steady-state. For the converter with only one cell in the lower position, the circuit will have inherent-balancing ability and does not even require additional balancing control. When needed, balancing control for lower cells can be used as shown in Fig. 9.

The reference cell voltage is calculated by averaging the capacitor voltages in half bridge cells

$$v^*_{ref} = \frac{1}{M} \sum_{j=N+1}^{N+M} v^*_{Cj} \tag{17}$$

TABLE I
PARAMETERS OF THE APPLICATION EXAMPLE

Symbol	Quantity	Value
P	Power rating	1 MW
V_L	Nominal low dc voltage	3 kV
V_H	Nominal high dc voltage	30 kV
I_{pk}	Maximum device current	800 A
V_{pk}	Maximum device voltage	8 kV
f_s	Switching frequency	1 kHz
T_e	Equivalent operating cycle	250 μs

with v^*_{Cj} the sampled capacitor voltage. As capacitor voltages contain considerable ac components, first order low-pass filters are used. By comparing the reference voltage to the dc voltage of each cell, a proportional feedback control is used for regulation. A dead zone is created to allow a small tolerance of voltage imbalance. A saturation function is used to limit the adjustable range. As the current at the switching instant, and in average is positive while the cell capacitor is connected in series to the others, this capacitor voltage can be charged by increasing the cell duty-cycle.

The general output voltage feedback control for all sub-modules is shown in Fig. 10. The voltage regulator is represented by $H_v(z)$, usually an anti-windup proportional-integral (PI) controller or a phase lead controller. The gain in this controller for sub-modules in lower position is doubled compared to that in upper position because of the duty-cycle differences (see Fig. 5). The pulse generated by the lower sub-modules is almost complementary to that of upper sub-modules.

IV. STEP-UP CONVERTER APPLICATION EXAMPLE

The proposed converter can be used as a dc transformer with high step-up ratio. One interesting application of the proposed converter is to convert a low voltage 400 V source into distribution voltage level (a few kilo volts). The converter can further be reconfigured with a transformer to provide isolation between input and output. This can boost the dc voltage with a very high step-up ratio and enables direct conversion from a wind turbine dc-link to an HVDC link for example. Due to the page limit, isolated step-up converter is not considered further here. Another application of the proposed converter is to use it to step-up a 2-5 kV wind turbine dc output to the 20-50 kV dc collection level. This requires a typical step-up ratio of $10:1$. In this section, an example of the step-up operation for a turbine converter is provided.

The application example discussed here is based on the proposed MMC dc-dc converter with two lower sub-modules (one redundant) and four upper sub-modules. It operates as a step-up converter from 3 kV to 30 kV. The application is a turbine converter delivering 1 MW power to a 30 kV medium-voltage dc collection bus. Series connected ABB HiPak IGBT modules of type 5SNA 1200G450300 are used as the main switches. The parameters of this example are listed in Table I.

The simulation results of the step-up converter in the application example are shown in Fig. 11. The typical voltage drop across the IGBT is lower than 4 V, which is much smaller than the maximum switch voltage of 4.5 kV. In this example, the affect of the voltage drop can be considered

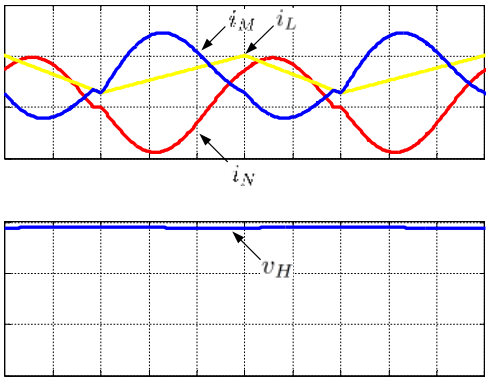


Fig. 11. Simulated currents and output voltage of the converter. (X–axis: Time, 50 μs/div; Y–axis: Magnitude of current, 500 A/div; Magnitude of voltage, 10 kV/div)

negligible. The output voltage is a dc voltage with a ripple lower than 1%. As the converter is operating in resonant mode, the losses calculation is very complicated. According to IEC 61803, the losses measured in HVDC converter is not likely to be a sufficient accurate indication of actual losses. Therefore, IEC 61803 standardizes a method of calculating the power losses. In additional to IEC 61803, the draft IEC 62751 break down power losses into individual components [30]. The power losses of the proposed converter have been calculated based on the simulation results.

The switching losses are comprised of the upper stack IGBT switching losses P_{N1}^{sw}, upper stack diode reverse recovery losses P_{N2}^{sw}, lower stack IGBT switching losses P_{M1}^{sw} and P_{M2}^{sw}. The clamping IGBTs in the upper stack are soft switched under zero current condition. The total energy loss when clamping IGBTs turn off is a function of the current i_N at that switching instant and so is written as $E_{\text{off}}(i_N)$. Therefore, the upper stack clamping IGBTs' switching losses are calculated as $P_{N1}^{\text{sw}} = 2Nf_sE_{\text{off}}(i_N)$. The clamped diodes in the upper stack are soft switched off so that the reverse recovery losses are negligible. The clamping IGBTs in the lower stack are soft switched on and off. However, their anti-parallel diodes have reverse recovery losses as $P_{M1}^{\text{sw}} = 4Mf_sE_{\text{rr}}(i_M)$. The clamped IGBTs in the lower stack are hard switched on and off with the losses written as $P_{M2}^{\text{sw}} = 4Mf_sE_{\text{off}}(i_M) + 4Mf_sE_{\text{on}}(i_M)$. The total switching losses are

$$P_{\text{tot}}^{\text{sw}} = 2Nf_sE_{\text{off}}(i_N) + 4Mf_sE_{\text{rr}}(i_M) + 4Mf_sE_{\text{off}}(i_M) + 4Mf_sE_{\text{on}}(i_M). \quad (18)$$

The switching losses are obtained as $P_{\text{tot}}^{\text{sw}} = 8 \times 1\text{k} \times 1.9 + 8 \times 1\text{k} \times 0.6 + 8 \times 1\text{k} \times 0.7 + 8 \times 1\text{k} \times 1.2 = 35.2$ kW. The conduction losses comprise the upper stack IGBT conduction losses P_{N1}^{con}, upper stack diode conduction losses P_{N2}^{con}, lower stack IGBT conduction losses P_{M1}^{con}, and lower stack diode conduction losses P_{M2}^{con}. The saturation voltage V_{CE} and forward voltage V_{F} are functions of the current, which can be found from the datasheet. The conduction losses of the upper stack IGBTs and diodes are given by $P_{N1}^{\text{con}} = 2NI_NV_{\text{CE}}(I_N)\lambda_{N1}$ and $P_{N2}^{\text{con}} = 2NI_NV_{\text{F}}(I_N)\lambda_{N2}$, respectively. The factor λ represents the ratio of the conduction time to the switching period. The conduction losses of the lower stack are written as $P_{M1}^{\text{con}} = 2MI_MV_{\text{CE}}(I_M)\lambda_{M1}$ and $P_{M2}^{\text{con}} = 2MI_MV_{\text{F}}(I_M)\lambda_{M2}$. The total conduction losses are

$$P_{\text{tot}}^{\text{con}} = 2NI_NV_{\text{CE}}(I_N)\lambda_{N1} + 2NI_NV_{\text{F}}(I_N)\lambda_{N2} + 2MI_MV_{\text{CE}}(I_M)\lambda_{M1} + 2MI_MV_{\text{F}}(I_M)\lambda_{M2}. \quad (19)$$

Summarizing the numeric result of the conduction loss calculation is $P_{\text{tot}}^{\text{con}} = 8\times551\times0.9+8\times642\times0.1+4\times798\times0.84+4\times912\times0.16 = 7.7$ kW. The resistive losses mainly come from the losses in the input inductor and the resonant inductor, represented by $P_L^{\text{res}} = I_L^2r_L$ and $P_{L_s}^{\text{res}} = I_N^2r_{L_s}$, respectively. The total resistive losses are

$$P_{\text{tot}}^{\text{res}} = P_L^{\text{res}} + P_{L_s}^{\text{res}}. \quad (20)$$

The calculated resistive losses are $P_{\text{tot}}^{\text{res}} = 325^2 \times 0.185 + 306^2 \times 0.025 = 21.9$ kW. The total losses are calculated as

$$P_{\text{tot}}^{\text{loss}} = P_{\text{tot}}^{\text{sw}} + P_{\text{tot}}^{\text{con}} + P_{\text{tot}}^{\text{res}}. \quad (21)$$

The total power losses are calculated as $P_{\text{tot}}^{\text{loss}} = 64.8$ kW. By comparing the ratio between power losses and output power, the efficiency in the application example is about 94%. As the switch voltages and currents are high, switching losses are more than half of the total losses. The calculated efficiencies with 1 kHz switching frequency is shown in Table II. It can be seen when voltage level increase, the efficiency is improved. Further improvement of efficiency could be achieved with fewer redundant sub-modules and reduced switching frequency. However, the cost would increase due to larger volume capacitors required.

TABLE II
EFFICIENCY VERSUS INPUT VOLTAGE

Voltage [V]	2000	4000	6000	8000
Efficiency	90.6%	93.2%	94.0%	94.3%

The main disadvantage of non-isolated dc-dc converter compared to transformer coupled dc-dc converters is the high current peak in the high voltage side. This results in high conduction losses and requires high current rating IGBTs. A similar drawback exists in conventional boost converter where the switch needs to withstand the high peak voltage and also should be able to conduct the highest peak current. However, the proposed converter has a modular structure which is scalable in terms of voltage levels and avoids the difficulty of voltage sharing in a series connection of a large number of IGBTs. The equivalent switching frequency of the proposed converter is much higher than that of a standard boost converter while maintaining low switching frequency in each module. Also, it eliminates the use of bulky isolation transformers where entire high voltage applies on the insulation between windings. This converter may not suit all step-up applications but where the voltages ratio is in the region of $10:1$, the advantages of this converter may prove useful. In practice, a specific tradeoff should be made for the chosen application so that the converter can be properly configured.

The experimental test of a downscaled setup is provided in the next section to validate the concept. As the experimental

TABLE III
PARAMETERS OF THE EXPERIMENTAL SYSTEM

Symbol	Quantity	Value
V_L	Nominal low dc voltage	30 V
V_H	Nominal high dc voltage	300 V
I_{pk}	Maximum switch current	30 A
T_b	Sampling period	100 μs
T_e	Equivalent operating cycle	250 μs
L	Low voltage side inductor	821 μH
L_s	Series inductor	120 μH
C_1	Cell 1 capacitor	48.9 μF
C_2	Cell 2 capacitor	49.1 μF
C_3	Cell 3 capacitor	48.2 μF
C_4	Cell 4 capacitor	48.7 μF
C_5	Cell 5 capacitor	48.8 μF
C_6	Cell 6 capacitor	49.3 μF
C_L	Low voltage side capacitor	470 μF
C_H	High voltage side capacitor	180 μF
R_L	Low voltage side load	18 Ω
R_H	High voltage side load	1070 Ω

results are obtained under low voltage operation, the performance may not be good as the result of the simulated application example discussed here. However, the experimental work can prove that the converter is operated as expected.

V. EXPERIMENTAL RESULTS

A downscaled experimental prototype with four upper cells and two lower cells was constructed based on the proposed circuit in Fig. 2(b) for verification. As the experimental operating voltage level is much lower than that of the application example, the IGBT voltage drop and diode forward voltage drop become very significant and the results are expected to show a lower step-up ratio. The dc capacitors on the low-side and the high-side were 470 μF and 180 μF, respectively. The inductors on the low-side and high-side were 821 μH and 120 μH, respectively. The sub-modules were implemented using capacitors with a nominal capacitance value of 50 μF. As a result, the resonant frequency was expected to be approximately 4.1 kHz. The switching frequency for upper cells and lower cells were fixed as 1 kHz and 2 kHz, respectively, giving an effective operational frequency of 4 kHz which is slightly less than the resonant frequency. The detailed circuit parameters are listed in Table III.

A. Open-Loop Tests

The open-loop tests used a fixed charging ratio of $d = 0.6$. For the step-up operation, the input voltage was 30 V and the output voltage was expected to be 300 V. However, as there are high conduction losses in the real switches, with only open-loop control, the high voltage will be lower than the idealized value. For comparison purposes, the converter using the experimental parameters has been simulated here. Fig. 12(a) and (b) show the waveforms of simulated currents and voltages with voltage drop in each switch set to 1 V. The experimental current and voltage waveforms shown in Fig. 12(c) and (d) are quite similar to the corresponding simulation results. However, when the current i_N in Mode 1 cross zero from negative, the current resonance is dramatically damped compared to the simulation result in Fig. 11 (the application example) where this current is freely resonating. This is caused by the voltage drop across the switches (which appears relatively large in this downscaled prototype). When the current i_N is negative in Mode 1, the voltage drop across the diodes is positive compared to v_N. When the current i_N changes to positive, the voltage drop across the IGBTs becomes negative compared to v_N. Because in this mode the inductor L is charging and the capacitor C_H is discharging, the rise of current i_N is suppressed until the end of this mode. When Mode 2 begins, the inductor current i_L is discharged to the high voltage side and the current i_N keeps resonating until it reaches zero or the end of the equivalent operating cycle.

The simulated stack voltage waveforms in Fig. 12(b) are close to the experimentally measured stack voltage waveforms in Fig. 12(d). However, the upper stack voltage v_N is lower than expected amplitude. The sum of the lower stack voltage and upper stack voltage is far below 300 V. As a result, the conversion ratio is lower than $10:1$. The output voltage should be adjusted by closed-loop control to achieve the required level.

For step-down operation, the input high voltage was set to 300 V. The output low voltage is expected to be 30 V. However, as there are voltage drops in the real switches, the output voltage may be lower than expected. Fig. 13(a) and (b) show the simulated step-down current and voltage waveforms with 1 V voltage drop in each switch. In contrast, the experimental step-down current and voltage waveforms in Fig. 13(c) and (d) are quite similar to the relevant simulation results. The inductor L is charging in Mode 1 and discharging in Mode 2. The lower stack current is zero during this mode. The currents i_L and i_N should increase linearly in Mode 1 and i_L equals i_N. In Mode 2, the current i_L start to decrease linearly. All the cell capacitors in the upper stack are in series with the inductor L_s, forming a resonant tank for i_N to discharge. The stack voltage waveforms are in accordance with the waveforms in Fig. 6. This verifies the operation analysis of the proposed converter. The output high voltage is around 25 V with $v_H = 300$ V under open-loop control. The output voltage is lower than the expected value due to the voltage drop across the IGBTs.

The current and voltage waveforms of sub-modules in step-up operation are shown in Fig. 14. As Cell 1 can represent all the upper cells and Cell 6 can represent the lower cells, the waveforms of Cell 1 and Cell 6 are shown. It can be seen in Fig. 14(a) that the resonant current frequency is 4 kHz and the switching frequency of upper cells is 1 kHz. As explained in the previous sections, the interleaved PWM can quadruple the equivalent operating frequency. The switch-on and switch-off currents in the clamped switch of the upper cells are low. In the lower stack (see Fig. 14(b)), the clamped switch of Cell 6 has a switching frequency of 2 kHz. However, the current flowing through has an equivalent frequency of 4 kHz. This verifies the operation principle of the interleaved PWM control.

The step-down operation results are also provided. The current and voltage waveforms of sub-modules in step-down operation are shown in Fig. 15. The waveforms of Cell 1 and Cell 6 are shown. It can be seen in Fig. 15(a) that the resonant current frequency is 4 kHz and the switching frequency of upper cells is 1 kHz. The equivalent operating frequency is

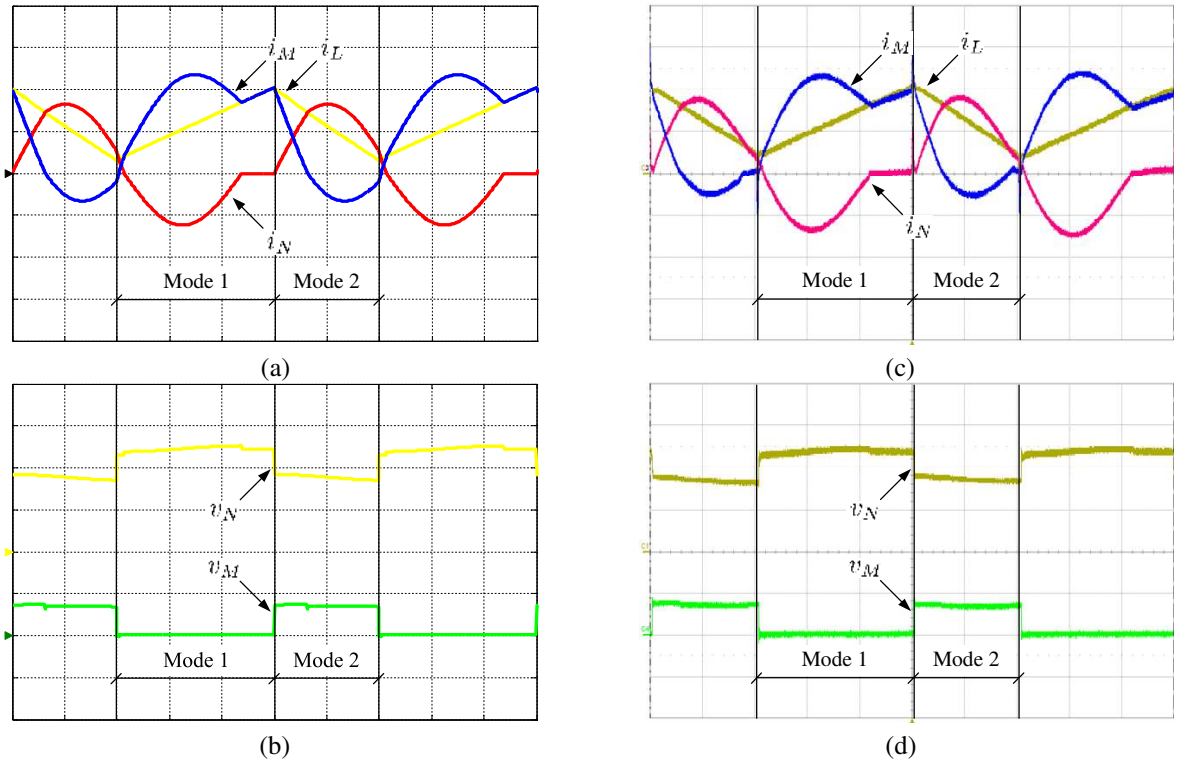


Fig. 12. Simulation and experimental waveforms of the proposed converter for step-up conversion (X–axis: Time, 50 μs/div). (a) Simulated currents (Y–axis: Magnitude of current, 2 A/div). (b) Simulated voltages (Y–axis: Magnitude of voltage, 100 V/div). (c) Experimental currents (Y–axis: Magnitude of current, 2 A/div). (d) Experimental voltages (Y–axis: Magnitude of voltage, 100 V/div).

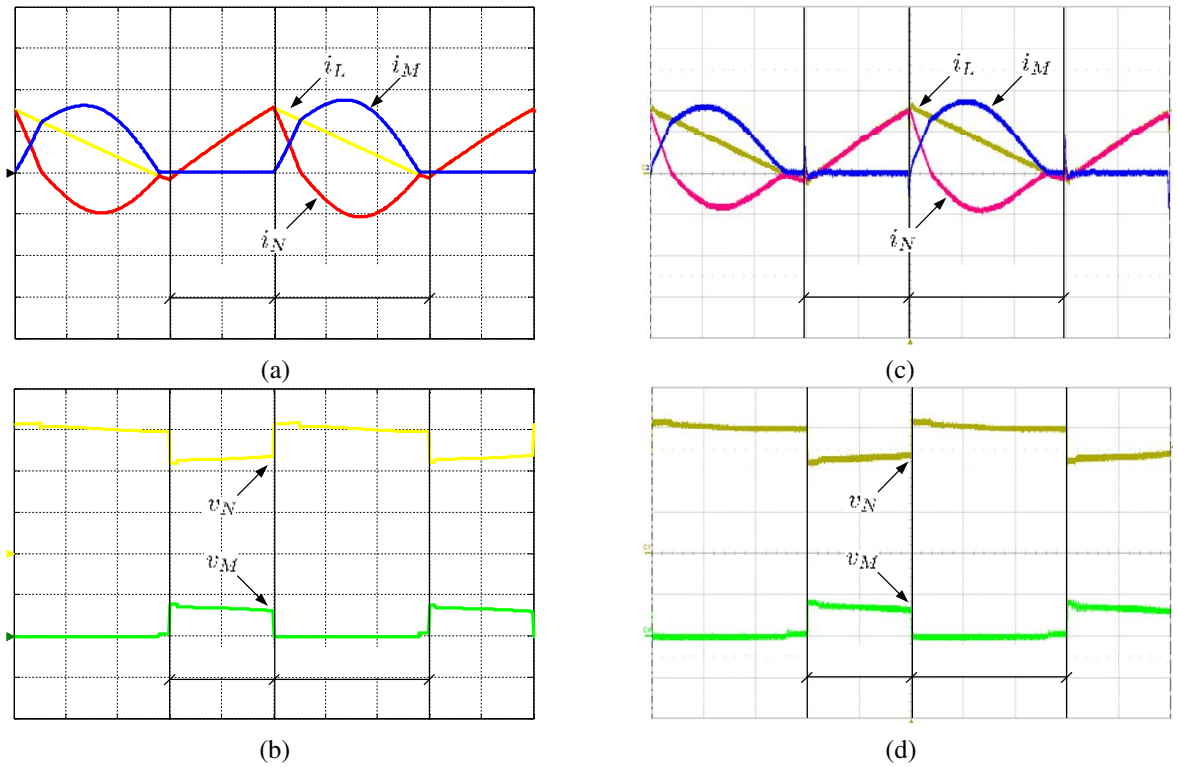


Fig. 13. Simulation and experimental waveforms of the proposed converter for step-down conversion (X–axis: Time, 50 μs/div). (a) Simulated currents (Y–axis: Magnitude of current, 2 A/div). (b) Simulated voltages (Y–axis: Magnitude of voltage, 100 V/div). (c) Experimental currents (Y–axis: Magnitude of current, 2 A/div). (d) Experimental voltages (Y–axis: Magnitude of voltage, 100 V/div).

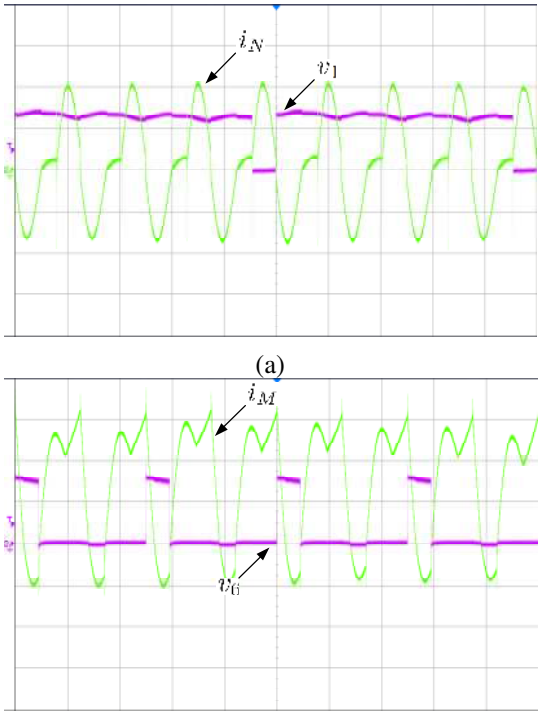


Fig. 14. Experimental step-up sub-module current and voltage of the clamped switch of (a) Cell 1 and (b) Cell 6 (X–axis: Time, 200 μs/div; Y–axis: Magnitude of current, 2 A/div; Magnitude of voltage, 50 V/div).

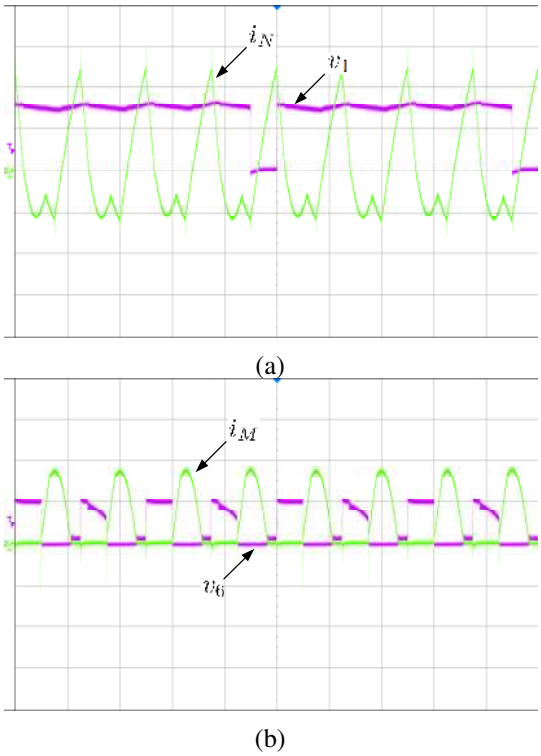


Fig. 15. Experimental step-down sub-module current and voltage of the clamped switch of (a) Cell 1 and (b) Cell 6 (X–axis: Time, 200 μs/div; Y–axis: Magnitude of current, 2 A/div; Magnitude of voltage, 50 V/div).

increased by the interleaved PWM. The resonant frequency is four time as high as the switching frequency. In the Cell 6 of the lower stack (see Fig. 15(b)), the cell current has an equivalent frequency of 4 kHz. As the current is zero when the clamping IGBT in Cell 6 is switched off, the voltage of the clamped diode in Cell 6 can have a voltage lower than the cell capacitor voltage. However, the actual switching frequency used in Cell 6 is still 2 kHz.

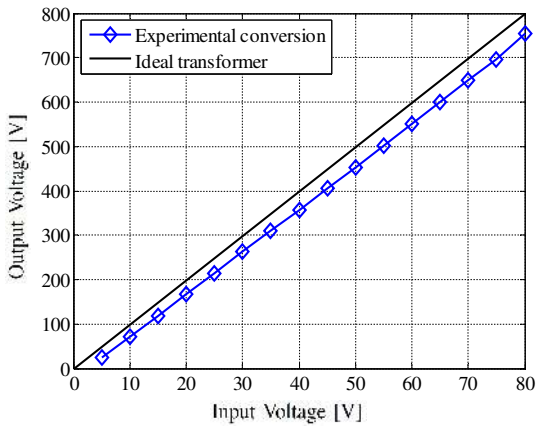


Fig. 16. Experimentally measured step-up high voltages versus different input low voltages.

B. Linearity Tests

The linearity of the output voltage versus the input voltage of the step-up operation is tested. Fig. 16 shows how the output (high-side) voltage varies as the input (low-side) voltage is changed for a fixed charging ratio of $d = 0.6$ (that is, open-loop operation) and also the characteristic of an ideal dc transformer. The circuit shows a linear relation between output and input voltages but with an offset compared to the ideal case. This offset is accounted for by the conduction voltage drops of the IGBTs and diodes of the sub-modules. The low sub-module voltage in this downscaled prototype results in a noticeable relative error in Fig. 16 when the input voltage is especially low.

Furthermore, the linearity of the output voltage versus the input voltage of the step-down operation is shown in Fig. 17. The circuit shows a linear relation between output and input voltages but with an offset compared to the ideal dc transformer. This offset is due to voltage drops across the semiconductors. The relative error in Fig. 17 reduces when the input voltage is increased. When the cell voltage approaches the rated voltage, the step-down ratio will be close to the ideal value.

C. Closed-Loop Tests

Closed-loop control was applied to test the regulation properties of the converter. The output voltages was fed back to a PI controller to change the charging ratio. If the high-side voltage is lower than the ideal value, the controller will increase the effective duty-cycle above the ideal value.

Fig. 18 shows the experimental current and voltage waveforms of the closed-loop controlled step-up conversion. The input low voltage was fixed as $v_L = 30$ V. Compared to the

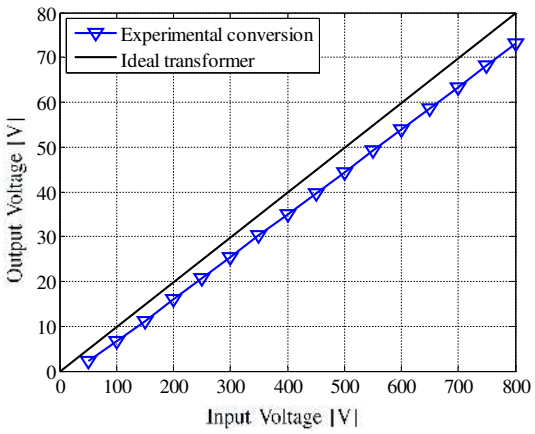


Fig. 17. Experimentally measured step-down low voltages versus different input high voltages.

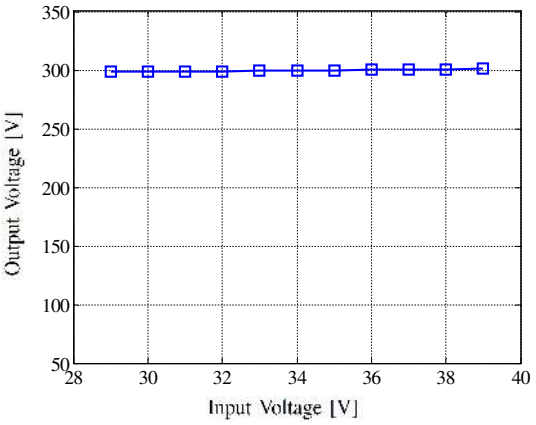


Fig. 19. Experimentally measured step-up voltages with closed-loop control.

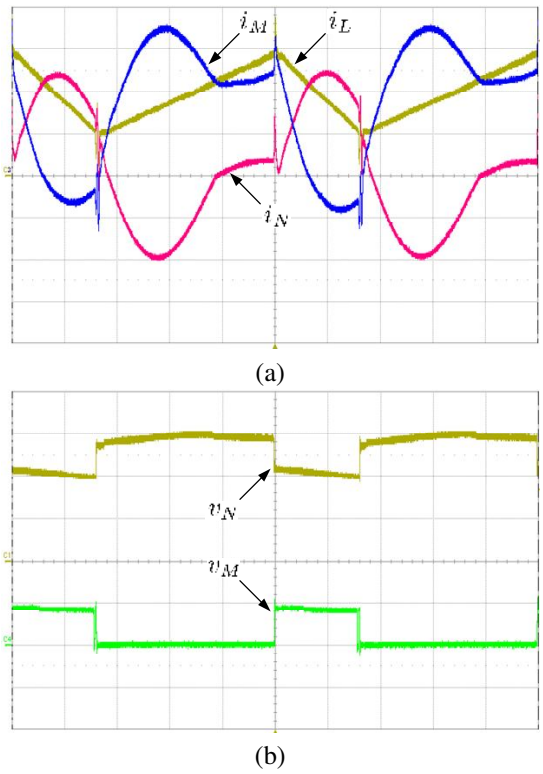


Fig. 18. Experimental waveforms of the closed-loop control step-up conversion (X–axis: Time, 50 μs/div). (a) Experimental currents (Y–axis: Magnitude of current, 2 A/div). (b) Experimental voltages (Y–axis: Magnitude of voltage, 100 V/div).

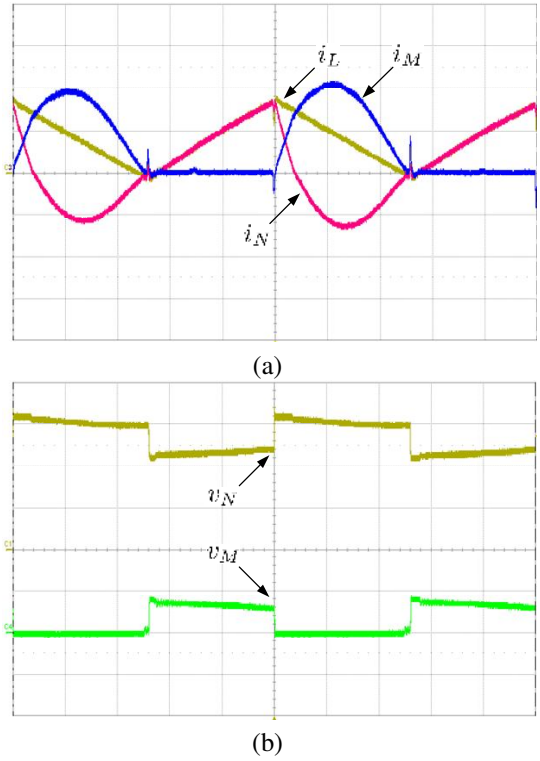


Fig. 20. Experimental waveforms of the closed-loop control step-down conversion (X–axis: Time, 50 μs/div). (a) Experimental currents (Y–axis: Magnitude of current, 2 A/div). (b) Experimental voltages (Y–axis: Magnitude of voltage, 100 V/div).

waveforms under open-loop control with $d = 0.6$ (see Fig. 12), it can be seen that the charging ratio d in the closed-loop curve has been raised by the controller. Moreover, the currents in the converter with the closed-loop controller are higher than those with the open-loop controller and the peak voltage of v_N is higher as well. As a result, the step-up conversion ratio of $10 : 1$ is achieved such that the high voltage v_H is almost 300 V. Fig. 19 shows the experimentally measured step-up voltages under closed-loop control. It can be observed that the closed-loop controller is effective that the high voltage is always controlled around the rated value 300 V.

Fig. 20 shows the experimental current and voltage waveforms of the closed-loop controlled step-down conversion. The input high voltage was fixed as $v_H = 300$ V. Compared to the waveforms under open-loop control with $d = 0.6$ (see Fig. 13), it can be seen that the charging ratio d in the closed-loop controlled converter has been reduced. Moreover, the currents in the converter with the closed-loop controller are higher than those with the open-loop controller and the duty-cycle of voltage v_M is higher as well. As a result, the step-down conversion ratio of $1 : 10$ is achieved such that the low voltage v_L is 30 V. Fig. 21 shows the experimentally measured output voltages under closed-loop control. It can be seen that

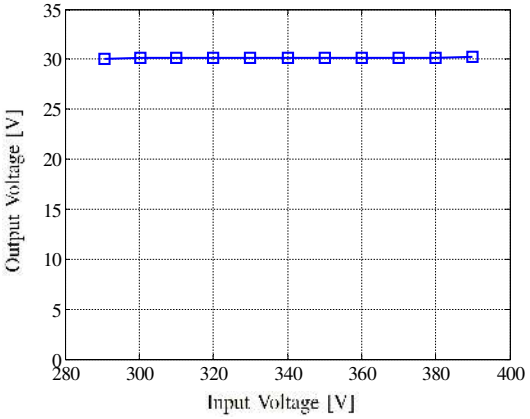


Fig. 21. Experimentally measured step-down voltages with closed-loop control.

TABLE IV
CELL CAPACITOR VOLTAGES

	Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6
Step-up [V]	70.78	71.09	70.17	70.94	89.59	89.89
Step-down [V]	75.88	76.11	75.87	76.09	40.10	40.09

the closed-loop controller is effective that the low voltage is always regulated around the rated value 30 V.

The capacitor voltages were also measured and are shown in Table IV under nominal input voltage conditions. The voltages in upper sub-modules are balanced with each other, and the voltages in lower sub-modules are balanced as well. This gives the advantage of sharing the high voltage among sub-modules. In real applications with high operation voltage, the voltage drop across semiconductors is relatively low and the voltage differences between sub-modules should be very small.

VI. CONCLUSION

The new transformerless MMC dc-dc converter has been presented and analyzed. Two stacks of sub-modules in series arrangement support the high voltage. The dc capacitors of the sub-modules are used also for resonant operation. The proposed converter has a simple configuration and bidirectional conversion ability. The step-up operation and the step-down operation are demonstrated. This converter is capable of operating under open-loop control as a dc transformer with good linearity. Alternatively, closed-loop control can be applied for trimming of the output voltage. The operating principle was verified through a bench-scale experimental prototype. The proposed converter may exhibit relatively high losses because of the high ac current that resonates in the sub-modules but reasonably high efficiency was shown to be possible in high voltage applications such as a 1 MW, 3 kV to 30 kV dc-dc converter. Further efficiency improvement can be achieved with lower switching frequency, but cell capacitors with a higher volume will be required. The converter can achieve a large step-up conversion ratio without the use of transformers and can also be used for step-down conversion. The proposed converter has the features of modularity, scalability and simplicity and these may make it attractive in some applications.

REFERENCES

[1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, Aug 2010.

[2] J. I. Leon, S. Kouro, S. Vazquez, R. Portillo, L. G. Franquelo, J. M. Carrasco, and J. Rodriguez, "Multidimensional modulation technique for cascaded multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 2, pp. 412–420, Feb 2011.

[3] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 2930–2945, Dec 2007.

[4] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28–39, June 2008.

[5] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2197–2206, July 2010.

[6] M. A. Perez, J. Rodriguez, E. J. Fuentes, and F. Kammerer, "Predictive control of ac-ac modular multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 7, pp. 2832–2839, July 2012.

[7] E. Solas, G. Abad, J. A. Barrena, S. Aurtenetxea, A. Carcar, and L. Zajac, "Modular multilevel converter with different submodule concepts-part ii: Experimental validation and comparison for hvdc application," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4536–4545, Oct 2013.

[8] M. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modelling, control schemes and applications of modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 4–17, Jan 2015.

[9] J. Ferreira, "The multilevel modular dc converter," *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4460–4465, Oct. 2013.

[10] J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Transactions on Industry Applications*, vol. 32, no. 3, pp. 509–517, 1996.

[11] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[12] L. Harnefors, A. Antonopoulos, S. Norrga, L. Angquist, and H.-P. Nee, "Dynamic analysis of modular multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 7, pp. 2526–2537, July 2013.

[13] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *Proceeding of IEEE Power Electronics Specialists Conference*, 1992, pp. 397–403.

[14] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Transactions on Industry Applications*, vol. 37, no. 2, pp. 611–618, Mar./Apr. 2001.

[15] S. Busquets-Monge, S. Alepuz, and J. Bordonau, "A bidirectional multilevel boost-buck dc-dc converter," *IEEE Transactions on Power Electronics*, vol. 26, no. 8, pp. 2172–2183, 2011.

[16] T. Todorcevic, P. Bauer, J. A. Ferreira, and R. van Kessel, "Bidirectional modular multilevel dc-dc converter control and efficiency improvements through separate module control method," in *Proceeding of IEEE Energy Conversion Congress and Exposition*, 2013, pp. 2038–2043.

[17] K. D. T. Ngo and R. Webster, "Steady-state analysis and design of a switched-capacitor dc-dc converter," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 30, no. 1, pp. 92–101, 1994.

[18] F. Khan and L. Tolbert, "A multilevel modular capacitor-clamped DC-DC converter," *IEEE Transactions on Industry Applications*, vol. 43, no. 6, pp. 1628–1638, Nov./Dec. 2007.

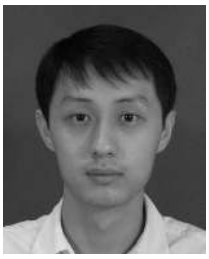
[19] D. Cao and F. Z. Peng, "Zero-current-switching multilevel modular switched-capacitor DC-DC converter," *IEEE Transactions on Industry Applications*, vol. 46, no. 6, pp. 2536–2544, Nov./Dec. 2010.

[20] G. Ortiz, H. Uemura, D. Bortis, J. W. Kolar, and O. Apeldoorn, "Modeling of soft-switching losses of igbts in high-power high-efficiency dual-active-bridge dc/dc converters," *IEEE Transactions on Electron Device,*, vol. 60, no. 2, pp. 587–597, Feb 2013.

[21] C.-M. Young, M.-H. Chen, T.-A. Chang, C.-C. Ko, and K.-K. Jen, "Cascade cockcroft-walton voltage multiplier applied to transformerless high step-up dc-dc converter," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 2, pp. 523–537, Feb 2013.

[22] M. Kasper, D. Bortis, and J. W. Kolar, "Novel high voltage conversion ratio rainstick dc/dc converters," in *Proceeding of IEEE Energy Conversion Congress and Exposition*, 2013, pp. 789–796.

[23] X. Zhang, T. C. Green, and A. Junyent-Ferre, "A new resonant modular multilevel step-down dc-dc converter with inherent-balancing," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 78–88, Jan 2015.
[24] T. Luth, M. M. C. Merlin, T. C. Green, F. Hassan, and C. D. Barker, "High-frequency operation of a dc/ac/dc system for hvdc applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4107–4115, Aug 2014.
[25] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *IEEE Power Tech Conference Proceedings, Bologna*, vol. 3, 2003, pp. 1–6.
[26] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable modular multilevel converters for hvdc-transmission," in *IEEE Power Electronics Specialists Conference*, 2008, pp. 174–179.
[27] A. Antonopoulos, L. Angquist, L. Harnefors, K. Ilves, and H.-P. Nee, "Global asymptotic stability of modular multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 2, pp. 603–612, Feb 2014.
[28] E. Solas, G. Abad, J. A. Barrena, S. Aurtenetxea, A. Carcar, and L. Zajac, "Modular multilevel converter with different submodule concepts-part i: Capacitor voltage balancing method," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4525–4535, Oct 2013.
[29] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2633–2642, Aug 2010.
[30] P. S. Jones and C. C. Davidson, "Calculation of power losses for mmc-based vsc hvdc stations," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, Sep. 2013, pp. 1–10.



Xiaotian Zhang (S'11-M'12) was born in Xi'an, China, in 1983. He received the B.S. (with honors) and M.S. degrees in Electrical Engineering from Jiaotong University, Xi'an, China, in 2006 and 2009, respectively, and the PhD degree (with honors) in electrical engineering and electronics from the University of Liverpool, U.K., in 2012.

Since 2013, he has been with the Department of Electrical Engineering, Imperial College London, U.K. His research interests include control modelling and circuit design of multilevel converters for high voltage applications.

Tim C. Green (M'89-SM'02) received a B.Sc. (Eng) (first class honours) from Imperial College London, UK in 1986 and a Ph.D. from Heriot-Watt University, Edinburgh, UK in 1990. Both degrees were in electrical engineering. He is a Chartered Engineer in the UK. He was a Lecturer at Heriot-Watt University until 1994 and is now a Professor of Electrical Power Engineering at Imperial College London, Deputy Head of the Electrical and Electronic Engineering Department and Director of the Energy Futures Lab. His research interest is in formulating the future form the electricity network to support low-carbon futures. A particular theme is how the flexibility of power electronics and control can be used to accommodate new generation patterns and new forms of load, such as EV charging, as part of the emerging smart grid. He has particular interests in offshore DC networks and of management of low voltage networks. He leads the HubNet consortium of 8 UK universities coordinating research in low-carbon energy networks and is the Network Champion for the Research Councils UK.