

# The MuPix System-on-Chip for the Mu3e Experiment

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## Abstract

Mu3e is a novel experiment searching for charged lepton flavor violation in the rare decay  $\mu^+ \rightarrow e^+e^-e^+$ . Decay vertex position, decay time and particle momenta have to be precisely measured in order to reject both accidental and physics background. A silicon pixel tracker based on 50  $\mu\text{m}$  thin high voltage monolithic active pixel sensors (HV-MAPS) in a 1 T solenoidal magnetic field provides precise vertex and momentum information. The MuPix chip combines pixel sensor cells with integrated analog electronics and a periphery with a complete digital readout. The MuPix7 is the first HV-MAPS prototype implementing all functionalities of the final sensor including a readout state machine and high speed serialization with 1.25 Gbit/s data output, allowing for a streaming readout in parallel to the data taking. The observed efficiency of the MuPix7 chip including the full readout system is  $\geq 99\%$  in a high rate test beam.

**Keywords:** Silicon sensors, Pixel detectors, Monolithic, CMOS, HV-MAPS, Mu3e

## 1. The Mu3e Experiment

The Mu3e experiment [1] will be carried out at the Paul Scherrer Institute (PSI) in Switzerland aiming to find or exclude the decay  $\mu^+ \rightarrow e^+e^-e^+$  at a sensitivity level in branching ratio of  $10^{-16}$ , improving the current limit of  $10^{-12}$  established by SINDRUM in 1988 [2] by four orders of magnitude. This requires operating the Mu3e experiment at very high muon stopping rates of  $\mathcal{O}(10^9 \text{ Hz})$  for several years while keeping the background below the  $10^{-16}$  level. In particular, background from radiative muon decays with internal conversion  $\mu^+ \rightarrow e^+e^-e^+\nu\bar{\nu}$  needs to be suppressed by an excellent momentum resolution well below 0.5 MeV/c. Accidental background can be suppressed by a combination of precise time resolution of  $\mathcal{O}(100 \text{ ps})$ , vertex resolution of  $\mathcal{O}(200 \mu\text{m})$  and a very good momentum resolution. Since electrons and positrons from the muon decay at rest have a maximum momentum of 53 MeV/c, the momentum and vertex resolutions are limited by multiple Coulomb scattering. This requires the reduction of the detector material to 0.1% of a radiation length  $X_0$  per detector layer.

The Mu3e detector is composed of an extremely lightweight silicon pixel detector [3] surrounding a double cone target in a magnetic field of 1 T in combination with a scintillating fiber and a scintillating tile detector [4, 5] for precise timing, see

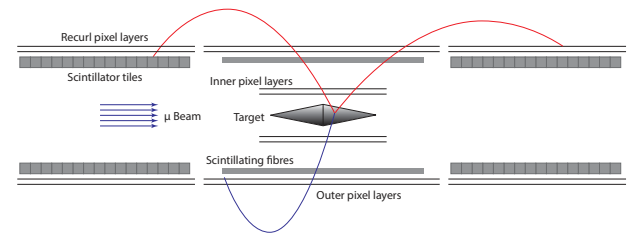


Figure 1: Mu3e detector with signal event.

Fig. 1. The silicon pixel detector is based on high voltage monolithic active pixel sensors (HV-MAPS) thinned to 50  $\mu\text{m}$ , readout via aluminium flex prints and mounted on Kapton<sup>®</sup> frames.

## 2. High Voltage Monolithic Active Pixel Sensors

High voltage monolithic active pixel sensors [6, 7] are pixelated detectors based on the commercially available HV-CMOS technology. Reverse biasing the deep N-well in the P-substrate with -60 V to -85 V leads to a depletion zone in the order of 15  $\mu\text{m}$  thickness as reported in [7]. Ionizing radiation creates electron-hole pairs in the depletion zone. The electrons are collected via drift within 1 ns, see Fig. 2. Because of the very thin active detection layer, thinning to 50  $\mu\text{m}$  is possible. In addition, CMOS analog and digital electronics can be implemented in the N-well so no extra readout chip is required.

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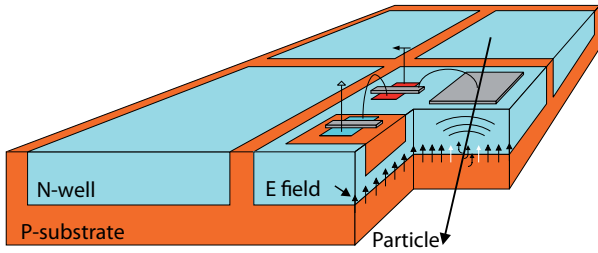


Figure 2: HV-CMOS pixel detector scheme [6].

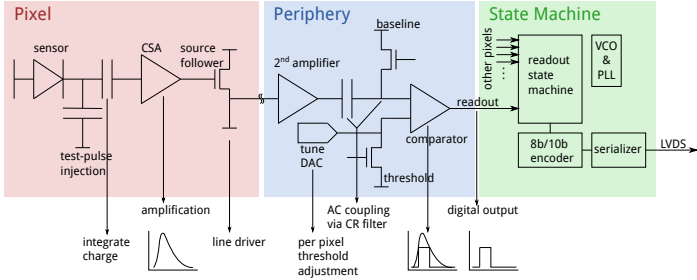


Figure 3: Block diagram of the signal path in the MuPix7 chip.

### 3. The MuPix System on Chip

For the MuPix chip to be used in the Mu3e experiment, a pixel size of  $80 \times 80 \mu\text{m}^2$ , an overall dimension of  $2 \times 2 \text{cm}^2$  and a thickness of only  $50 \mu\text{m}$  is required.

Several smaller prototypes implemented in the AMS 180 nm HV-CMOS process have been extensively characterized [8, 9, 10, 11]. A line driver in the pixel cell sends the analog pulse over a point-to-point connection to a corresponding digital pixel in the periphery. The signal is discriminated, a hit flag is registered and an eight-bit time-stamp is latched. Additionally, each digital pixel has a four-bit tune digital to analog converter (DAC) which allows to adjust the baseline for a common threshold in order to correct for pixel to pixel variations, see Fig. 3. The analog part with the preamplifier is implemented in the deep N-well above the sensitive pixel area, while the digital part is located in a small inactive region next to the pixel matrix in order to avoid digital crosstalk, see Fig. 4.

The MuPix7 prototype is the first in its series which integrates the complete readout circuitry, including a readout state machine, fast clock circuitry and fast serial output. At the beginning of each readout cycle, the hit flags of all pixels are copied to a second register. These registers drive a priority logic selecting the first hit in each column, which is then copied to a buffer in the column periphery. At the same time, the pixel hit flag is cleared and set ready to detect the next hit. A second priority logic identifies the first column with a hit, which is then sent to the fast output link. This is repeated until all column buffers are empty and the next hit in each column can be copied to the periphery. If all hits are read or an adjustable number of hits is surpassed, the cycle starts from the beginning. This readout is controlled by an on chip state machine running at 62.5 MHz and runs in parallel to the data taking. The only

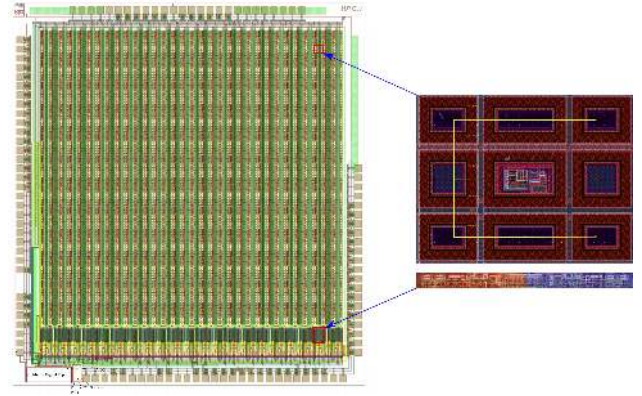


Figure 4: MuPix7 layout and zoom-in of one pixel and the corresponding electronics in the periphery. The pixel cell is subdivided in nine diodes with the amplifier electronics implemented in the central one. Note that periphery electronics serving two pixels is shown.

dead time incurred is in the hit pixels waiting for the copying to the column periphery. At low occupancy, this is comparable to the shaping time of around  $1 \mu\text{s}$ . The output data consists of the row, column address and Gray-encoded time-stamp of hits interspersed with control words and synchronization counters. The data is 8b/10b encoded, serialized and sent off-chip via a 1.25 Gbit/s low voltage differential signaling (LVDS) link. The clocks required for the time-stamp generation, the readout state machine, the serializer and the fast link are all generated on-chip. To this end a voltage controlled oscillator together with a phase locked loop connected to an external 125 MHz clock have been implemented. The MuPix7 prototype has 32 by 40 pixels of  $103 \times 80 \mu\text{m}^2$  size and was characterized in numerous laboratory tests and test beam campaigns.

The MuPix7 is directly glued and bonded to a dedicated test board, the MuPix7 printed circuit board (PCB), which delivers ripple-free and stabilized low voltage, high voltage, threshold and test pulses to the chip. A commercially available state-of-the-art FPGA (ALTERA Stratix IV) on a PCIe card is used for generating the master clock and handling the communications to and from the MuPix7 chip. LVDS is used for all signals with speeds of up to 1.25 Gbit/s. Four planes of MuPix7 PCBs were combined in a MuPix beam telescope [12], with first, third and fourth MuPix7 providing the track reference and the second MuPix7 as device under test (DUT).

### 4. MuPix7 Performance

The MuPix7 chip is the first HV-CMOS chip with an internal readout and a fast 1.25 Gbit/s LVDS serial data output. The high speed serial output data shows very good signal quality, see Fig. 5. The eye opening has 131 mV height with 5.4 mV RMS noise and 525 ps width with 45 ps jitter when probed with high bandwidth Sub-Miniature-A (SMA) cables close to the chip outputs.

High hit rate tests up to 380 kHz per sensor have been performed at PSI with a 250 MeV/c mixed positron, muon and pion beam. At the CERN SPS, a 180 GeV/c pion beam with an in-

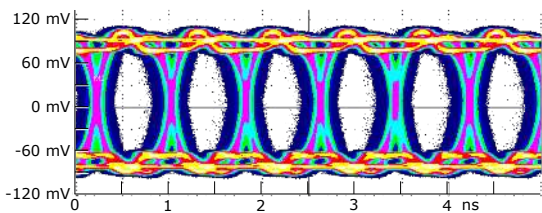


Figure 5: Eye diagram of MuPix7 fast serial data output, shown as signal amplitude in mV versus time in ns.

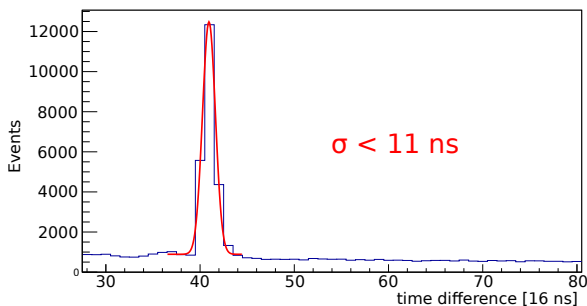


Figure 6: Time resolution of the MuPix7 chip.

stantaneous hit rate of above 500 kHz per sensor plane was used for testing. Further studies have been carried out with a 1 GeV/c electron beam of MAMI at the Johannes Gutenberg University Mainz and a 2 to 6 GeV/c positron beam at DESY - each with a hit rate of around 1 kHz.

The rate capability tests were performed at the PSI with hit rates between 0.15 kHz and 380 kHz. At 380 kHz the chip was using only about 4% of its available bandwidth. The theoretical upper limit for the MuPix7 chip is a hit rate of 30 MHz corresponding to a flux of 284 MHz/cm<sup>2</sup>. For the expected rate of  $2 \cdot 10^9$  muon stops per second at the Mu3e experiment the charged particle flux will be up to 40 MHz/cm<sup>2</sup>. A full sized chip will have up to four fast serial output links.

The time resolution of the MuPix7 has been determined by sampling with a 62.5 MHz Gray counter, see Fig. 6. Plastic scintillators were used as time reference. A Gaussian fit of the relative time between MuPix7 hit time and scintillator signals yields  $\sigma = 11$  ns, which gives an upper limit of the time resolution.

For the measurement of the particle detection efficiency, the noise of each pixel has been equilibrated to 1 Hz for one global threshold with the help of the tune DACs and a threshold scan has been performed. In the plateau, hit efficiencies of around 99.5% have been determined for the 250 MeV mixed positron, muon and pion beam at PSI, see Fig. 7. The noise in the efficiency plateau region is in the range of 2 to 12 Hz per pixel, with a power consumption of around 300 mW/cm<sup>2</sup>, which is within the Mu3e pixel detector cooling budget of 400 mW/cm<sup>2</sup>.

In order to study the dependency of the detection efficiency on the thickness of the depletion zone, threshold scans at four different angles with respect to the positron beam were con-

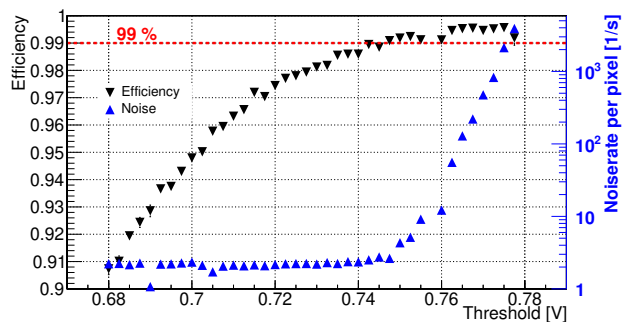


Figure 7: Hit efficiencies and noise versus threshold for the MuPix7.

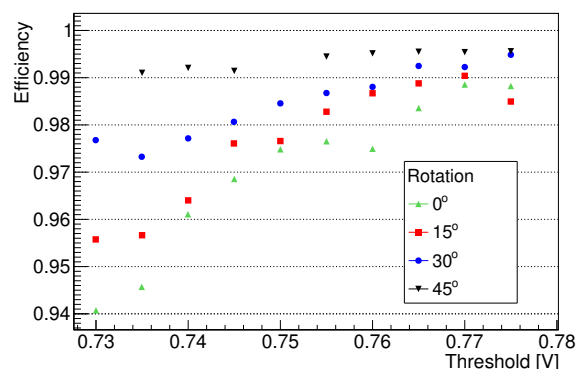


Figure 8: Hit efficiencies versus threshold for the MuPix7 chip at angles of 0°, 15°, 30° and 45° with respect to the beam axis. Statistical errors are smaller than the markers.

ducted, using a 4 GeV/c positron beam at DESY, see Fig. 8. The measurement taken at an angle of 45° shows a much broader efficiency plateau as compared to the 0° measurement. 45° corresponds to a  $\sqrt{2}$  times thicker effective depletion zone. A planned change of the substrate resistivity from 20  $\Omega$ cm to 80  $\Omega$ cm should lead to an increase in number of signal electrons by a factor of two and thus an even broader efficiency plateau.

The spatial resolution of the MuPix7 chip has been measured using a 4 GeV/c positron beam at DESY and a MuPix beam telescope, see Fig. 9. The unbiased hit residuals are  $\sigma_x = 38.1 \mu\text{m}$  and  $\sigma_y = 30.6 \mu\text{m}$ , which is consistent with the intrinsic single cell resolution (pitch/ $\sqrt{12}$ ) folded with uncertainties from multiple Coulomb scattering and tracking. All studies above were carried out with MuPix7 samples thinned to 50  $\mu\text{m}$  or 62  $\mu\text{m}$ . No influence of the thickness on the performance was observed.

## 5. Conclusions

The current prototype MuPix7 is a 50  $\mu\text{m}$  thin full system on chip combining pixel sensor, analog electronics and full digital readout. All pixels and the integrated readout circuitry are always running in parallel, so no dead-time on top of the signal shaping time of around 1  $\mu\text{s}$  is induced. The newly developed 1.25 Gbit/s fast serial data readout has an excellent performance

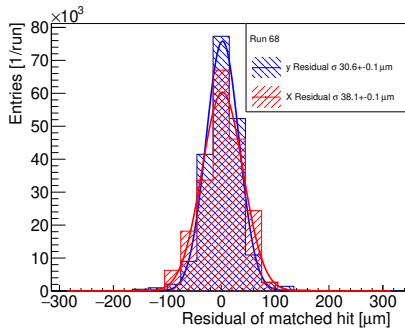


Figure 9: Spatial resolution of the MuPix7 chip.

with large eye openings and has been reliably operated in multiple test beam campaigns. The time resolution of the MuPix7 time stamps is better than  $\sigma = 11$  ns. The spatial resolution of  $\leq 38.1 \mu\text{m}$  is dominated by the pixel cell size contribution. The full system hit efficiency is  $\geq 99\%$ .

The MuPix7 chip performs very well, meeting all requirements that can be investigated on a small scale prototype. Upscaling to a  $13 \times 23 \text{ mm}^2$  pixel chip is the next step, together with an investigation of higher resistivity substrates.

The MuPix7 is a chip demonstrating the unique capabilities of HV-MAPS technology. High rates and lowest amount of traversed material make them the ideal candidate for future applications, enabling precision experiments like Mu3e. The MuPix chip has also been chosen as detector for the PANDA Lumi detector [13] and the P2 experiment [14]. Their moderate price allows for relatively large instrumented areas, making them a candidate for track-trigger applications at large radii in LHC-type experiments. Irradiation studies are ongoing to validate the HV-MAPS technology for LHC.

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