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Topics: Noise measurement, Noise (electronics), Capacitive sensing, Relaxation oscillator and Capacitance

The Noise Performance of a High-Speed Capacitive-Sensor Interface Based on a Relaxation Oscillator and a Fast Counter

Manel Gasulla, *Member, IEEE*, Xiujun Li, and Gerard C. M. Meijer

***Abstract*—This paper presents the analysis and experimental results on the noise performances of a capacitive-sensor interface. The interface is able to measure low capacitance values in the order of picofarads and is implemented with a simple relaxation oscillator, a fast counter, and a microcontroller. The goal is to find the criteria to implement a low-noise system, so that, even with a short measuring time, low noise can be obtained. Experimental results are performed in order to prove the validity of the theoretical analysis. The achieved resolution, with a measuring time of 20 ms, was better than 14.2×10^{-7} for the measurement of a capacitance value of 2.2 pF.**

***Index Terms*—Capacitance measurement, capacitance transducers, jitter, oscillator noise, relaxation oscillator.**

I. Introduction

CAPACITIVE sensors are used in a wide variety of measurement and control systems, such as liquid-level gauges, pressure meters, accelerometers, and precision positioners. In these applications, the capacitances to be measured are often in the range of 0.1–10 pF and, normally, a high resolution (low noise) is required.

Electronic interfaces whose output signals are period modulated are very attractive because they can directly be interfaced to a microcontroller. Such interfaces can easily be implemented with a simple relaxation oscillator [1] and applied to capacitive sensors [2]. Reference [2] reported a resolution of better than 10^{-4} for a measurement range of 1 pF with a measurement time of 100 ms. Such a measurement time can be acceptable for measurement systems with slow-changing physical signals. However, in some applications, this measurement time can be too long. Normally, there is a tradeoff between the measurement time and the resolution, so a shorter measurement time implies a worse resolution. To maintain the resolution while reducing the measuring time, we should improve the noise performance of the sensor interface.

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In order to achieve a high resolution ($<10^{-4}$–10^{-5}) with a short measuring time ($<1-10$ ms), we investigated the noise performance of a common type of interface, with a period-modulated output signal. In such interfaces, noise is contributed both by the relaxation oscillator and by the counter which counts the period of the output signal. The contributions for the different noise sources in the relaxation oscillator have been analyzed to determine criteria for implementing a low-noise (high-resolution) sensor interface. In a previous work, a similar analysis was performed for an oscillator implemented as an integrated circuit [3]. In this paper, we consider the application of commercially available ICs (op-amps and comparators) to implement the oscillator. The flexibility in replacing the applied components by other ones with different performance has allowed us to perform a wide range of experiments to verify the theoretical analysis. As a counter, we could use the internal counters of a general purpose microcontroller. However, most of the commercial low-cost microcontrollers can be driven with clock frequencies only up to 20 MHz, with their internal counters normally working at an even lower frequency. In this paper, it is proposed to use an additional counter working at a higher frequency in order to reduce the quantization noise, caused by digitizing the period-modulated output signal.

Regarding the overall accuracy of capacitive systems, the reduction of systematic error sources and the sensitivity to electromagnetic interference (EMI) also have to be considered. Many advanced measurement techniques to achieve this could be discussed, including the application of three-signal autocalibration [1] and advanced techniques for chopping and synchronous detection. However, in this paper, we will mainly limit our attention to the noise performance of the sensor interface. The resulting interface system will be applied in a contactless capacitive angular position sensor [4] and in the feedback loop of an active magnetic-bearing positioner.

II. Interface System

A. Relaxation Oscillator

Fig. 1 shows the schematic circuit of the first-order relaxation oscillator [1], [2], which is the core of the capacitive interface. The oscillator is implemented with an operational amplifier (op-amp), a comparator (comp), two digital inverters, the capacitances $C_{\rm off}$ and $C_{\rm int}$, and a controlled current source $I_{\rm int}$, which value depends on the resistor $R_{\rm int}$. The performance of the oscillator is described elsewhere [3], [5]. The capacitor $C_{\rm x}$ represents the capacitance of the sensor to be measured and $C_{\rm p1}$

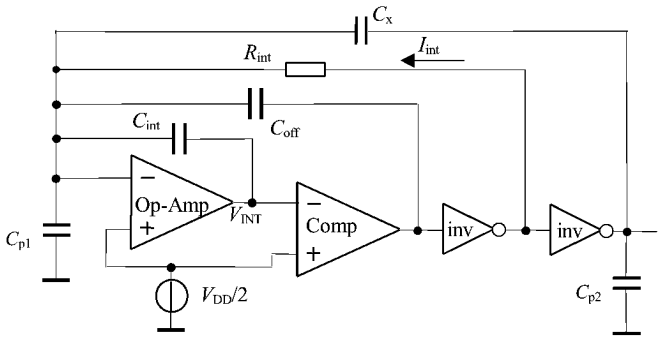

Fig. 1. First-order relaxation oscillator.

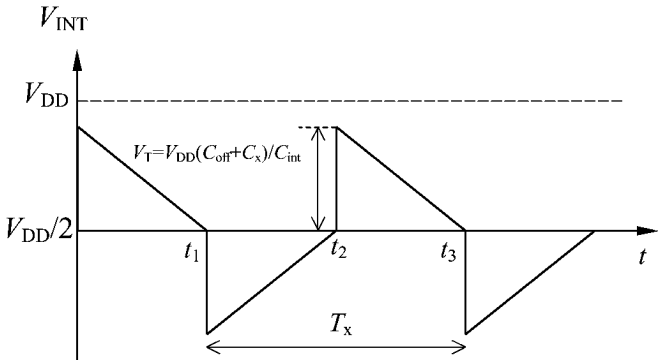

Fig. 2. Voltage at the output of the op-amp.

and C_{p2} model the parasitic capacitances to ground due to, for example, the connected cables. Fig. 2 shows the voltage at the output of the op-amp. When this voltage crosses the threshold level $V_{\mathrm{DD}}/2$, the output of the comparator and the inverters switch, and the charge is transferred from capacitors C_{x} and C_{off} to C_{int}, generating a step voltage at the op-amp output. Next, the current I_{int} removes the charge stored at C_{int} until the op-amp output reaches the threshold level again. The period of the oscillator output signal is given by

$$T_x = 4R_{\mathrm{int}}(C_{\mathrm{off}} + C_{\mathrm{x}}). \tag{1}$$

Some parameters are fixed: the sensor itself determines C_{x}, and C_{off} is normally chosen to be around the maximum value of C_{x}; the value of C_{int} must be at least $2(C_{\mathrm{off}} + C_{\mathrm{x}})$ in order to avoid saturation of the op-amp output (considering a rail-to-rail output op-amp); the supply voltage is determined by the application itself. So, the period, T_{x}, of the output signal can be controlled by the value of R_{int}, i.e., the value of the integration current I_{int}.

B. Complete Interface

The capacitive–sensor interface is mainly composed of a relaxation oscillator, a multiplexer, a fast counter, and a microcontroller (Fig. 3). The relaxation oscillator converts the capacitance values of the sensing element to a period-modulated output. The counter measures the elapsed time of N periods. The multiplexer selects the measured capacitance. The microcontroller controls the external counter and multiplexer, reads the data, and transmits them via a RS232 interface to a PC.

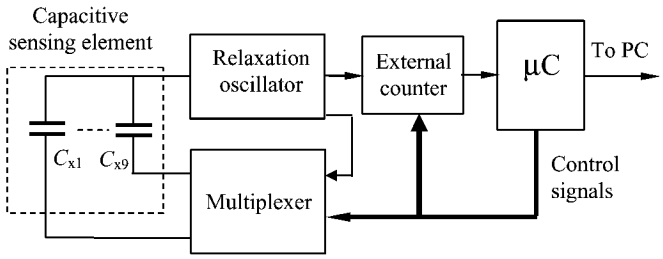

Fig. 3. Functional block diagram of the capacitive–sensor interface.

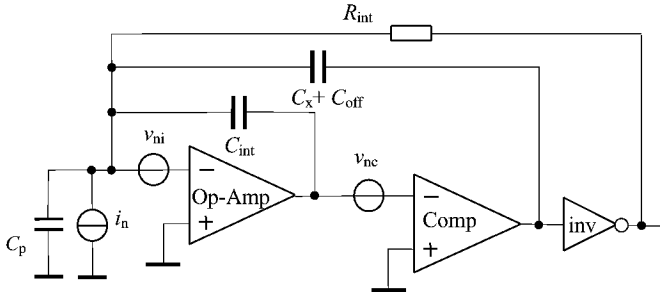

Fig. 4. Relaxation oscillator with the main noise sources.

To measure the period of the square-wave signal at the oscillator output, a constant pulse counting (CPC) method [6] is used. In the CPC method, we count the elapsed time, T_e, for N periods of the output signal of the relaxation oscillator. So,

$$T_{\mathrm{e}} = NT_{\mathrm{x}}. \tag{2}$$

The counter measures this elapsed time by counting clock pulses with a counting frequency of 50 MHz (20 ns). The measured times for the capacitances C_{off} and the external capacitances C_{x1} to C_{x9} are sent to the PC.

III. Noise Analysis

The noise performance of the oscillator is investigated using the circuit schematic of Fig. 4 in which the main noise sources have been indicated.

The considered noise sources are as follows:

— the input noise voltage v_{ni} of the op-amp;
— the input noise current i_{n} of the op-amp;
— the input noise voltage v_{nc} of the comparator.

As compared to the other noise sources, the noise due to the resistor is negligible in all the experiments carried out in Section IV. Furthermore, the input noise current of the comparator has no influence. Therefore, these noise sources have not been included into the model. In the analysis, we will assume that all of the noise sources have a flat-band (white noise) spectrum and are uncorrelated with the output signal of the comparator.

White noise can be described as the sum of an infinite number of sinusoidal components having equal amplitudes, differing frequencies, and a random phase. The influence of the noise in the circuit will be first calculated by evaluating the influence of a single sinusoidal noise component. In this way, a transfer function will be obtained and used, together with the power spectral density (PSD) of the input noise, to calculate the influence of the overall noise on the period of the output signal.

A. Noise Voltage Analysis

First, the effect of $v_{\rm ni}$ and $v_{\rm nc}$ is analyzed. The normalized one-period time error of the output signal is defined as

$$\varsigma = \frac{\Delta T_{\rm x}}{T_{\rm x}}. \tag{3}$$

According to the analysis described in the Appendix, the magnitude of the transfer function given by (A.6), $|H_v(\mathrm{j}f)|$, relates (3) with the (sinusoidal) components of the noise voltage at the input of the comparator, $v_{\rm n}$. The standard deviation of (3), σ_ς, which we will refer in this paper as the jitter of the oscillator, is given by

$$\sigma_\varsigma(v_{\rm n}) = \sqrt{\int_0^{B_{\rm eq}} |H_v(\mathrm{j}f)|^2 S_v(f)\mathrm{d}f} \tag{4}$$

where $B_{\rm eq}$ is the equivalent bandwidth of the system (for simplicity, we assume an ideal brick-wall low-pass frequency response) and $S_v(f)$ is the PSD of the noise voltage at the input of the comparator. Considering $B_{\rm eq} \gg f_x(=1/T_{\rm x})$, a condition that has to be satisfied to assure a low nonlinearity [3], [5], and a flat frequency spectrum of the noise, (4) can be approximated as

$$\sigma_\varsigma(v_{\rm n}) = \frac{C_{\rm int}}{V_{\rm DD}(C_{\rm off}+C_{\rm x})}\sqrt{\frac{3}{2}S_v B_{\rm eq}}. \tag{5}$$

When the corner frequency of $S_{\rm v}$ is much lower than $f_{\rm x}$, the contribution of the $1/f$ noise is negligible. Using (5) the jitter due to the voltage noise source $v_{\rm nc}$ of the comparator can be expressed as

$$\sigma_\varsigma(v_{\rm nc}) = \frac{C_{\rm int}}{V_{\rm DD}(C_{\rm off}+C_{\rm x})}\sqrt{\frac{3}{2}S_{\rm vc} B_{\rm comp}} \tag{6}$$

where $S_{\rm vc}$ is the PSD of $v_{\rm nc}$, and $B_{\rm comp}$ is the "unity-gain bandwidth" of the comparator.

For the noise voltage $v_{\rm ni}$ of the amplifier, its equivalent PSD at the input of the comparator is given by

$$S_v = S_{\rm vi}\left(\frac{C_{\rm total}}{C_{\rm int}}\right)^2 \tag{7}$$

where $S_{\rm vi}$ is the PSD of $v_{\rm ni}$ and $C_{\rm total} = C_{\rm off}+C_{\rm x}+C_{\rm int}+C_{\rm p}$. Defining $B_{\rm amp}$ as

$$B_{\rm amp} = f_{\rm T}\frac{C_{\rm int}}{C_{\rm total}} \tag{8}$$

where $f_{\rm T}$ is the unity-gain bandwidth of the op-amp, and using (5), the jitter due to $v_{\rm ni}$ can be expressed as

$$\sigma_\varsigma(v_{\rm ni}) = \frac{C_{\rm total}}{V_{\rm DD}(C_{\rm off}+C_{\rm x})}\sqrt{\frac{3}{2}S_{\rm vi} B_{\rm eq\,min}} \tag{9}$$

where $B_{\rm eq\,min}$ is the lowest value of $B_{\rm comp}$ and $B_{\rm amp}$. When $B_{\rm amp} < B_{\rm comp}$, the jitter can be expressed as

$$\sigma_\varsigma(v_{\rm ni}) = \frac{1}{V_{\rm DD}(C_{\rm off}+C_{\rm x})}\sqrt{\frac{3}{2}S_{\rm vi} f_{\rm T} C_{\rm int} C_{\rm total}}. \tag{10}$$

Keeping the parasitic capacitance $C_{\rm p}$, and then $C_{\rm total}$, at a minimum will reduce the jitter. On the other hand, if $C_{\rm p} \gg C_{\rm int}$, the jitter will increase with the square root of $C_{\rm p}$.

B. Noise Current Analysis

Similarly to the analysis developed in the Appendix for the effects of the noise voltage, a transfer function can be found that relates (3) with the (sinusoidal) components of the noise current. The magnitude of this transfer function is given by [7]

$$|H_i(\mathrm{j}f)| = \frac{\sin^2\left(\frac{\pi f}{2f_{\rm x}}\right)}{V_{\rm DD}(C_{\rm off}+C_{\rm x})\pi f} \tag{11}$$

where the frequency f in the denominator accounts for the integration of the current by the circuit. The jitter due to the current noise is given by

$$\sigma_\varsigma(i_{\rm n}) = \sqrt{\int_0^{B_{\rm eq}} |H_i(\mathrm{j}f)|^2 S_i(f)\mathrm{d}f} \tag{12}$$

where $S_{\rm i}(f)$ is the PSD of $i_{\rm n}$. Considering white noise and $B_{\rm eq} \gg f_{\rm x}$, the jitter due to the input noise current $i_{\rm n}$ of the amplifier can be approximated as

$$\sigma_\varsigma(i_n) = \frac{1}{V_{\rm DD}}\sqrt{\frac{S_i R_{\rm int}}{2(C_{\rm off}+C_{\rm x})}}. \tag{13}$$

In this case, the bandwidth of the comparator and the op-amp do not contribute to the jitter.

C. Final Jitter

The jitter for N periods of the oscillator output is given by

$$\sigma_\varsigma = \frac{\sigma_{\Delta(NT_{\rm x})}}{NT_{\rm x}} = \frac{\sigma_{\Delta T_{\rm e}}}{T_{\rm e}}. \tag{14}$$

After some extensive calculations, it can be found that

$$\sigma_\varsigma(v_{\rm n}) = \frac{C_{\rm int}}{V_{\rm DD}(C_{\rm off}+C_{\rm x})}\sqrt{\frac{(3/2+2(N-1))}{N^2}S_v B_{\rm eq}} \tag{15}$$

$$\sigma_\varsigma(i_{\rm n}) = \frac{1}{V_{\rm DD}}\sqrt{\frac{S_i R_{\rm int}}{2N(C_{\rm off}+C_{\rm x})}} = \frac{1}{2V_{\rm DD}(C_{\rm off}+C_{\rm x})}\sqrt{\frac{S_i}{2Nf_{\rm x}}}. \tag{16}$$

When $N \gg 1$, (15) can be rewritten as

$$\sigma_\varsigma(v_{\rm n}) = \frac{C_{\rm int}}{V_{\rm DD}(C_{\rm off}+C_{\rm x})}\sqrt{\frac{2}{N}S_v B_{\rm eq}}. \tag{17}$$

As can be seen, the jitter given by (16) and (17) decreases with the square root of the measured period number N. The jitter due to the voltage noise (comparator and amplifier) is independent of the frequency of the oscillator. The jitter due to the current noise of the amplifier decreases with an increasing value of $f_{\rm x}$. However, when the oscillator frequency $f_{\rm x}$ is too high, approaching to $B_{\rm amp}$, the nonlinearity of the conversion from the capacitance to the period of the oscillator will increase [3], [5]. By choosing $f_{\rm x} < B_{\rm amp}/4$, we assure that the nonlinearity due to this high-frequency influence is less than 10^{-5}. The use of a low-noise comparator and a low-noise op-amp will reduce the jitter. Bipolar op-amps have a low-noise voltage but a high-noise current. On the other hand, JFET-input and complimentary metal–oxide–semiconductor (CMOS) op-amps have a higher noise voltage but a negligible noise current. So, there will be a tradeoff in choosing an appropriate op-amp.

When a time period is digitized with a counter, quantization noise will be intruded. The magnitude of the quantization noise depends on the digitized time period $T_{\rm e}$. In the worst-case, when $T_{\rm e} = (k + 0.5)t_{\rm s}$, where $t_{\rm s}$ is the sampling time of the counter and k is an integer, the jitter due to the quantization noise of the counter amounts to

$$\sigma_{\varsigma}(t_{\rm s}) = \frac{t_{\rm s}/2}{T_{\rm e}} = \frac{t_{\rm s}/2}{NT_{\rm x}}. \tag{18}$$

The quantization noise is inversely proportional to measured period number N. In the best case, when $T_{\rm e} = kt_{\rm s}, \sigma_{\zeta}(t_{\rm s}) = 0$. As all the noise sources are uncorrelated, we obtain the final jitter by calculating the root of the sum-of-squares of the different noise sources

$$\sigma_{\varsigma} = \sqrt{\sigma_{\varsigma}^2(v_{\rm ni}) + \sigma_{\varsigma}^2(v_{\rm nc}) + \sigma_{\varsigma}^2(i_{\rm n}) + \sigma_{\rm q}^2(t_{\rm s})}. \tag{19}$$

IV. Experimental Results

The capacitive-sensor interface has been applied in a contactless capacitive angular-position sensor [4] and in the feedback loop of an active magnetic-bearing positioner. In these applications, the capacitance values were lower than 3 pF. For the magnetic-bearing positioner application, a measurement time of less than 1 ms and a resolution of 10^{-4} were required in order to guarantee the stability of the closed loop and the accuracy of the positioner.

In the first step, only the noise performance of the relaxation oscillator (Fig. 1) was investigated. The time interval for different number of periods (N) was measured using a universal counter instrument 53132A (Agilent), which has a resolution of 300 ps. With this setup, the contribution of the quantization noise to the measured jitter was negligible. The measurement results were sent to a PC via a general purpose interface bus (GPIB) bus.

The relaxation oscillator was implemented with $C_{\rm off} = 1.8$ pF and $C_{\rm int} = 10$ pF, allowing a measurement range for the external capacitances of 3.2 pF (using a rail-to-rail op-amp). This range was sufficient for the intended applications. In this first step, no external capacitance $C_{\rm x}$ was used. The (single) supply voltage was fixed to 5 V. In order to investigate the noise effects of the used components, different types of amplifiers and comparators with different noise performances and bandwidths were used. As representatives for two different types of op-amps, we selected an OPA2350 and an MAX412. The OPA2350 is a rail-to-rail CMOS amplifier with a low bias current, whereas the MAX412 is a low-voltage-noise bipolar jucntion transistor (BJT) device. For the comparator, two different devices, an MAX942 and an OPA2132 were selected. The first one is a high-speed BJT comparator, whereas the second one is a junction field-effect transistor (JFET)-input amplifier with a low transition time. Table I lists the unity-gain-bandwidth and the input noise voltage and current of the OPA2350, MAX412, and OPA2132. These specifications are not listed for the MAX942 because, as usual for comparators, the manufacturer only provides the information about the delay time. However, we can expect that it will have a wide "bandwidth."

TABLE I
Significative Parameters for the Applied Amplifiers

	OPA2350 (CMOS)	MAX412 (BJT)	OPA2132 (JFET-input)
$f_{\rm t}$	38 MHz	28 MHz	8 MHz
$v_{\rm n}$	5 nV/$\sqrt{\rm Hz}$	1.8 nV/$\sqrt{\rm Hz}$	8 nV/$\sqrt{\rm Hz}$
$i_{\rm n}$	4 fA/$\sqrt{\rm Hz}$	1.2 pA/$\sqrt{\rm Hz}$	3 fA/$\sqrt{\rm Hz}$

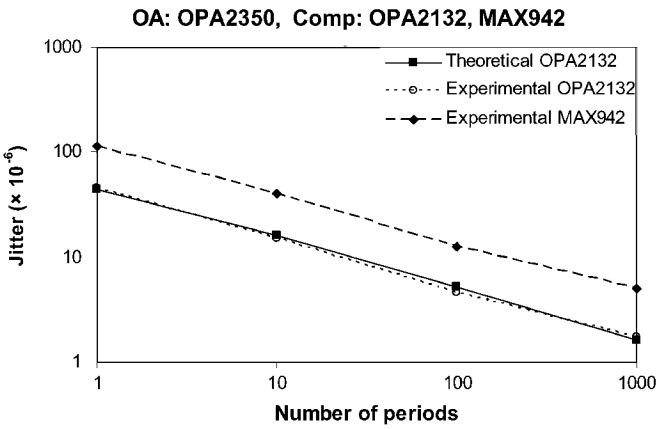

Fig. 5. Jitter using an OPA2350 as the op-amp and an OPA2132 and an MAX942 as comparators. The interval time was measured a universal counter instrument.

The relaxation oscillator was tested with a parasitic input capacitance up to 400 pF ($C_{\rm p1}$ in Fig. 1). In this case, when using a MAX412 as op-amp, $B_{\rm amp}$ amounts to 0.7 MHz. In order to reduce nonlinear effects by accomplishing the relation $f_x < B_{\rm int}/4$, we chose $R_{\rm int} = 1.2$ MΩ. Then, with $C_{\rm x} = 0$, $f_{\rm x}$ has a value of 116 kHz.

Fig. 5 shows the jitter results when using an OPA2350 as op-amp, and an OPA2132 and an MAX942 as comparators. In case of using an OPA2132 as comparator, the experimental and theoretical results agreed with each other. For the theoretical calculations, we assumed that there is a residual parasitic capacitance with a value of 5 pF. In this case, the main jitter contribution was due to the noise voltages of the op-amp and the comparator, and the noise current of the op-amp had a negligible contribution. Then, as predicted by (17), the jitter decreased inversely proportional with the square root of N. For $N = 1000$ (measuring time of 8.6 ms), the jitter amounted to 1.7×10^{-6}.

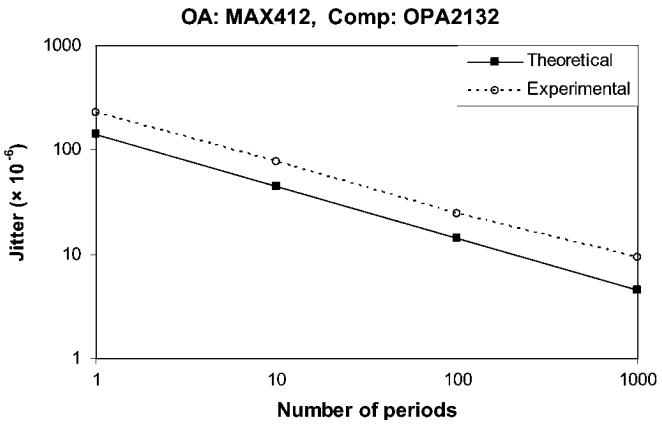

Fig. 6. Jitter using an MAX412 as the op-amp and an OPA2132 as the comparator. The interval time was measured a universal counter instrument.

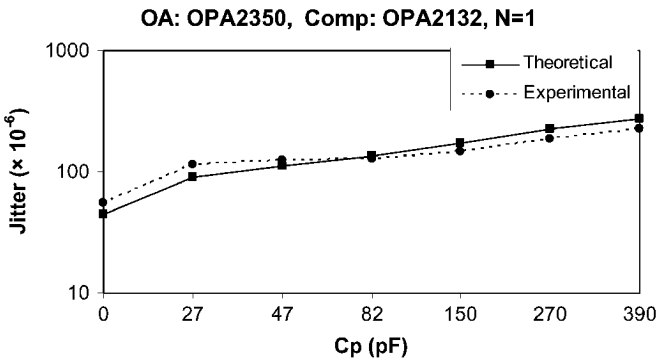

Fig. 7. Jitter using an OPA2350 as the op-amp and an OPA2132 as the comparator, for $N = 1$ and different values of $C_{\rm p}$. The interval time was measured by a universal counter instrument.

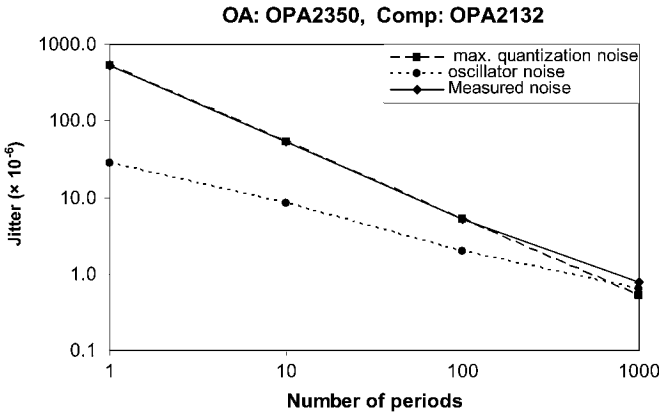

Fig. 8. Jitter using an OPA2350 as the op-amp and a OPA2132 as the comparator. The interval time was measured using the circuit of Fig. 3.

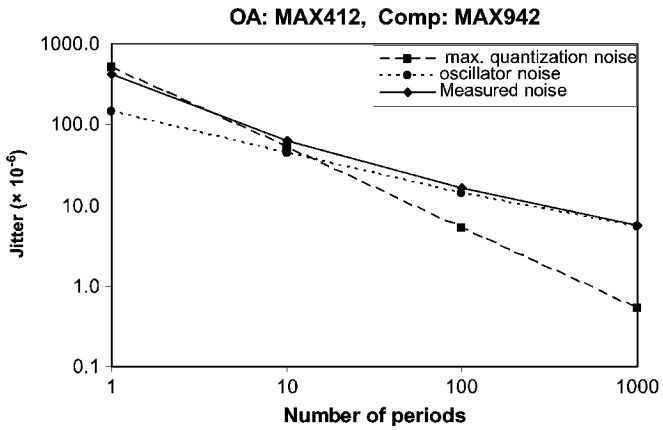

Fig. 9. Jitter using an MAX412 as the op-amp and an MAX942 as the comparator. The interval time is measured using the circuit of Fig. 3.

When using an MAX942 as comparator a larger (more than twice) amount of jitter was observed. Probably, this could be due to the larger "bandwidth" or the different noise level of the comparator MAX942 as compared to the OPA2132. Due to the lack of data about the input noise and bandwidth of the comparator MAX942, there is not a theoretical prediction.

Fig. 6 shows the results of the jitter when using a BJT amplifier MAX412 as op-amp and an OPA2132 as comparator. Here, there was a slight difference between the theoretical and experimental results. This could be due to a difference of the actual noise current with respect to the typical value provided by the manufacturer. In this case, the jitter was mainly contributed by the noise current of the op-amp. This jitter was four times larger than that when using an OPA2350 for the op-amp. Therefore, in order to reduce the jitter of the oscillator, a CMOS op-amp is more suitable than a BJT op-amp. The jitter was also measured by using an MAX412 as op-amp and an MAX942 as comparator. The results (not shown) were similar to those shown in Fig. 6, confirming that the input noise voltage and the bandwidth of the comparator have no influence when the predominant source is the noise current of the op-amp, as predicted by (16).

Fig. 7 shows the effect of the parasitic capacitance $C_{\rm p}$ on the jitter. In this measurement, we applied the "best" choice using an OPA2350 as op-amp and an OPA2132 as comparator. For $N = 1$, as predicted by (10), the jitter increased with an increasing value of $C_{\rm p}$.

To evaluate the effect of the quantization noise due to the counter, in the second step, a complete capacitive-sensor interface according to the functional block diagram of Fig. 3 was implemented, using a 74HC4040 counter with a 50-MHz clock (sampling time of 20 ns) and a PIC16F876 microcontroller (Microchip) with a clock frequency of 20 MHz. For the oscillator (Fig. 1), we used $R_{\rm int} = 1.2\ {\rm M}\Omega, C_{\rm off} = 1.8$ pF, and $C_{\rm x} = 2.2$ pF, which results in $T_{\rm x} = 19.2\ \mu$s ($f_{\rm x} = 52$ kHz).

Fig. 8 shows the jitter results when using an OPA2350 as op-amp and an OPA2132 as comparator. The quantization noise predominated up to $N = 1000$ (measurement time of 19.2 ms). At this point, the total jitter amounted to 7.8×10^{-7}. With (1), it can be calculated that the interface can measure $C_{\rm x}$ with a resolution of 14.2×10^{-7}. With $N = 10$ (measurement time of 192 μs), the resolution was better than 10^{-4}, thus accomplishing the requirements for the magnetic-bearing positioner application. Replacing the comparator by a MAX942 increased the noise of the oscillator resulting in a total jitter of 2.1×10^{-6} for $N = 1000$. In this case, the quantization noise predominated up to $N = 100$. Fig. 9 shows the resulting jitter when using a MAX412 as op-amp and an MAX942 as comparator. In this case, the total jitter for $N = 1000$ increased to 5.7×10^{-6},

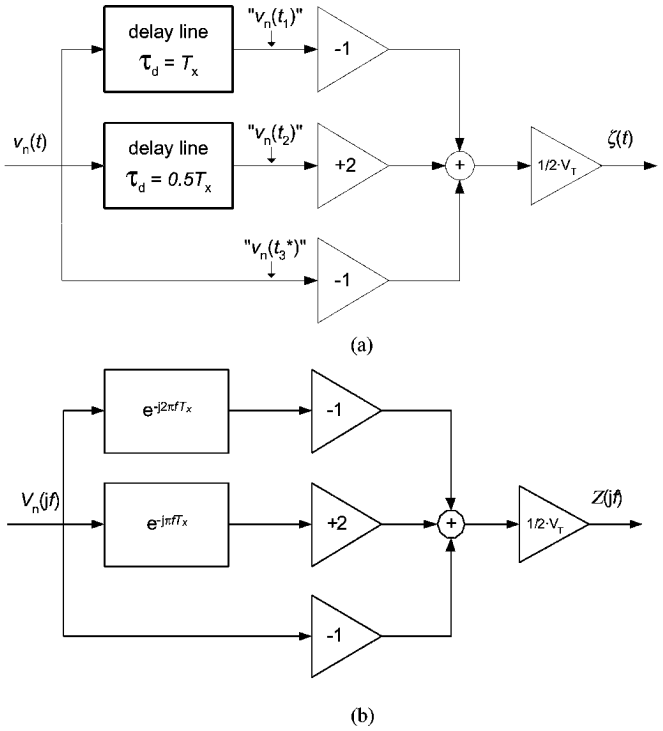

Fig. 10. (a) Time-domain filter model that relates $v_{\rm n}(t)$ with $\zeta(t)$. (b) S-domain filter model that relates $V_{\rm n}(\mathrm{j}f)$ with $Z(\mathrm{j}f)$.

and the quantization noise predominated up to $N = 10$. Similar results to those shown in Fig. 9 were obtained when replacing the comparator MAX942 by an OPA2132.

V. Conclusion

A high-speed capacitive-sensor interface, implemented with a simple relaxation oscillator, a fast counter, and a microcontroller, has been presented. The interface is able to measure low-capacitance values in the order of several picoFarads with a high resolution and has been applied in a contactless capacitive angular-position sensor and in the feedback loop of an active magnetic-bearing positioner. The noise performance of the relaxation oscillator has theoretically been analyzed, and guidelines for implementing a low-noise oscillator have been pointed out. The theoretical predictions have been verified by experimental measurements using different types of amplifiers and comparators. It has been shown that to achieve a low jitter, a CMOS op-amp with a low input-noise voltage and a relatively narrow bandwidth has to be applied, together with a low-noise comparator. Meanwhile, the parasitic capacitance at the input of the op-amp should be kept at a minimum. As to be expected, the jitter appears to be inversely proportional to the square root of the measurement time. A prototype of a complete setup implemented with a microcontroller and a high-speed (50-MHz) counter has also been tested. For the best combination of op-amp and comparator, a resolution of 14.2×10^{-7} has been obtained for a measuring time of 19.2 ms and an external capacitance value of 2.2 pF. For a measuring time of 192 μs, a resolution better than 10^{-4} has been obtained, thus accomplishing the requirements of the magnetic-bearing positioner application.

Appendix

Fig. 2 shows the output signal of the op-amp. The voltage and current noise sources described in Section III will affect the position of the switching times t_1, t_2, and t_3 in Fig. 2 and then the value of $T_{\rm x}$. We define the variation $T_{\rm x}$ due to the various noise sources as

$$\Delta T_{\rm x} = t_{\rm n1} + t_{\rm n2} \tag{A.1}$$

where

$$t_{\rm n1} \approx \frac{v_{\rm n}(t_2^*) - v_n(t_1^*)}{\alpha} \tag{A.2}$$

$$t_{\rm n2} \approx \frac{v_{\rm n}(t_2^*) - v_{\rm n}(t_3^*)}{\alpha}. \tag{A.3}$$

The instants t_1^*, t_2^*, and t_3^* correspond to the switching times in a noise-free oscillator. In (A.2) and (A.3), we assume that the noise voltage at the actual switching time $v(t_{\rm n})$ and at the fictitious noise-free transition $v(t_{\rm n}*)$ are approximately equal [7]. The factor α represents the absolute value of the slope of the integrating voltage versus the time

$$\alpha = |\Delta V/\Delta t| = \frac{2V_{\rm T}}{T_{\rm x}} = \frac{2V_{\rm DD}(C_{\rm off} + C_{\rm x})}{T_{\rm x}C_{\rm int}}. \tag{A.4}$$

Substituting (A.2) to (A.4) in (3), we obtain

$$\varsigma = \frac{\Delta T_{\rm x}}{T_{\rm x}} = \frac{t_{\rm n1} + t_{\rm n2}}{T_{\rm x}} = \frac{[2v_{\rm n}(t_2^*) - v_{\rm n}(t_1^*) - v_{\rm n}(t_3^*)]C_{\rm int}}{2V_{\rm DD}(C_{\rm off} + C_{\rm x})}. \tag{A.5}$$

Following the analysis in [7], (A.5) can be seen as a combination of *noise samples at different moments*. Suppose that the t_3^* is the moment "now." Then, t_2^* is a moment $T_{\rm x}/2$ ago, and t_1^* is a moment $T_{\rm x}$ ago. We can "shift" $v_{\rm n}(t_2^*)$ and $v_{\rm n}(t_1^*)$ in time by using two delay lines. Fig. 10 depicts a time-domain filter model for (A.5) and its frequency-domain filter model. In Fig. 10(b), the input $V_{\rm n}(\mathrm{j}f)$ represents one sinusoidal component of the input noise. Because signal phase is not considered in noise analysis, only the magnitude of the frequency response of the filter is evaluated. That is given by

$$\begin{aligned} |H_v(\mathrm{j}f)| &= \frac{|-e^{-\mathrm{j}2\pi fT_{\rm x}} + 2e^{-\mathrm{j}\pi fT_{\rm x}} - 1|}{2V_{\rm DD}(C_{\rm off} + C_{\rm x})} C_{\rm int} \\ &= \frac{2C_{\rm int}}{V_{\rm DD}(C_{\rm off} + C_{\rm x})} \sin^2\left(\frac{\pi f}{2f_{\rm x}}\right) \end{aligned} \tag{A.6}$$

where $f_{\rm x} = 1/T_{\rm x}$. As can be derived from (A.6), the influence of the uncorrelated voltage-noise source on the period of the oscillation is maximal for frequencies at the odd multiples of $f_{\rm x}$ and minimal (zero) for frequencies at the even multiples of $f_{\rm x}$.

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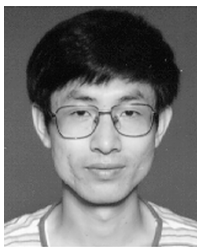

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