

The OPAL silicon microvertex detector

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Received 23 July 1992

A silicon strip microvertex detector has been designed, constructed and commissioned in the OPAL experiment at the LEP electron-positron collider. The microstrip devices incorporate a new FoxFET biasing scheme developed together with Micron Semiconductor Ltd., UK. The devices digitise with a precision close to 5 μm and have an exceptionally high signal-to-noise ratio. The associated microelectronics were all custom made for the OPAL project. The detector began operation in 1991 and has since continued to be part of the OPAL experiment, performing to a very high standard and opening up new areas of physics studies.

1. Introduction

In 1990 a proposal was approved to equip the OPAL experiment at LEP with two cylindrical layers of silicon microstrip devices, to be positioned around a reduced diameter beam pipe at the centre of the existing OPAL drift chamber assembly.

The proposed system, having been through the phases of prototyping, detailed integral design, manufacture and installation within the OPAL experiment, was successfully commissioned for physics data in May 1991. The microstrip devices were developed within the OPAL Microvertex Group [1] and have single-sided capacitively-coupled readout of the azimuthal $r-\phi$ coordinate at known radii^{#1}.

^{#1} The coordinate system is cylindrical, with z -axis along the e^- beam direction.

The components of the OPAL central tracking in $r-\phi$ are now [2]:

- A jet drift chamber, giving $\sigma(r\phi) \sim 135 \mu\text{m}$ from 159 sense-wires at radii between 0.25 and 1.85 m.
- A vertex drift chamber, giving $\sigma(r\phi) \sim 55 \mu\text{m}$ from 12 wires at radii between 0.10 and 0.16 m.
- Two layers of silicon microstrip detectors with intrinsic $\sigma(r\phi) \sim 5 \mu\text{m}$. The detectors are tangential to cylindrical surfaces at radii of 0.061 and 0.075 m, as illustrated in fig. 1.

The increased single coordinate precision of the silicon devices together with an intrinsic two-track resolution of better than 150 μm make a significant improvement to the capabilities of the central tracking of the experiment. Efficiency of track reconstruction within jets is improved, as is the ability to reconstruct distinct secondary vertices on an event-by-event basis for hadrons containing heavy quarks which may travel up to millimetres before decaying. As a result such

processes can be tagged more readily and their detailed physics studied more effectively. In addition, particle lifetimes in the region of 10^{-13} s can be measured much more precisely.

In this paper details of the new silicon FoxFET detectors are given in section 2, and their geometrical

and electrical configurations are described in section 3. Details of the associated electronics are in section 4, while in section 5 the techniques and online software algorithms for recording the data from the detectors are described. Section 6 deals with the powering of the devices and all aspects of control and monitoring of the

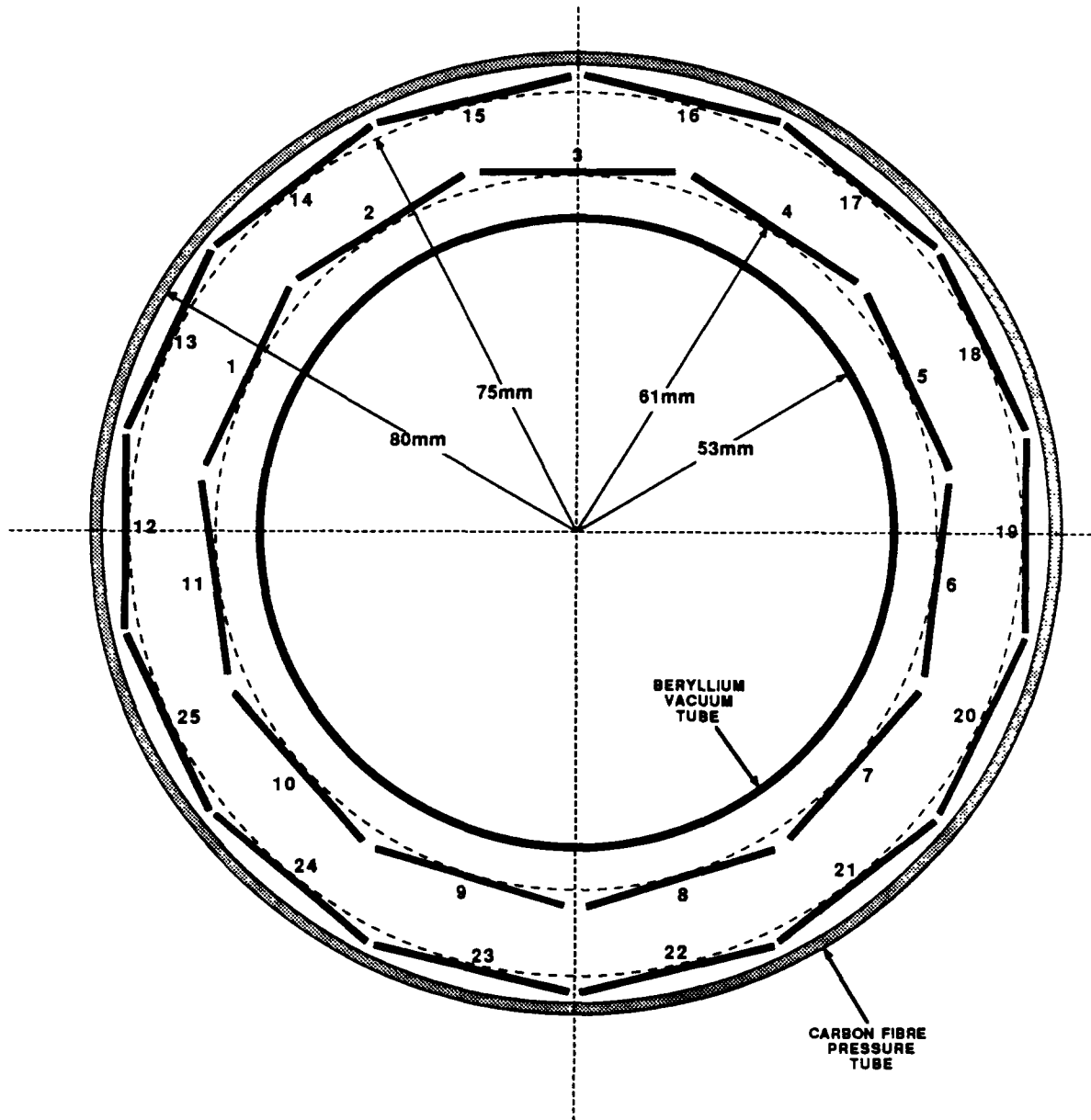


Fig. 1. The layout of the silicon microstrip devices in the $r\phi$ plane. The inner and outer layers contain, respectively, 11 and 14 devices, and are positioned between a beryllium vacuum tube, 1.1 mm thick, and an outer carbon fibre pressure tube, 2 mm thick.

cooling system, temperatures and absorbed radiation. The offline reconstruction of data is outlined in section 7 and the current performance of the system within OPAL is discussed in section 8.

2. The silicon microstrip detectors

The silicon wafers of the microstrip detector were designed and developed in the UK in collaboration with Micron Semiconductor Ltd. [3]. These capacitively-coupled ‘‘FoxFET’’ detectors make use of a novel biasing technique for the implanted strips, described in detail in ref. [1], where test results and probe-station measurements are also reported. The use of a field effect transistor with the gate over the field oxide provides simplicity of fabrication while allowing the dynamic bias resistance to be tuned through the gate voltage control. As shown in fig. 2, the gate overlaps both the ends of the strips (the FET source) and the low-bias rail (the FET drain). Detectors are typically operated with a gate–drain voltage of about -15 V, corresponding to a dynamic resistance of at least 10 M Ω , and a drain voltage of 3.6 V. These values were chosen to match the characteristics of the charge-

amplifier chips used for readout (section 4.1), and have resulted in excellent signal-to-noise performance within OPAL.

The detectors are single-sided devices with 25 μm strip pitch, fabricated on 300 μm thick, high-resistivity (5 – 10 k Ω cm) silicon wafers, which are fully depleted below 35 V. Every second strip has an aluminium readout strip above the 170 nm thin oxide insulation (fig. 2) which has the full length of the implanted strip and gives 16 pF/cm capacitive coupling. The total detector interstrip capacitance is about 1.6 pF/cm. Each detector is 33 mm wide and 60 mm long and has 629 readout strips and twice this number of p^+ implant strips. Measurements tracking a 950 nm wavelength, 15 μm wide light spot across a detector in 1 μm steps showed that the intermediate strips work as expected to linearise the charge division [1].

The wafers are passivated with a silox coating and kept in a nitrogen atmosphere in the experiment. The total leakage current per detector (all strips plus guard line) is low, typically well below 1 μA . These currents rise to stable values within a few minutes and all detector parameters have shown great stability in the experiment. The typical single hit efficiency of a 60 mm long bonded wafer is about 99% , and test beam mea-

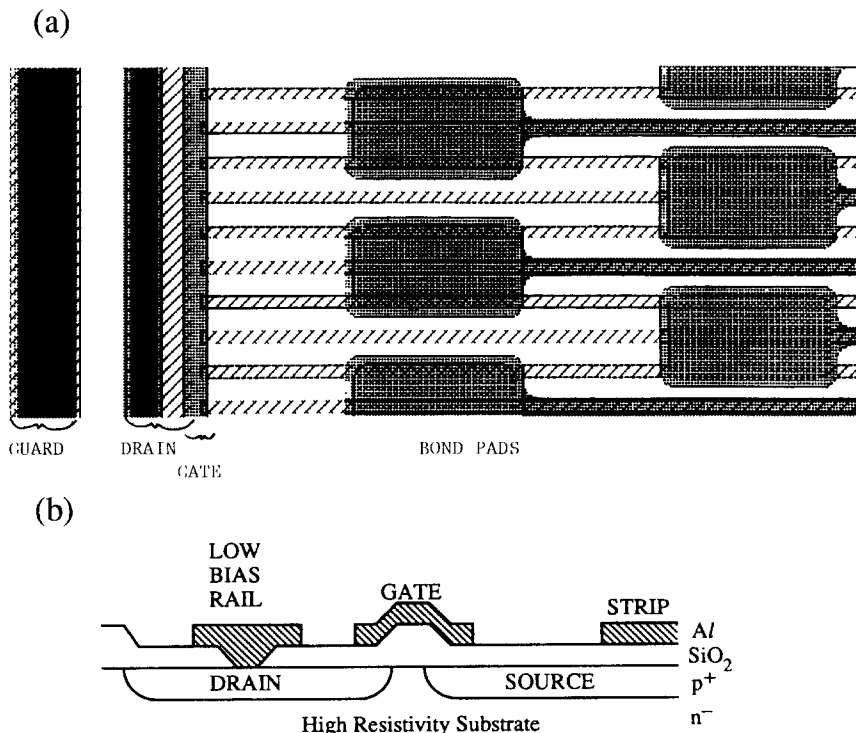


Fig. 2. (a) A FoxFET microstrip device, showing the readout strips with their bond pads, at 50 μm intervals, interleaved with further p^+ implants used to linearise charge division. The dynamic bias control of the p^+ implants is provided by the gate–drain potential difference of the FoxFET. (b) Cross section of the detector bias structure.

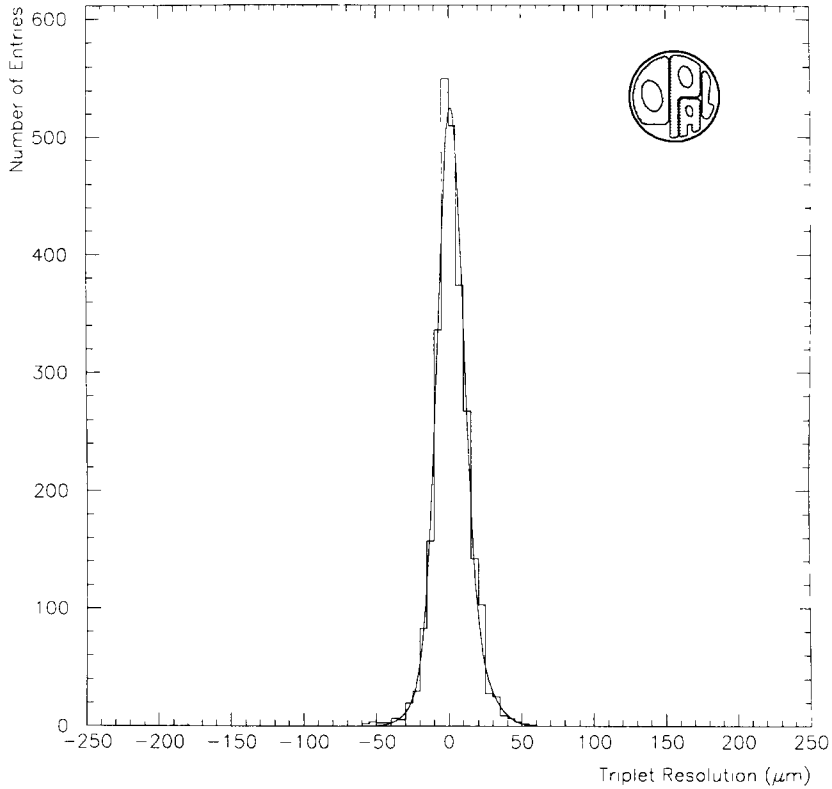
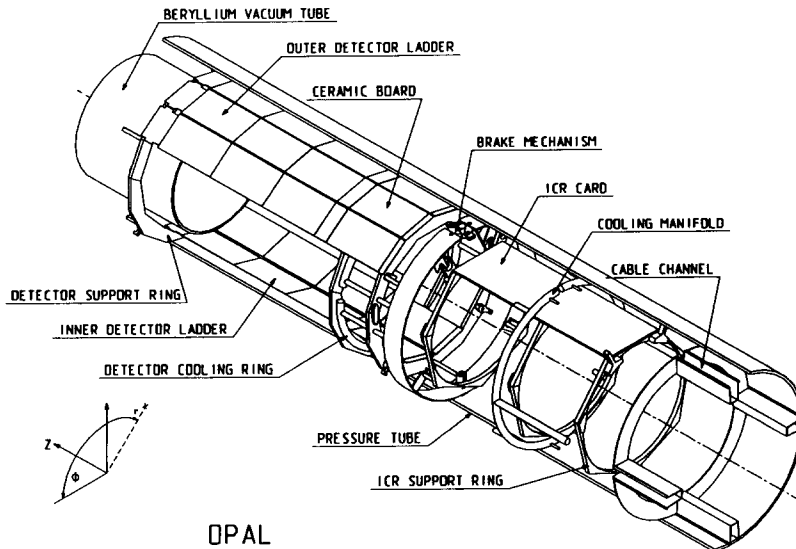


Fig. 3. The measured precision of an OPAL ladder placed at the centre of a triplet of detectors in a 5 GeV pion test beam. The fitted curve corresponds to a ladder resolution of 6 μm .

measurements at CERN have demonstrated that an intrinsic resolution of better than 6 μm is readily achieved. This is illustrated in fig. 3, which shows the resolution

measured with three detectors placed about 10 mm apart in a 5 GeV pion beam.

Radiation tests at 5 Gy/h for 100 h using a ^{90}Sr



OPAL

Fig. 4. An illustration of the OPAL silicon microvertex detector, showing some of the 25 detector ladders, the support and cooling structures and part of the Interconnect Ring (ICR) assembly and the emerging cable channels.

source showed no discernible changes in the characteristics of the FoxFET biasing. This dose far exceeds that expected at LEP (section 6.2).

3. The mechanical design

The silicon wafer support structure is shown schematically in fig. 4, together with the readout elements, water cooling manifolds and external cable routes. The innermost beryllium pipe is 1.1 mm thick and has a minimum inner radius of 53 mm. This provides the vacuum enclosure for the circulating beams. The outer pipe, 2 mm thick carbon fibre epoxy with an inner radius of 80 mm, provides the inner surface for sealing the 4 bar absolute pressure enclosure that contains both the jet and vertex drift chambers. A limited annular space between the pipes of less than 23 mm is available for the silicon detector assembly. This constrains the geometrical options for detector layout and requires a compromise between maximising azimuthal coverage and having the largest possible lever arm between detector layers. The resulting layout in $r\phi$ is shown in fig. 1, with 11 devices in the inner layer and 14 in the outer layer. The silicon of the inner layer extends over the polar angular range $|\cos \theta| < 0.83$.

3.1. The OPAL detector ladder

3.1.1. Ladder structure

The structure of an individual detector ladder is shown in fig. 5. Three silicon wafers are positioned end-to-end and the strips which are read out are wire-bonded serially to provide a detector 180 mm long with 629 readout channels at a pitch of 50 μm across a sensitive width of 31.4 mm.

The wafers are glued onto a 0.5 mm thick epoxy/Kevlar composite plate with a room tempera-

ture curing epoxy adhesive. The expansion coefficient of the plate is about 7 ppm/ $^{\circ}\text{C}$, while that of silicon is approximately 3 ppm/ $^{\circ}\text{C}$. The wafers and support represent about 0.6% of a radiation length of material for particles coming at normal incidence from the interaction point. Aluminium alloy end pieces are incorporated during fabrication of the support to act as heat sinks, and the assembly is stiffened by a light epoxy/Kevlar section glued along the axis.

A glass pitch adaptor is positioned at the end of the wafer assembly, as indicated in fig. 5. It carries 20 μm wide aluminium tracks to convert the detector strip-readout pitch of 50 μm down to the 44 μm pitch of the MX5 Microplex chips (section 4.1), which incorporate the amplifiers and analogue shift registers necessary for reading out the strips. The pitch conversion facilitates the bonding between the detector strips and input pads of the Microplex chips. A ceramic plate carrying the MX5 chips and other front-end electronics, as described in section 4.3, completes the ladder elements. It is attached to the heat sink to dissipate the heat generated by the MX5 chips.

3.1.2. Ladder assembly

The complete ladder assembly is carried out using a precision jig and measurement system consisting of:

- An optical system working at 170 \times magnification, having a CCD camera, an electronic reticule generator and monitor.
- Translation tables with linear encoder scales accurate to 5 $\mu\text{m}/\text{m}$.
- Three vacuum fixtures having adjustment in two orthogonal directions and a rotation in this plane.
- A vacuum fixture to hold an aligned set of wafers during adhesive cure.

The three wafers of each ladder are aligned individually on the vacuum fixture (c) using the optical alignment system. They are then transferred to the holding fixture (d), allowing their kevlar support to be aligned

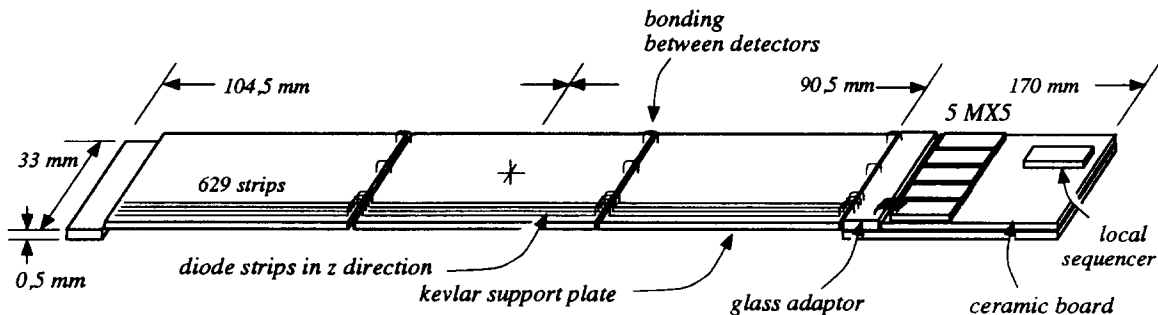


Fig. 5. The OPAL microvertex ladder; three FoxFET wafers are supported on a thin kevlar plate. They are joined together electrically by serial wire bonding of the 629 readout channels from the devices, via adaptor tracks on a glass plate, through to MX5 Microplex chips on a ceramic board. The board also houses a Local Sequencer chip and surface mounted components of the signal readout circuitry.

on the same machine. After application of the epoxy adhesive the wafer set is returned to its original axis and held in the fixture until adhesive cure is complete. The glass pitch adaptor is assembled in a similar process.

3.1.3. Bonding

Each detector ladder requires about 2600 bond-wire connections to be made between the readout strips of the three silicon wafers, the glass pitch adaptor and the inputs to the five Microplex chips (fig. 5). There are in addition 25 power and control wire connections.

The bonding was carried out at CERN using a Hughes Model 2470 ultrasonic wedge-bonding machine and 25 μm diameter aluminium wire. A check was made during bonding for “punch-through” channels, which have resistive connections between the metal readout strip and the underlying p^+ implants caused by holes in the oxide insulation layer. The individual silicon wafers were tested at Micron Semiconductors Ltd. and delivered with at least 99% good channels. After assembly and bonding about 96% of the channels of a ladder of three daisy-chained wafers are good, with low noise, no punch-through and no bonding or electronic faults. Some of the remaining 4% of channels also provide usable signals for physics analysis.

3.2. The detector mounting

The detector ladders are mounted on three split polygonal aluminium rings as indicated in fig. 4. The two end rings carry legs, two stiff and two spring-loaded, that position the detector in the supporting carbon fibre pressure pipe. The third ring, close to the MX5 readout chips, is equipped with a water cooling circuit. Two rings have dowel holes for precise positioning of the ladders. The complete structure is made from two half-shells joined together around the OPAL beam pipe, with 11 ladders mounted on the upper half-shell and 14 on the lower one.

An interconnect ring (ICR), which carries additional electronics, busses and connectors, is joined to the detector (fig. 4). Its structure also consists of two half-shells joined together around the beam pipe and supported from the pressure pipe. The ICR is made up of seven multilayer printed circuit boards mounted around three equally spaced light aluminium rings, forming a 180 mm long heptagon.

Fine wires provide the electrical connections from the ends of individual detector ladders onto the ICR assembly. Cabling from the ICR is grouped into four thin aluminium channels positioned, one in each quadrant, around the inner surface of the pressure pipe, as indicated in fig. 4. With this arrangement the cabling does not enter the fiducial acceptance of the OPAL luminosity detectors. The cable tray support consists of

300 mm long half cylinders made of kevlar/epoxy foils joined together to form a rigid structure.

For insertion within OPAL, the elements of the detector (the ladders, the ICR assemblies and four cable tray sections) are mounted in turn at the only accessible section of beam-pipe, which is 330 mm long and situated 2.36 m from the centre of OPAL. The elements are attached end-to-end in turn as the assembly is pushed towards the intersection region. The absolute position of the detector is known from a length measurement of a fine wire attached to the central structure and passed outwards through one of the cable trays. The system is maintained in a fixed position at the centre of OPAL by a braking mechanism attached to the detector support. This exerts outward pressure into the carbon fibre pipe and is activated externally.

3.3. The survey of the detector

The half-shell ladder structures were joined together for metrology measurements prior to insertion in the experiment. The metrology equipment consisted of a fixed focus periscope attached to the arm of a coordinate measuring machine. Each ladder was surveyed with 27 three-dimensional readings in a grid that spanned the three-wafer assembly. The reproducibility of these measurements was found to be at the 2 μm level within a ladder assembly, but between ladders the accuracy was limited by the 5 μm absolute accuracy of the coordinate measuring machine.

Final alignment constants of the devices, both internally, wafer to wafer and ladder to ladder, and globally for the complete assembly with respect to the surrounding drift chamber, are obtained by optimising the track fits to Z^0 decay events. Differences in the transverse positions of ladders of typically 10 μm are observed between the optical measurements and the final alignment constants.

4. The electronics

The signals, capacitively-coupled to the individual readout implant strips of a ladder, are amplified by means of five MX5 Microplex chips, whose operation is controlled by one Local Sequencer chip. These components are sited on the ceramic board attached to the detector (figs. 4, 5). The Local Sequencers are in turn controlled by a FASTBUS Master Sequencer, and the analogue signals from the detector are processed by FASTBUS SIROCCOs [4]. These FASTBUS modules are described in section 5. Connection between the detector and the FASTBUS crate, which is situated in the counting room, is made via a series of cables

passing through an external interfacing panel and the Interconnect Ring next to the detector (fig. 4).

For test purposes, the Sequencers and Microplex chips allow known calibration pulses to be injected onto the inputs of the amplifiers of a given ladder. In addition, a pulse can be applied to the backplane of the wafers on a ladder for further tests of the functioning of the readout chain.

4.1. The MX5 Microplex chip

The MX5 is a further development of the UK fully custom VLSI RAL MX series [5], taking advantage of the 1.5 μm Mietec CMOS process to achieve excellent noise performance. The detector ladders are read out by five chips each of 128 channels, positioned as shown in fig. 5. Each chip measures 6.28 mm by 6.66 mm and is 300 μm thick. Unlike previous versions of the MX-chip series, the control and readout bus lines are daisy chained across the chips by means of short bonds. The analogue signals from all five chips are multiplexed onto a single balanced pair output. In most cases the outputs of two neighbouring ladders are multiplexed together, giving 10×128 channels read out in sequence by one FASTBUS SIROCCO channel [4].

Each channel of the MX5 includes a charge-sensitive preamplifier followed by two storage capacitors and switches, used as sample-and-hold. The switches allow the storage of signals subsequently read out under the control of the 128-channel shift register. The logic of a single channel is shown in fig. 6. The chips are operated with an active amplifier filter, the "bandwidth limit", to slow the rise time of the output to about 250 ns and give a corresponding improvement (a factor of 1.6) in the noise performance of the unloaded

chip. Again, to optimise noise performance the chips are operated in high power mode, which requires the cooling to cope with a dissipated power of 250 mW per chip. With these running conditions, the noise performance of the chip in numbers of electrons is measured to be $325 + 23/\text{pF}$ equivalent noise charge (ENC). The capacitive loading represented by the three bonded silicon wafers on a ladder is deduced to be about 29 pF, from the total measured noise of a ladder assembly of about 1000 ENC. This corresponds to a signal-to-noise performance of 22:1 for minimum ionising particles traversing 300 μm of silicon in the 180 mm long ladder. It is found empirically that the noise performance of the MX5 chips deteriorates appreciably for detector bias resistance below 10 M Ω . The gate-drain voltages of the FoxFET detectors are therefore adjusted to give dynamic resistances in the 10–40 M Ω range.

When powered, the MX5 input protection circuitry shows performance degradation at radiation levels above about 30 Gy. This should not be a limitation for planned operation within OPAL, and the MX5 proves to be highly satisfactory for the readout of this detector.

4.2. The Local Sequencer chip

The Local Sequencer is a semi-custom VLSI gate array state machine designed within the OPAL collaboration [6] and fabricated in Falcon 5 μm CMOS technology by Micro Circuit Engineering [7]. The die measures 5.8 mm by 6.8 mm and has 64 bond pads, of which 28 are used on the OPAL ceramic. The device is unusual in having an analogue switching capability which allows calibration pulses to be set from an ana-

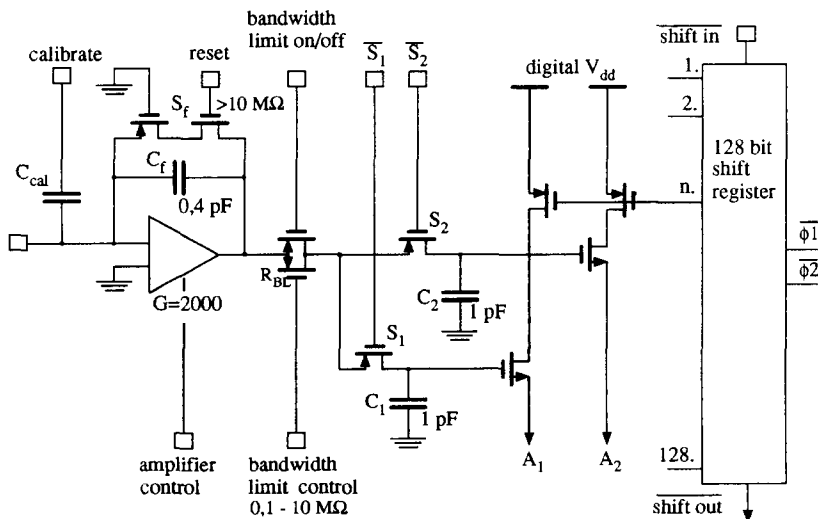


Fig. 6. The logic of a single channel of the 128-channel MX5 Microplex chip.

logue voltage derived from the Master Sequencer. Its operation is described in detail in ref. [6], and its function is to provide the capture and readout signals needed by the MX5 chips and to permit all envisaged MX operations with a minimum of input control signals and cables.

Each set of five MX5 chips on a ladder is served by a single Local Sequencer. A number of sequencers can be connected in a chain in a way that allows them to share an analogue readout path to a single SIROCCO channel while preserving a degree of independent control of each Sequencer in the chain.

Each Local Sequencer needs only four digital control signals; one "enable", two "steer" lines, and a "step" signal which acts as an asynchronous clock. Due to the parallel nature of their control the 25 Local Sequencers are driven by only two independent sets of signals, provided by the purpose-built Master Se-

quencer, which service respectively the 11 upper-half and 14 lower-half ladders. State transitions are initiated by the step signal. The steer lines choose between different transitions and set various internal flag registers at the initialisation of a run. These flags control the production of calibration pulses of either polarity, on any combination of four lines, and the state of the bandwidth limit and power-select signals to the MX5 chips.

The Local Sequencer has extensive diagnostic facilities incorporated in its design. The chips were simulated and wafer tested at 3 MHz operation, guaranteeing readout at 1.5 MHz. Higher speeds were seen to be obtainable, but unnecessary because of limitations imposed by the MX5 amplifier rise time and shift register clocking speed. Radiation tests have shown a gradual degradation in performance of the Local Sequencer above 50 Gy.

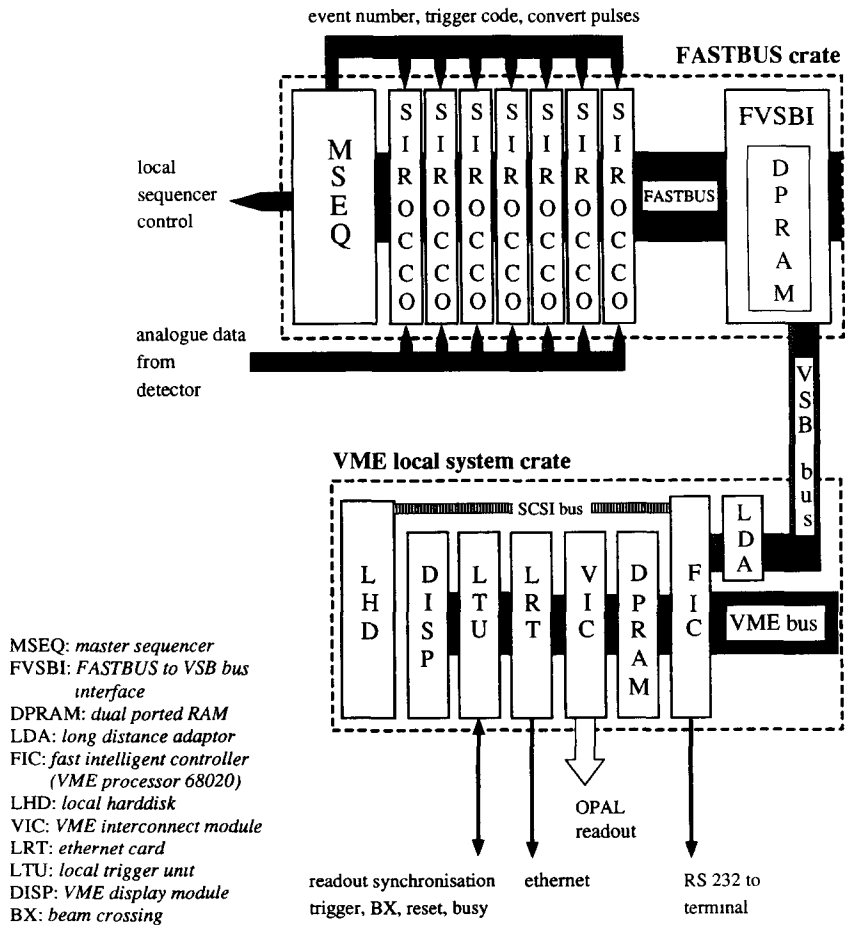


Fig. 7. An overview of the readout system, with a FASTBUS crate containing a Master Sequencer module and seven SIROCCO modules, and the readout processor housed in a VME crate. The crates are connected by a VSB bus cable and a FASTBUS to VSB bus interface (FVSBI).

4.3. The ceramic board

Each detector ladder is equipped with one ceramic board, carrying the Microplex readout chips, the Local Sequencer, surface mounted devices for calibration and low voltage power and bias filtering. Each unit is a $33 \times 65 \text{ mm}^2$ thick-film four-layer gold circuit, silk screened on a $300 \mu\text{m}$ thick ceramic (Al_2O_3) substrate, and cut to final dimensions by laser. The boards were designed, mounted and tested at CERN within OPAL, and very good noise suppression is achieved through careful screening and filtering.

4.4. The Interconnect Ring

The seven multilayer printed circuit boards of the Interconnect Ring (fig. 4) contain busses and connec-

tions serving control, biasing and powering for all 25 ladders of the microvertex detector, and high-speed differential amplifiers (AD848) for the multiplexed analogue output signals. The two independent half-rings drive the 11 upper and the 14 lower ladders, respectively. Space limitations in the four cable trays situated between the vacuum pipe and the inner surface of the pressure tube require the outgoing cables from the Interconnect Ring to consist of relatively thin copper wires, thus giving rise to substantial voltage drops over their 7 m length. The cables were specially made, with double screening and single point grounding, as well as remote sensing for the floating power supply system. These precautions have enabled the complete detector system to achieve an exceptionally high signal-to-noise ratio for the experimental data recorded in OPAL.

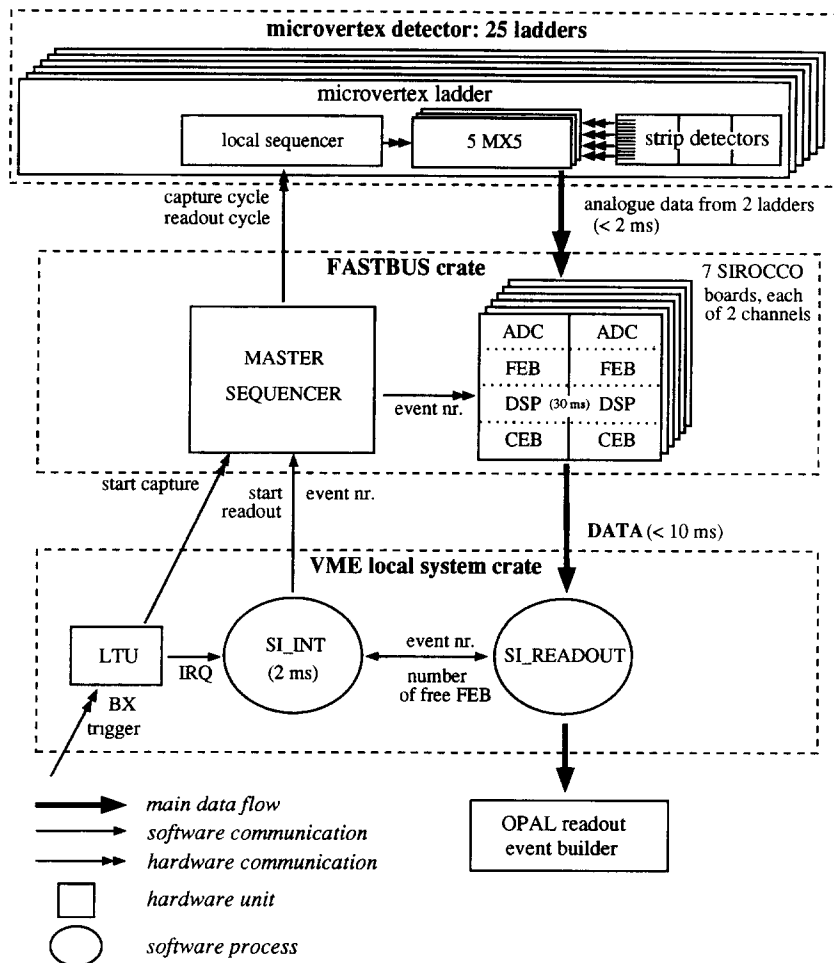


Fig. 8. Overview of the data flow in the microvertex detector readout. A trigger signal received by the local trigger unit (LTU) starts the process SI_INT. Having checked for a free front-end buffer (FEB), this starts the readout of the MX chips via the Master Sequencer and the Local Sequencers. The data are digitised on the SIROCCO board, written to a FEB, processed by the DSP and copied to a crate-end buffer (CEB), from where they are read by the process SI_READOUT.

4.5. The interfacing panel

The interfacing panel is an electrically passive and fully isolated Euro-crate chassis, mounted on the magnet of the experiment. It allows the rearrangement of controls, bias and low voltage wiring and also provides the conversion point for increasing the copper cross section of all the cables before they travel a further 25 m to the counting room. As the chassis is electrically floating and connected only to the shields of all used cables, pickup signals from external noise sources are practically eliminated. In addition, all cable shields are grounded only at the detector end to avoid noise from ground loop currents.

5. Data acquisition and real time processing

The OPAL microvertex detector has approximately 16000 individual readout strips. In order to achieve efficient data reduction without causing significant dead time, a highly parallel front-end processing system is used.

5.1. General structure

The general layout of the readout and data acquisition electronics is illustrated in fig. 7. A FASTBUS crate contains seven SIROCCO IV modules [4], which are used to digitise and process the raw analogue data, and a custom-built Master Sequencer module, which controls the whole detector via the individual Local Sequencers. The FASTBUS is interfaced via VSB bus and a FVSBI interface [8] to a standard OPAL local system crate [9]. The important components within this VME system are a FIC 8230 processor [10] running the OS-9 operating system [11], an OPAL local trigger unit (LTU), and a VME interconnect module, for communication with the OPAL event builder [9].

Control over the whole system is accomplished using a combination of hardware and software. The Master Sequencer is the key component. It contains blocks of RAM which can be loaded with code to control Local Sequencer state transitions and the necessary timing pulses for the SIROCCOs. A sequence of code is executed by incrementing the Master Sequencer address counter at a fixed rate, the necessary steering signals for the Local Sequencers being derived from the output bits in the memory. In addition, several loadable registers allow fine tuning of the Master Sequencer timing, the setup of the Local Sequencer configuration, and the determination of the size of calibrate pulses. There are three different code sequences:

1) SETFLAGS sequence:

Set up required flags in Local Sequencers.

2) CAPTURE sequence:

Carry out an analogue signal capture cycle on all ladders in synchronisation with a LEP beam crossing. In order to achieve this, the sequence is started by sending a signal derived from the previous beam crossing. This signal is vetoed by the LTU during the readout of a triggered event.

3) READOUT sequence:

Carry out a readout cycle. This results in the multiplexed data being clocked out from the front-end in synchronisation with analogue to digital conversion in the SIROCCO modules. It is initialised by the VME processor writing an event number to a Master Sequencer register, after receiving an OPAL trigger. The event number is sent by the Master Sequencer to each of the SIROCCO modules.

Each of the seven SIROCCO modules consist of two independent channels, which are used separately to process the data from the one or two inner or two outer layer ladders driven by a single Interconnect Ring (ICR) card. After digitising using a 10-bit FADC, the data are stored in one of four front-end buffers (FEB), the buffer used being determined from the lower two bits of the event number. The data are then processed using a Motorola 56001 digital signal processor (DSP) [12]. The DSPs are used to perform pedestal and noise calculation, pedestal subtraction and hit finding as described in section 5.2. After processing and sparcification, the data are formatted and written to one of four output buffers (CEB) in RAM, again depending on the event number.

The VME processor (FIC 8230) maintains control over the whole system, as illustrated in fig. 8. At the start of a run it configures and downloads the code to the DSPs and Master Sequencer. During a run two processes running in the FIC handle the communication with the FASTBUS system. The first handles the receipt of an OPAL trigger via the LTU, and starts the READOUT sequence by downloading an event number to the Master Sequencer as soon as there is a free FEB. The event number details are passed to the second process, which runs asynchronously. This process polls an address corresponding the output buffer (CEB flags) for the next expected event in each DSP channel, until the event is ready, then does a DMA transfer via VSB into local memory. A simple accounting procedure is used to determine the number of free FEBs at any instant. The event number associated with each event also provides a simple system to assure data integrity. Additional processes running on the OS-9 system provide online monitoring and histogramming and pass events on to the OPAL event builder. For development and diagnostic work, it is also possible to read real or simulated data from a local hard disk, to

download it to the DSPs for processing, and to write events to hard disk or tape.

5.2. The DSP algorithms

Great care has to be taken in the design of the DSP programs, as they are the key component of the online system for determining the quality of data coming from the microvertex detector. The programs use well proven numerical algorithms with adjustable parameters. In addition, there are online histograms which may be switched off for efficiency reasons at higher trigger rates. The programs are coded in assembler language, and are described in detail in ref. [13].

A single DSP handles the analogue data from one or two microvertex ladders (up to 10 MX5 chips or 1280 channels). Its main goals are to subtract level offsets and pedestals and to find hit clusters in order to reduce the data volume read out without losing any physics information.

5.2.1. The data model

Each readout channel has an individual pedestal value that has to be subtracted from the raw data. Pedestals can vary considerably from channel to channel, but the value for an individual channel changes only slowly with time. Each channel is assigned an incoherent noise value, which is the width of the pedestal distribution in the absence of hits, and which may also vary slowly with time. In addition, all channels read out by the same MX5 chip are allowed to be shifted by a common level offset, and this ‘‘coherent’’ noise may vary event by event and chip by chip.

5.2.2. The processing steps

There is a sequence of processing steps in each of the DSPs. Firstly, the level offsets are calculated chip by chip and subtracted from the data. To be insensitive to dead and noisy channels this is done by calculating the median of all channel contents, using a histogramming method. After subtraction of the pedestals a cluster search is performed. Here the amplitudes of two neighbouring channels are added and the sum is compared with the noise from those channels. A cluster is identified if the signal exceeds three times the noise value. The data of the channels inside a cluster and of adjacent strips are written into an event record to be read out.

In the next step pedestal and noise values are recalculated. To cope with slow drifts with time they are updated after each event for all channels with no hit using the following algorithms:

$$p_{n+1} = p_n + c_1 S,$$

$$n_{n+1}^2 = (1 - c_2)n_n^2 + c_2 S^2,$$

where S is the residual signal after offset and pedestal subtraction and p_i and n_i are the pedestals and noise values for event i . The values used for c_1 and c_2 are typically chosen to be 0.01.

The last processing step is a search for noisy channels (dynamic bad channel masking, section 5.2.4), to keep the rate of unwanted data low.

At each processing step histograms are filled to monitor the behaviour of the detector, the data processing algorithms, the suppressed data and the read-out performance. Fig. 9 shows a comparison of the data before and after processing by the DSP. Only the shaded channels are read out.

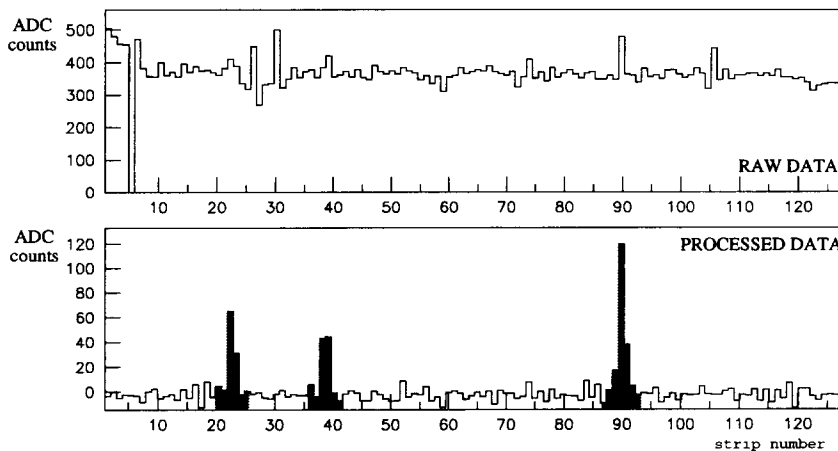


Fig. 9. Data from one MX5 chip are shown before and after processing by a SIROCCO DSP. This example contains one dead channel and three channels with abnormally high pedestal values. After the processing three genuine clusters are clearly identified, and only the shaded channels are read out.

5.2.3. Pedestal run

At the start of each run a detector calibration is performed using a hundred random triggers. The mean and rms of the amplitudes are calculated for each channel, giving the initial pedestal and noise values for the data processing algorithms.

5.2.4. Bad channels and dynamic bad channel masking

In the SIROCCO boards the status of each channel is kept in a list. Channels are flagged as NOISY or DEAD at the end of a pedestal run if their noise values lie outside upper or lower limits. In addition, dynamically after each event, a check is made for bad channels. A NOISY channel can be restored if its noise value recomputed with N (typically 25) events falls below a preset threshold. Conversely, a channel can be set NOISY if it has more than a specified number of hits from N events. NOISY channels are not read out, but their pedestal and noise values are updated so that they may recover.

For each event the number of bad channels per chip is written to the output record. In practice the number

of such bad channels was negligible throughout the 1991 data taking.

5.2.5. Performance of the DSP programs

The DSP processing time is 25–32 ms per event, depending on the amount of histogramming and the number of hits. Calculation and subtraction of offsets, subtraction of pedestals, updating of pedestals and noise and basic histogramming take 25 ms per event. The selectable histogramming can take up to an additional 7 ms per event.

5.3. Performance within OPAL

During 1991, the typical OPAL trigger rate of 3–4 Hz was easily handled using the front-end buffering. Therefore the DSP processing and readout time were not limiting and the dead time was dominated by the analogue readout and digitising sequence, which took approximately 2 ms.

A study of dilepton events has shown that inefficiencies in information transfer due to the online data

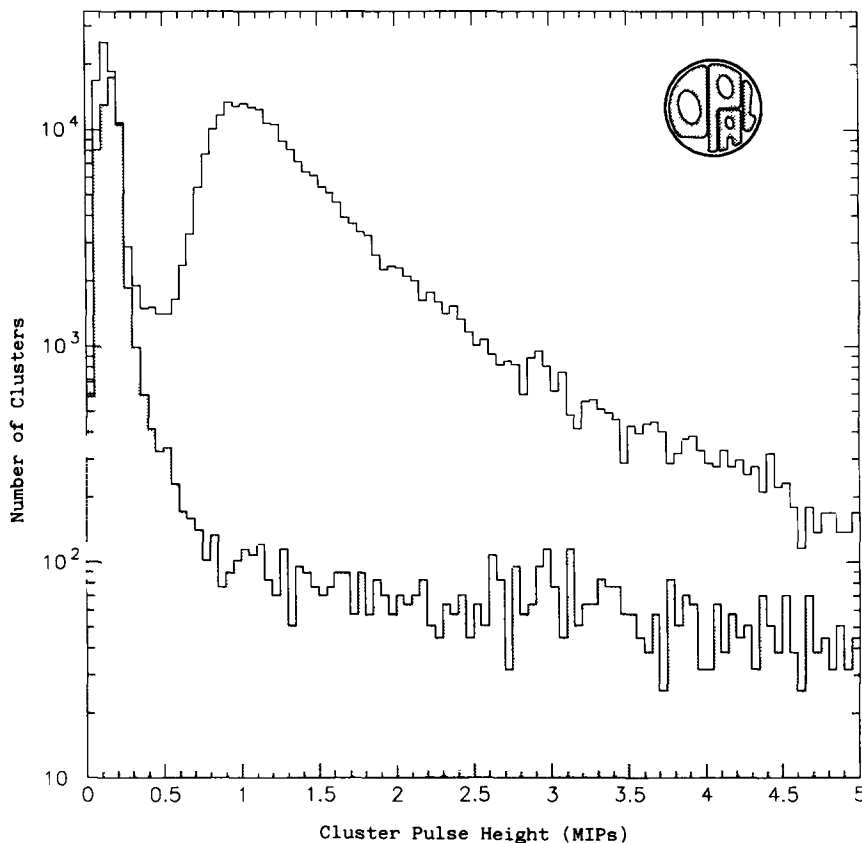


Fig. 10. The open histogram shows the distribution of the summed pulse height per cluster for hadronic Z^0 decay in units of MIPs (the pulse height from a minimum ionising particle). The shaded histogram shows the distribution seen in luminosity Bhabha events (where very few tracks enter the silicon detector) and hence the contribution from noise, synchrotron radiation, etc.

processing are negligible. After online processing the data were found to contain approximately 0.3 noise clusters per ladder. The front-end data processing therefore reduces the raw data by a factor of about 300 without losing physics information.

6. Control and monitoring systems

The systems are centred around one VME crate containing an MVME147 CPU [14] and several interface modules, notably a 32 channel VME ADC [15], connected to the various components to be controlled and monitored. The CPU runs under the OS-9 operating system [11]. All control hardware and the detector powering system run on battery backed-up non-interruptable power supplies [16].

6.1. The power system

The FoxFET detectors and the associated electronics on the Interconnect Ring (ICR) cards need six different voltages, with flexibility to allow different

settings for each ladder and ICR card. The voltages are grouped, with seven sets of supplies for each of the MX5 Microplex, high-speed amplifier and common FoxFET guard voltages, one set for each ICR card. There are in addition 25 sets of FoxFET bias, drain and gate voltages, one set for each ladder. Two low voltage channels are also needed for the common control electronics on each half-ring of ICR cards.

All power and bias voltages are provided by a LABEN powering system [17], consisting of 16 dual power supply modules, each capable of supplying two ICR cards and two detector ladders with their necessary voltages. The LABEN system is interfaced to the detector through power interface modules which re-group the voltages and protect detectors against over-voltages. By means of a passive network, appropriate time constants are included in the power interface modules to ensure smooth ramp down if the input voltages are disconnected.

The LABEN system is controlled from the CPU module via an RS232 interface which allows voltages and current limits to be loaded and continuously monitored under software control. This control software is

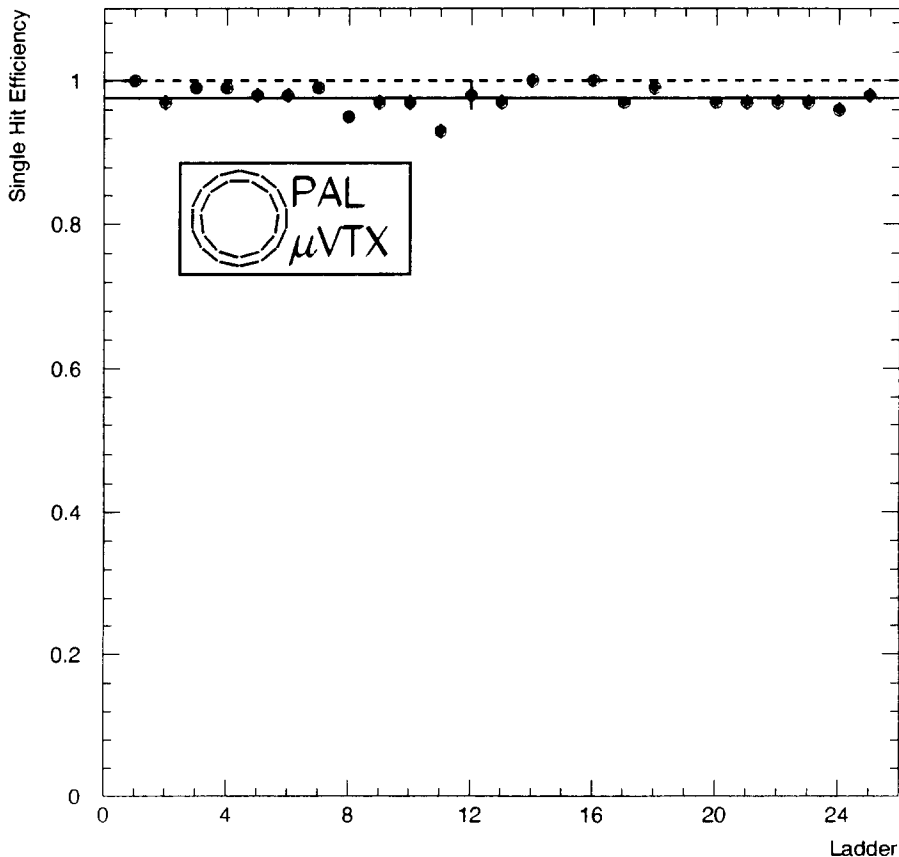


Fig. 11. The hit efficiency for each microvertex detector ladder from dimuon events.

split into three basic modules. The first is a program to ramp the voltages up and down with a menu-driven interface. The second continuously monitors correct functioning of supplies and the output voltages and currents, and the third can be called by other programs to perform an emergency ramp down. Overcurrents, voltages that are out of tolerance, or failure of the reference power supplies for the power interface modules, lead to an automatic ramp down under software control. A software-controlled ramp down is also initiated by a main power failure.

Voltage drops in the cables between the power supplies and Interconnect Ring are continuously measured by the ADC module and monitored by the CPU.

6.2. Radiation monitors

Four small radiation monitoring detectors are situated on the Interconnect Ring to measure radiation from the LEP machine at horizontal and vertical positions. These semiconductor devices [18] were carefully selected and calibrated before installation. They can record levels up to 0.8 Gy/h at a resolution of 0.25 mGy/h. The very low detector signal currents are

amplified and converted in special amplifiers mounted on the interface panel. The signal is transported to the electronics hut as a frequency, which is converted into a voltage in a purpose-built module. This voltage is then digitised by the ADC module and values are monitored by the CPU.

High radiation levels result in warnings and alarms in the OPAL control room. Although the CMOS electronics on the ladder ceramic have greater radiation tolerance when unpowered, no action is taken as high radiation bursts are normally of a shorter duration than the time required to ramp down voltages in a safe way. After the 1991 run the total radiation dose measured by the monitors was less than 0.5 Gy. This rate is expected to rise, perhaps by an order of magnitude, in future years through changes in the LEP machine. The microvertex detector is left unpowered during LEP machine development periods to minimise risk of radiation damage.

6.3. Cooling system

The 30 W of electrical power dissipated at the 25 detector ladders arises mainly from the Microplex chips

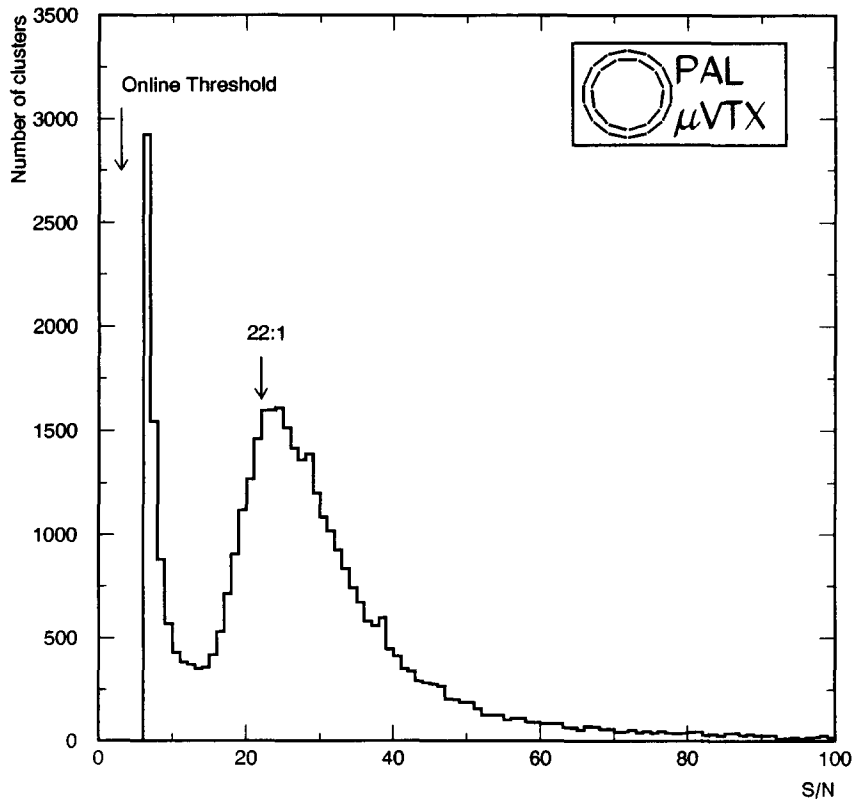


Fig. 12. The signal-to-noise ratio (S/N) for dilepton events taken in OPAL data, where the noise is the weighted average over all channels in a cluster.

mounted on the ceramic boards. This power is removed by temperature controlled circulating water. Two heat exchanger modules are cooled with primary water at 16°C, while a small magnet coupled gear pump circulates the secondary low pressure water through the detector at a rate of ~ 60 l/h. Water temperature is regulated electrically by means of Peltier elements [19] mounted between heat exchanger plates, with a maximum cooling power at 5°C temperature difference of 200 W.

The control electronics are interfaced to a VME module, that can be controlled and monitored from the CPU. Water pressure, velocity and temperatures are continually measured and monitored, and deviations from preset limits activate the control system.

The procedure for ramping the power up and down includes switching on and off cooling as needed to maintain stable temperature conditions at the detector. In equilibrium there is a temperature difference of about 3°C between the silicon at the two ends of the 180 mm long detector ladder. The power on the detector is ramped up about 8 h before the start of LEP running to ensure stable temperature conditions for data-taking, and is ramped down only at the end of a running period.

6.4. Temperature monitors

Temperatures around the detector are monitored by 21 thermistors. Seven of these are connected in

parallel in two groups to measure the ceramic board temperatures for the upper and lower half-ring ladders. Two thermistors measure the upper and lower half-ring cooling water temperatures and another six measure the temperature at three points along two of the detector ladders. Four thermistors measure the temperatures in the beam pipe cable trays, and two measure the cooling water temperature just before and after the heat exchange modules.

The thermistors are biased from a dedicated power supply and their voltages are digitised by the ADC module and monitored by the CPU, where the temperatures are also calculated to a precision of better than 0.2°C. In the event of overheating a warning is first issued in the control room, and if the temperature continues to rise the power is automatically ramped down by the software.

6.5. Interfacing within OPAL

Control and monitoring software communicate with the global OPAL slow control system. This allows error messages to be entered into the EMU [9] system and displayed on appropriate screens in the control room and elsewhere. The CPU itself can be accessed remotely through the local area network via TCP/IP software.

7. Offline processing

The offline processing for the silicon microvertex detector is performed within the framework of the standard OPAL reconstruction and Monte Carlo programs. The simulation of the silicon detector within OPAL has been described elsewhere [20]. The internal silicon pattern recognition consists of a cluster finding algorithm and the transformation of these clusters into the OPAL coordinate system. The silicon hits are then associated to tracks which have already been reconstructed in the other OPAL central tracking chambers and finally included in an overall track fit.

7.1. Cluster finding

When a minimum ionising particle traverses 300 μm of a silicon strip detector, energy is deposited with a typical Landau distribution and a most probable value of 84 keV. The particle impact point at the detector mid-plane is determined from the mean of the cluster strip positions weighted by their pulse heights.

The data available offline are the pedestal-subtracted pulse heights calculated by the DSP algorithms that pass the online cluster selection criteria (section 5.2). The offline algorithm used at present is simple, but works efficiently due to the cleanliness of the data

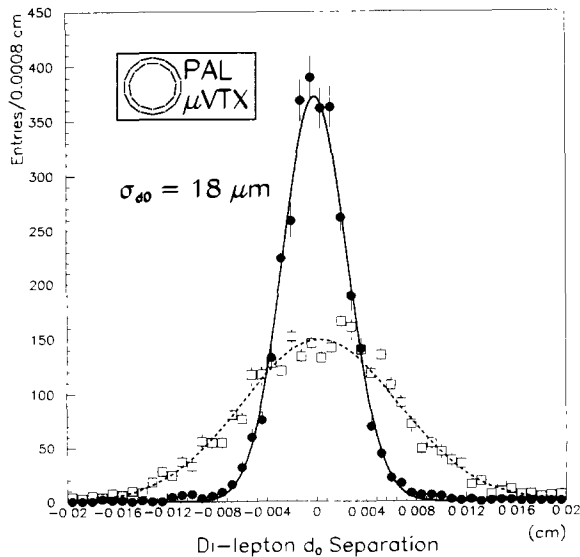


Fig. 13. The dilepton separation at the reconstructed interaction point using the central drift chambers alone (dashed), and with the addition of the silicon detector hits (solid). The latter distribution corresponds to an impact parameter (d_0) resolution of 18 μm .

coming from the DSPs. A cluster is required to have at least one strip with a pedestal-subtracted pulse height of more than 4σ , where σ is the noise of the individual strip, and an adjacent strip is included if its pulse height exceeds 1.5σ . The distribution of summed strip pulse heights in a cluster is shown in fig. 10 for hadronic Z^0 decays.

7.2. Hit association

The task of assigning silicon hits to charged tracks reconstructed in the OPAL jet and vertex drift chambers is simplified by the cleanliness of the silicon detector information and by the fact that both the track position and direction are well determined after

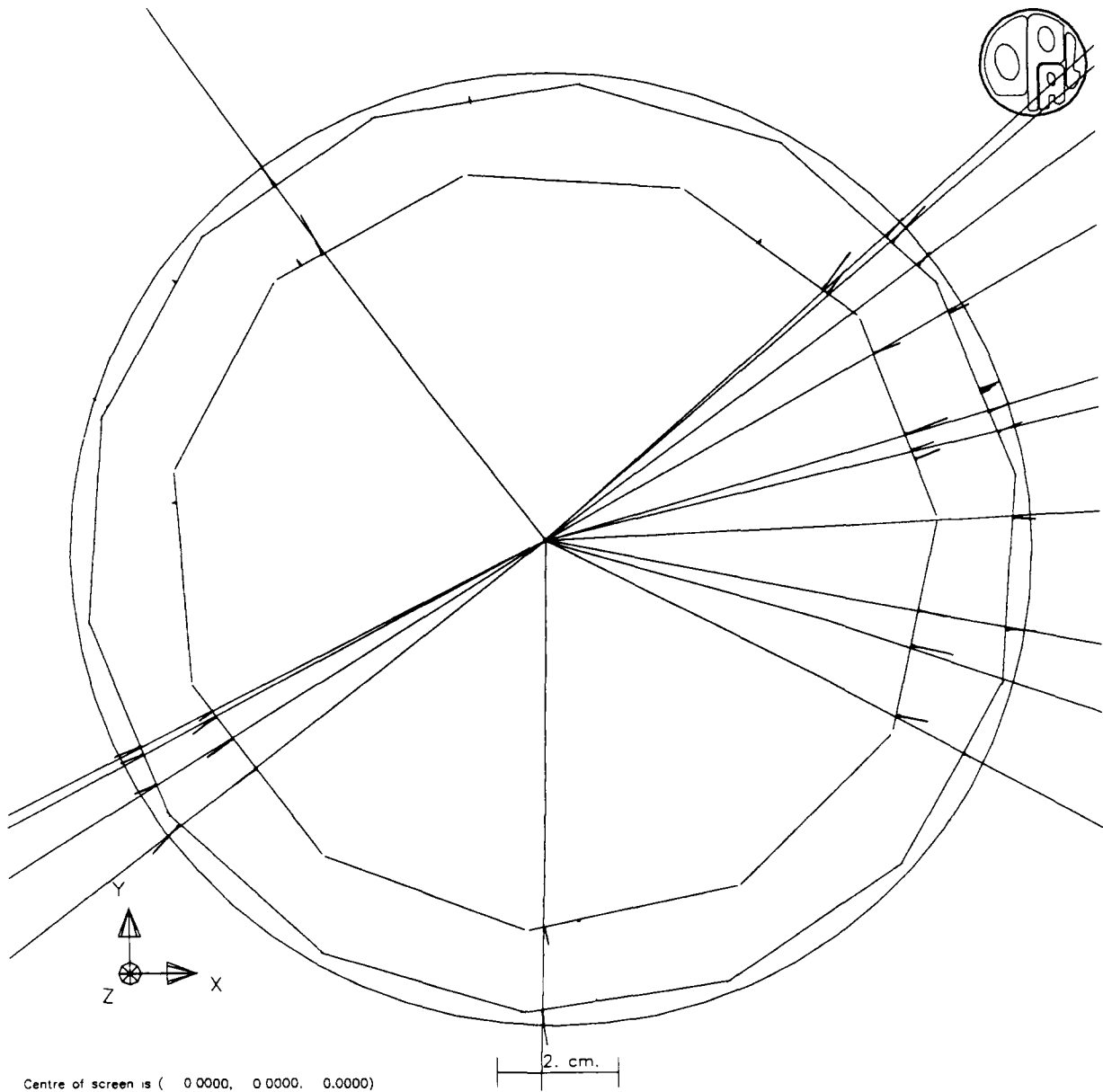


Fig. 14. A typical multihadronic decay recorded with the silicon microvertex detector, showing both the spatial and analogue pulse height information from the individual silicon detector hits.

extrapolation from the drift chamber measurements to the silicon detector. For a 5 GeV track, for example, the extrapolated position at the outer silicon barrel is known typically to about 40 μm , while the relative positions of the track at the inner and outer silicon barrels are known typically to about 10 μm .

Silicon hit association is performed using an iterative procedure. In early iterations, only well reconstructed charged tracks, normally including vertex drift chamber hits, are considered, and silicon hits are only assigned if both the inner and outer silicon barrels have unique candidates. In subsequent iterations, poorer quality tracks and potentially ambiguous associations are treated, and hits can be associated singly to tracks in cases where geometrically only one silicon layer could have provided a coordinate. Hit pairs (one from the inner barrel, one from the outer barrel) can be associated to tracks only if their absolute and relative positions are consistent with the track extrapolation within specified ranges.

Once a hit has been associated to a track, the z position of the track can be used to correct for possible z -dependent misalignments of the silicon detector (e.g. a small rotation about the beam axis) thereby improving the reconstructed (x , y) position of the silicon hit. Finally tracks with one or more silicon hits associated are refitted using a method which takes into account multiple scattering in the material between the silicon

detector and the OPAL drift chambers and within the silicon detectors themselves [21].

7.3. Alignment using tracks

A set of alignment constants, consisting of translations and rotations about three orthogonal axes, is defined for each wafer on every ladder of the detector. The metrology procedure prior to insertion in the experiment provided an initial set of these wafer alignment constants which have been refined using track-fit optimisation on dilepton events to align ladder pairs separated by 180° in azimuthal angle. Multihadronic decays provide a more comprehensive demand for relative alignment. An iterative procedure using both types of event currently results in an alignment precision of about 10 μm in the $r\phi$ plane.

The overall rotation and translation of the complete detector in the transverse plane with respect to the surrounding OPAL tracking chambers is obtained from dilepton events. The z position of the assembly is determined from tracks passing through the known small gaps between the sensitive areas of the wafers on a ladder.

The stability of the detector is such that one set of alignment constants can be used for all the 1991 data, any variations with time being below the 10 μm level.

8. The detector performance in OPAL

During the 1991 LEP running the silicon microvertex detector recorded more than 270 000 Z^0 decays, with an individual ladder hit efficiency of $\sim 97\%$ (fig. 11). Test beam configurations of OPAL ladders show the intrinsic track resolution of detectors to be better than 6 μm , with a signal-to-noise ratio for genuine hits peaked near 22:1. Fig. 12 confirms that this excellent noise performance is maintained in the OPAL environment.

Fig. 13 shows the track mismatch separation for dilepton events at the interaction point, using the central drift chambers alone, or with the addition of the silicon hits. The current impact parameter (d_0) resolution is about 18 μm , representing a factor of more than 2 improvement over the value without silicon microvertex detector data.

A typical multihadronic decay event is shown in fig. 14 with the silicon hit positions having an associated analogue display of pulse height. The reconstructed tracks are shown as extrapolations of those found in the outer chambers.

Because of the excellent signal-to-noise properties, the processed data from the DSPs are dominated by genuine hit information, with very little noise. This is illustrated in fig. 15, where the numbers of clusters

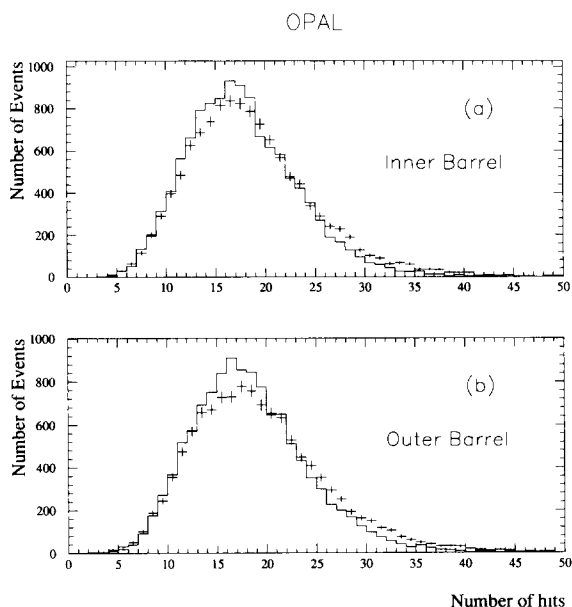


Fig. 15. A comparison between Monte Carlo prediction (solid histograms) and data (crosses) for the distribution of number of silicon hits in the inner and outer barrels of the microvertex detector in hadronic Z^0 decay events.

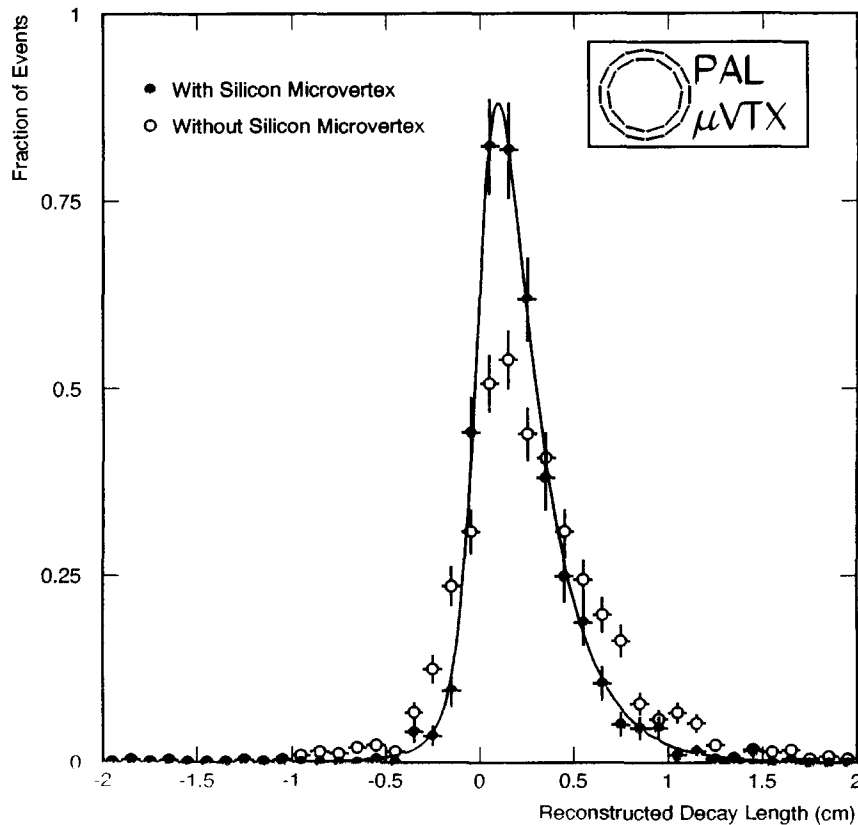


Fig. 16. The decay length distribution for 3-prong τ -decays, showing the improved resolution when silicon hit information is included in track reconstruction.

found in the inner and outer silicon barrels are compared with Monte Carlo prediction [20] for hadronic Z^0 decays. Events are simulated without the addition of noise hits from the silicon microvertex detector, and reasonable agreement is seen between data and Monte Carlo prediction.

As an illustration of the contribution now being made to the quality of track-related physics analyses we show in fig. 16 the distribution of the τ decay length obtained from the reconstruction of 3-prong τ decay vertices. The addition of the information from the silicon detector gives enhanced precision and leads to an improved determination of the τ lifetime.

9. Summary

The OPAL silicon microvertex detector was installed early in 1991, and during the 1991 data run it recorded more than a quarter of a million Z^0 decay events. The detector is well understood, and it continues to operate cleanly with excellent performance. The silicon microstrip devices provide data of exceptionally

high signal-to-noise ratio, and the silicon hit positions are known to an absolute precision of about $10 \mu\text{m}$ within OPAL for physics event reconstruction.

Acknowledgements

The successful design, construction and commissioning of the OPAL microvertex detector was made possible by the excellent technical support provided from the Cavendish Laboratory, Cambridge, CERN, Queen Mary and Westfield College and the Rutherford Appleton Laboratory Electronics and Engineering Divisions. From CERN we thank M. Burns and A. Lang for our SIROCCO modules and C. Hauviller, M. Mast and P. Wicht for the design work associated with the new OPAL vacuum and pressure pipes. We also thank the technicians of the OPAL detector group, and the PPE mechanical workshop and technical assistance groups and the MT surface treatment workshop, in particular G. Linsler, W. Bichler, G. Schmidlin, M. Price, A. Braem, D. Carminati, A. Folley, A. Gandi, F. DeDonato, L. Mastrostefano, A. Monfort and M.

Sanchez. From RAL we thank J.F. Connolly and P.H. Sharp for their support.

The contribution of Micron Semiconductor Ltd. in rapidly producing new silicon devices of excellent quality was invaluable. We thank M. Tyndel, H. Heijne and P. Weilhammer for useful discussions and P. Donnat, F. Lemeilleur, P. Gallno and M. Glaser for their participation in laboratory and test beam activities. We gratefully acknowledge the support of our funding authorities: Science and Engineering Research Council, UK, Bundesministerium für Forschung and Technologie, FRG, National Sciences and Engineering Research Council, Canada, and Department of Energy, USA.

References

- [1] P.P. Allport et al., Nucl. Instr. and Meth. A310 (1991) 155.
- [2] The OPAL Collaboration, K. Ahmed et al., Nucl. Instr. and Meth. A305 (1991) 275.
- [3] Micron Semiconductor Limited, Lancing, Sussex, UK.
- [4] N. Bingefors and M. Burns, SIROCCO IV front end readout processor for the DELPHI microvertex. Proc. Int. Conf. on Impact of Digital Microelectronics and Microprocessors on Particle Physics, Trieste, Italy, 1988, p. 116.
- [5] J.C. Stanton, A low power, low noise amplifier for a 128 channel detector read-out integrated circuit, RAL-89-009 (1989).
- [6] U.C. Dunwoody and M.J. Goodrick, The OPAL silicon microvertex local sequencer, Cavendish Laboratory preprint HEP-91/20 (1991).
- [7] Micro Circuit Engineering, Tewkesbury, UK.
- [8] M. Weymann, The FVSBI-fastbus to VSB interface, CERN internal note (1989).
- [9] J.T.M. Baines et al., The data acquisition system of the OPAL detector at LEP, to be published in Nucl. Instr. and Meth. A.
- [10] Fast intelligent controller, FIC8230, Users' Manual, Creative Electronics Systems S.A., Geneva (1987).
- [11] Using professional OS-9, version 2.2, Microware Systems Corporation, Des Moines (1987).
- [12] DSP56000/DSP56001 digital signal processor, Users' Manual, Motorola Inc., (1990).
- [13] K.H. Wolf, Online-Signalverarbeitung des OPAL-Microvertexdetektors, Diplomarbeit, Freiburg (1991).
- [14] Motorola Inc., MVME147 MPU VME module and MVME712/MVME712M transition module, Users' Manual, MVME147/DI (April 1988).
- [15] R. Hammarstrom, 32 channel multiplexed voltage ADC, version 1.3, OPAL internal note (September 1988).
- [16] Uninterruptable power supply, Vestale type V10R.
- [17] E. Frare, Programmable power supply unit model PSU 192 (Users' Guide)', ref. NSTM/0305 (March 1992), LABEN s.p.A., Milan, Italy.
- [18] Kodenshi SSC-1010 solar cells.
- [19] Melcor CP 1.4-127-06.
- [20] J. Allison et al., Nucl. Instr. and Meth. A317 (1992) 47.
- [21] P. Billoir, Nucl. Instr. and Meth. 255 (1984) 352.