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The OPAL Silicon Strip Microvertex Detector with Two Coordinate Readout

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Abstract

The OPAL experiment at the CERN LEP collider recently upgraded its silicon strip microvertex detector from one coordinate readout (ϕ only) to two coordinate readout (ϕ and z). This allows three dimensional vertex reconstruction and should improve lifetime measurements as well as b quark jet identification. This paper describes the new microvertex detector system with emphasis on the novel techniques and new components used to obtain the second coordinate information. These include the use of back-to-back single-sided detectors with orthogonally oriented readout strips, a gold printed circuit on a thin glass substrate to route the z strip signals to the electronics at the end of the detector, and the use of MX7 readout chips. Results on the performance of the new detector are presented.

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1 Introduction

1.1 Motivation for a Microvertex Detector in OPAL

OPAL is one of four large general purpose experiments running at the LEP e^+e^- collider at CERN [1]. The experiment achieves excellent charged particle tracking and momentum measurements using the combined properties of a silicon strip microvertex detector, a vertex drift chamber, a large acceptance high resolution jet-type drift chamber, and a z-readout drift chamber, all contained in a solenoidal magnetic field. Outside the tracking detectors are segmented electromagnetic and hadronic calorimeters for energy measurements of particles and jets. The outermost detection layer of the experiment consists of streamer tubes and drift chambers for muon tracking. The addition of the silicon microvertex detector to OPAL became possible after the first LEP run in 1989 when it was found that the low beam backgrounds permitted the use of a smaller diameter beam pipe. The desire for a high spatial resolution strip detector was primarily motivated by the need to measure or identify particles with typical decay lengths below a centimetre (such as b flavoured hadrons and τ leptons) and to search for new particles having similar decay lengths.

The first OPAL silicon strip microvertex detector (μVTX1) was installed and began data taking in June 1991. It consisted of two concentric layers of single-sided silicon detector wafers with AC coupled readout strips at 50 μm pitch oriented for azimuthal (ϕ) coordinate measurement.[1] A detailed description of μVTX1 can be found in Ref. [2]. The excellent single hit resolution of μVTX1 (about 5 μm rms as measured in the test beam, 8 μm in OPAL including alignment uncertainties) was demonstrated in Z^0 dilepton data where the impact parameter resolution was measured to be about 15 μm. The use of μVTX1 information resulted in a large improvement in tracking for OPAL which was directly demonstrated in the precision measurements obtained for the τ lepton and b flavoured hadron lifetimes [3] as well as improvements in b quark identification [4].

The original proposal for a microvertex detector for OPAL envisaged a two coordinate readout device, the one coordinate μVTX1 being an interim step until the techniques for two coordinate readout were perfected. It was expected that a further improvement in lifetime measurements and in the efficiency for identifying b quark events by means of three dimensional vertex reconstruction would be obtained from a microvertex detector with two coordinate readout.

1.2 Z Coordinate Readout Design Considerations: Silicon Detectors

The ideal solution for obtaining the second (z) coordinate information is to use a double-sided silicon detector with orthogonally oriented readout strips on opposite faces of the detector wafer. This optimises the signal size for minimal material thickness and allows for the possibility of pulse height correlations between the charge collected on the two sides. Double-sided detectors have already been used by the ALEPH collaboration at LEP using DC coupled devices [5]. Research and development work on AC coupled double-sided detectors was actively pursued within OPAL, however production quality devices were not obtained in time for the 1993 LEP run. Thus, an alternative solution using two single-sided

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[1]The OPAL coordinate system is defined so that z is the coordinate parallel to the beam axis, r is the coordinate normal to the beam axis, ϕ is the azimuthal angle and θ is the polar angle with respect to z.

detectors glued back-to-back (one with ϕ, one with z readout strips) was implemented. This solution obtains high quality two coordinate position measurements and benefits from the operational experience and good performance of the μVTX1 detector.

1.3 Z Coordinate Readout Design Considerations: Z Signal Routing

OPAL wished to achieve z coordinate readout without adding significant material within the acceptance of the detector, in contrast to designs that put the z coordinate readout electronics directly at the end of the z readout strips and therefore in the detector acceptance. These latter designs result in increased multiple scattering and backgrounds from photon conversions as well as difficulties in cooling the electronics. These problems can be avoided by routing the z strip signal to the end of the ladders, as is done for the ϕ strips. This can be realised in several ways; successful results have been achieved using metallised prints on glass, metallised prints on Kapton [6], and extra metallisation layers on the detector surfaces ('double-metallisation') [7]. The OPAL design uses a gold printed circuit on a glass substrate. The glass substrate is chosen to be thin (200 μm) to minimise the material in the active region. The details of this print are given in Sec. 3.2.2.

1.4 Overview of the New Microvertex Detector (μVTX2)

Apart from the schemes for z readout detectors and signal routing, the overall system structure of the new two coordinate readout silicon microvertex detector (μVTX2) follows closely the design of μVTX1. The basic modular unit is again the 'ladder' consisting of three pairs of back-to-back ϕ and z detectors aligned lengthwise in a row as shown in Fig. 1. Eleven ladders form the inner cylindrical detection layer and 14 ladders form the outer layer. Their radial positions (approximately 61 mm for the inner layer and 75 mm for the outer as shown in Fig. 2) are nearly identical to those of μVTX1. The ladders are so arranged in the two layers to avoid lining up the small gaps in ϕ coverage occuring between adjacent ladders in a layer, thus ensuring nearly 100% single hit coverage.

All the internal (located inside the OPAL detector proper) microvertex system has been redesigned and constructed for μVTX2. Many of the external support systems (located nearby but external to the OPAL detector) such as the data acquisition, power supply, monitoring, and cooling systems are similar or identical to those used in μVTX1. This paper will concentrate on the new features in μVTX2 and the modifications of the μVTX1 systems made for the new detector. For completeness, brief summaries will be given for systems that were carried over from μVTX1. Further details of those can be found in Ref. [2].

The following sections of this paper will describe: the detector wafers and their acceptance testing (Sec. 2); the mechanical design of the detector system focussing on ladder construction (Sec. 3); the front-end electronics (Sec. 4); the data acquisition and online processing (Sec. 5); the powering, cooling, and monitoring systems (Sec. 6); the offline processing and software alignment (Sec. 7); the detector performance (Sec. 8); and a concluding summary (Sec. 9).

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2 Detector Wafers

2.1 Single-sided FoxFET Biased Silicon Strip Detectors

The detector wafers used in μVTX2 are single-sided AC coupled FoxFET biased silicon strip detectors designed by OPAL and manufactured by Micron Semiconductor Ltd. [8] The ϕ readout detectors are identical in design to those used in μVTX1 apart from the thickness (reduced from 300 μm to 250 μm) and are further described in Ref. [9]. The implant strip pitch is 25 μm and the readout pitch is 50 μm. The z readout detectors have their strip orientation orthogonal to that of the ϕ detectors but the biasing structures and processing are otherwise the same. The z detectors have an implant strip pitch of 25 μm but have a readout pitch of 100 μm. A close-up view of a corner of the z detector design is shown in Fig. 3. The detector size for both ϕ and z is 33 mm × 60 mm, identical to that used in μVTX1.

The detectors are made from high resistivity (>5 kΩ cm) n-type bulk silicon with n^+-type doping and metallisation on the backplane and with p-type implant strips on the front (readout) side. Aluminium readout strips are metallised above every other (for ϕ detectors) or every fourth implant strip (for z detectors) with a silicon oxide layer in between to form the AC coupling capacitor. The implanted strips are biased via a multi-source, single drain MOS structure, called the FoxFET (for Field oxide Field Effect Transistor). The drain is a p-type implant bias line that runs around the active strip detection area. The FoxFET biasing structure is formed by the end of the implant strips (the source), the drain bias line and the gap between them which forms a p-n-p junction. A field plate (the gate) is metallised over an oxide layer above this gap. Biasing of the strips is obtained by the 'reach-through' mechanism which allows current to flow across the gap when a sufficient voltage difference exists between the drain and the strip. The effective resistance of this mechanism is a function of the strip leakage current and is typically greater than 100 MΩ. The gate provides a means for modifying the voltage/current properties of the biasing structure which can be useful if voltage shifts from radiation damage or other sources need to be compensated. Another p-type implanted strip, called the guard, lies outside the drain bias line. This is used to ensure uniform fields at the endmost strips and to collect leakage current occurring near the detector edges. The detectors are passivated with a silox coating.

2.2 Operation of Detectors

The depletion voltage for the detectors is expected to be in the range 15–40 V, as determined by measurements of test structure diodes from the same processed silicon wafers as the detectors. The bias voltage applied between the drain line and the backplane is in the range 35–60 V. The extra voltage above the expected depletion voltage compensates the voltage drop over the strip to drain channel and guarantees full depletion of the entire active region in all six detectors on a ladder. The gate to drain voltage is chosen to optimise noise performance and readout behaviour of the strips. In general for a gate–drain voltage difference below -15 V, the strip to drain channel becomes highly conductive thus producing a large thermal noise contribution. However, the average noise for strips is minimised and constant for a gate–drain voltage difference above -10 V. Furthermore, for this same range of gate–drain voltage difference, the number of badly behaved strips in the readout is low and no degradation in position resolution is observed. The gate-drain

voltage difference is chosen to be 0 V for straight-forward operation.

2.3 Detector Acceptance Testing and Results of Tests

Owing to the large number of detector wafers in the system (150) and the fact that access to the detector can occur only once a year during the LEP winter shutdown, a rigorous testing procedure was applied to all detector wafers to ensure system reliability. Visual inspections for defects, long term leakage current tests, and checks for AC coupling capacitor shorts were performed on each detector wafer before ladder assembly.

2.3.1 Visual Inspections

Detector design specifications required that there be less than 1% defective readout strips per detector. Each detector was visually inspected at CERN with a high magnification microscope. Typical flaws included shorts between or discontinuities in the metallised readout strips and defects in implants or metallisation. Only five detectors out of 260 inspected were rejected for excessive defects. However, the information on location of defects was valuable in choosing the best detectors and their optimum placement on the ladders. The average number of defective strips per detector from good wafers was about 1.5 (0.2%), well within the acceptance criterion.

2.3.2 Leakage Current Tests

Every detector was placed in a hermetically sealed probe station containing a dry nitrogen atmosphere, in which the bias voltage was set to the full expected depletion voltage plus an additional 20 V for at least eight hours. The individual drain, guard, and gate leakage currents were monitored throughout the test. For most detectors the currents would stabilise after about an hour. However, on some detectors, the currents (usually the guard current) would either increase dramatically after a few hours of running, or would behave erratically. The detector specifications called for a total leakage current of less than $1\mu A$. A total of 15 detectors (about 6%) were rejected for excessive leakage current. A distribution of the total leakage current at the end of the long term test for all detectors is shown in Fig. 4.

The microvertex detector in OPAL is run in a dry nitrogen atmosphere to avoid humidity induced effects that could lead to large leakage currents in the detectors. The long term leakage tests described above were performed with a relative humidity below 20%. In a sub-sample of detectors tested for humidity sensitivity about 10% had unstable or greatly increased leakage currents (mostly guard current) when exposed to greater than 40% relative humidity. Detectors with humidity sensitivity were not rejected if they passed the long term tests since they would be in a similarly dry environment when installed in the OPAL experiment. However, some correlation was observed between humidity sensitivity and the radiation induced leakage currents that occurred during the 1993 LEP run (Sec. 8.2).

4

3 Mechanical Design

3.1 Overview

The internal μVTX2 system consists of the silicon detector ladders, their mechanical support structure, and the front-end electronics. The mechanical assembly of this part of the μVTX2 system is shown schematically in Fig. 5. The principal features are: 25 ladders arranged in two concentric cylinders about the beam pipe; the three support rings to support the ladders, one of which is water cooled; two 200 μm thick beryllium support shells (half cylinders) which provide rigidity and isolate the ladders from forces during installation; the set of seven interconnect ring (ICR) printed circuit cards containing voltage fanout, control logic, and signal routing; and the cable guides carrying the cabling of all power, biasing, control and readout lines. The cables to the external support systems are taken from one end of the microvertex detector out along the LEP beam pipe. All these elements must fit in the narrow region between the 1.1 mm thick beryllium beam pipe and the inner wall of the pressure vessel containing the OPAL central tracking detectors. This space extends from radii of 54 mm to 80 mm.

Care was taken to minimise the radiation length of material such that for a particle emerging from the collision point at 90° to the beam direction, the total amount of material traversed in the μVTX2 detector system is, on average, 1.5% of a radiation length(X_0). The main contributions are from the silicon detectors ($1.1\%\,X_0$), the z-print ($0.3\%\,X_0$) and the beryllium shells ($0.1\%\,X_0$).

3.2 Ladder Structure

3.2.1 Ladder components

The components needed to construct a μVTX2 ladder are shown in an exploded schematic drawing in Fig. 6. In addition to the ϕ and z detector wafers, there are the gold print on glass for z readout ('z-print'); an aluminium print on quartz to adapt the readout pitch of the ϕ detectors to that of the amplifier chips for easier bonding ('pitch adaptor'); two thick film hybrid printed circuit boards ('hybrids') made on ceramic substrates which contain the readout chips and associated electronic components (one hybrid for each of the ϕ and z sides); two Kevlar-epoxy stiffener ribs; and finally an aluminium support plate with a fibreglass-epoxy skeleton frame glued to it, the frame serving as a spacer between the z-print and the back-to-back detector wafer sandwich.

3.2.2 The z-print

The z-print is a gold printed circuit on a thin glass substrate that routes the z strip signals to the front-end electronics located at the end of the ladder. As illustrated in Fig. 7, each z readout strip from a detector is daisy-chained to the equivalent strip on the next detector by bonding from the strips to the appropriate diagonal lines on the z-print that terminate next to those strips. The strips on the detector closest to the electronics are bonded to z-print lines that lead to the end of the ladder with their pitch matched to that of the front-end electronics chips. This daisy-chaining of detectors results in a three-fold ambiguity in assigning the position for a z readout channel. The z-print circuit is narrower than the detectors to facilitate the wire bond connections between the bond

pads at the edge of the z-print and the corresponding bond pads along the edges of the three detectors.

The z-print is made on 200 μm thick borosilicate glass with 0.8 μm thick gold metallisation [10] on chromium contact metal. There are nearly 1800 separate lines on each z-print with a typical metal line width and pitch of 20 μm and 40 μm, respectively. After processing the z-print is cut to a size of 29 mm by 209 mm.

3.2.3 Description of ladder assembly

The ladder assembly process begins with the fabrication of the light-weight frame made with 1 mm $\times$ 0.5 mm fibreglass-epoxy sections. At each end there is a 0.5 mm thick aluminium plate with fixing and alignment holes. The larger of these plates is used to support the hybrids and to transmit the heat from the electronics to the cooling ring. The location of the frame members is arranged to stiffen the detectors and z-print under the bond positions. The hybrids for the ϕ and z readout are glued simultaneously to opposite sides of the larger aluminium plate in a jig, using an epoxy. Curing is made at 100° C to prevent cracking of the ceramic during subsequent glueing with hot-setting compounds. The fibreglass-epoxy frame separates the detectors and the z-print by 1 mm which brings the level of the z-print to about that of the readout chips which facilitates bonding (Sec. 3.2.4).

The z detectors are aligned with a 0.4 mm gap between adjacent detectors. They are then joined to the structure with a hot-setting silicone glue [11]. The glue allows a low-stress fixing onto the active surface of the detector. To avoid distortion, all further assembly is made at room temperature. The z-print is then glued to the ladder using cold-setting epoxy and glass spacers are added at the readout end to support the thin glass under the bond pads. Note that the glass substrate of the z-print is an integral element of the ladder which provides structural rigidity.

The ϕ detectors are then glued back-to-back to the previously assembled z detectors. This assembly is made, after alignment, using cold-setting epoxy and including 25 μm diameter wires sandwiched between the detectors to provide the backplane bias contact. The wires are stretched the length of the detectors on the ladder and contact is made with conductive epoxy.

Alignment of both the ϕ and z detectors is made with respect to the alignment holes in the aluminium plates to an accuracy of about 10 μm. The alignment is carried out on a precision x–y transport table. This table is equipped with a video camera viewing through a high magnification microscope, a micron precision position readout, and three independent detector positioners. A record of the positions of selected detector fiducial marks is kept as the starting point for the software alignment procedure (Sec. 7.3) which makes the final determination of detector positions.

The pitch adapter, an aluminium printed circuit on quartz [12], is glued with cold-setting epoxy on the ϕ side. This print carries bias connections and provides readout connections by matching the pitch of the readout strips of the ϕ detectors to that of the readout chips. A pair of printed circuit strips on glass are glued to the z side of the aluminium plate to provide the bias connections to the z detectors from the hybrids. Finally, a pair of Kevlar-epoxy stiffener ribs are glued to the z-print, again with cold-setting epoxy. These ribs are 4 mm high, 200 μm thick, and 208 mm long. They run almost the full length of the z-print, providing rigidity against bowing. The completed

assembly is then ready for bonding.

3.2.4 Bonding of ladder elements

All connections between the detectors and the prints (z-print or pitch adaptor) and between the prints and the readout electronics are made by aluminium wire wedge bonding on an automatic bonding machine [13]. A total of more than 6000 bonds are made per ladder. The bonding is done in automatic mode and typically takes one day to complete one ladder. For bonding the ϕ side, the ladder is clamped down on the stiffener ribs. For the z side bonding, the ladder rests with the ϕ detectors face down, held in place by vacuum on Teflon pads.

About half the bonds are at a pitch of 44 μm or 50 μm. The other half, those between z-prints and z detectors, are at a pitch of 100 μm. The high density bonding is obtained by superposing two layers of bonds between two sets of pad rows at a pitch of 88 μm or 100 μm. This bonding is easier if the two surfaces to be interconnected are at the same height. If the bonds are in one row and the higher surface is non-conducting outside the bond pads, as is the case for the connection between the z-print and the z detectors, the machine can bond across a level difference of up to several millimetres.

The detector wafer bias voltages are brought to the ladders via RC filtering circuits located on the hybrids. Bond connections are made from the hybrids to metal bias lines on the glass prints or pitch adaptors. These bias lines, with the exception of the backplane bias, are then bonded to bias pads on the first detectors. Bias bond pads exist at both ends of all detectors and allow bias lines to be daisy-chained to all three detectors on each side of the ladder. The backplane bias connection is made by routing the two wires that were sandwiched between the ϕ and z detectors, to the appropriate bias lines on the pitch adaptor and glueing them down with conductive epoxy. When the bonding is completed the ladder is ready for readout testing.

3.2.5 Problems encountered during ladder construction

A serious problem was encountered in the bonding of the ϕ detectors. The number of strips per ladder having both high leakage current and shorted AC coupling capacitors was observed to increase slowly as ladder construction proceeded. This combination of faults led to higher noise and saturation of the amplifier channel of the strip owing to the leakage current flow to the input. Adjacent channels were also affected if the leakage current was large. This problem started at the few per mil level but increased to the percent level midway through ladder construction. The solution was to change from 25 μm to 17.5 μm diameter bond wire. Although 25 μm wire is considered standard for this type of application, it appears that the different bond parameters used for bonding the thinner wire (much less energy, time, and pressure) were necessary to avoid damage to the detectors.

Metal adhesion on the z-print, pitch adaptor, and hybrids required particular attention. The manufacturers of these pieces required several attempts before satisfactory metal adhesion of the bonding surfaces was achieved. Bond testing before acceptance was essential to avoid later problems. It was also found that problems of metal adhesion were much reduced when bonding with the thinner (17.5 μm) bond wire.

In addition to metal adhesion, a number of technical difficulties were encountered in producing the large, high detail, high print quality z-print. The first was that the required

size (209 mm × 29 mm) exceeded that allowed by most processing machines which were intended for silicon wafers with maximum diameters of 6 inches (153 mm).

Secondly, the specified print quality of fewer than 10 defects (shorted lines or open circuits) per piece was not often achieved and, given the tight ladder production schedule, there was no time for reprocessing cycles to improve the print quality. Although about 75% of the prints did not have the specified quality, it was found that nearly all defects could be repaired by hand. Shorts were cut through by scraping with a scribe needle in a probe station micro-manipulator. Opens were fixed by bonding across the gap in the metal line. This repair procedure required significant manpower but did allow completion of the project on time and with a very low print defect rate (about 1–2 defects per print).

A third difficulty with the z-print arose when cutting the circuit to the desired size. It was not possible to print the circuit on a pre-cut glass blank because the metal lines needed to approach the edges of the glass closely. The metallisation and etching techniques require considerable space between the print and the glass edge to achieve good print quality. Therefore the print was cut from a larger piece of glass after processing, with the best result obtained not by sawing but rather by careful scribing with a diamond tool. Despite the apparent fragility of the 200 μm thick z-prints, none was broken in cutting, in ladder construction, or in handling of ladders.

3.2.6 Ladder testing, repairs, and results

The completed ladder assembly was given a thorough set of tests to verify the quality of the readout, the expected depletion voltage, the signal to noise ratio measured with a radioactive source, and the long term stability of both the leakage currents and the readout quality.

The quality level of ladders after their final tests was such that more than 99% of channels had good readout characteristics (low noise, no large pedestal offsets, proper connection to the strips on the detectors). However, to obtain this quality level all ladders required some fault repair. The largest number of such faults was due to remaining or created shorts and opens in the metal lines on the z-print. These z-print faults were repaired in the same way as described in Sec. 3.2.5. However, the full ladder structure did not allow all lines with open circuits to be repaired. Many of the channels damaged by bonding (Sec. 3.2.5) were disconnected from their readout by removing their bonds. Faults in ladders were identified by reading out all the channels of a ladder and searching for channels with non-standard pedestal or noise values. This test and the tests described below were performed with a small scale readout system that used very similar digitising and control electronics, but based on CAMAC rather than Fastbus, as used in the full system in OPAL.

After repairs, the ladder operating voltage was verified by a backplane pulsing test. In this test a pulse injected onto the common backplane biasing line of the ladder induces a signal on all readout channels of the ladder. The signal is proportional to the strip to backplane capacitance. The capacitance is a measure of the depletion depth in the silicon; it decreases quickly as the bias voltage is applied and finally reaches an asymptotic value when full depletion occurs. The operating voltage was chosen 5 V above this depetion voltage. The depletion voltage determined by this method agreed with the value expected from the measured wafer test structure depletion voltage and behaviour of the FoxFET biasing structures.

The signal to noise ratio was measured separately for each of the six detectors on the ladder. A collimated Ru^{106} β source was used to illuminate a small spot of about 5 mm diameter approximately in the middle of each detector and a signal from minimum ionising particles observed. The signal to noise ratios measured in this way agreed closely with those later measured with data in the final detector (Sec. 8.3).

A final test involved running the ladders in readout mode with full biasing for an extended period of time. This test verified the long term stability of all important ladder parameters, for example leakage currents, readout data quality, and power consumption. This test was carried out for a minimum of 24 hours in conditions resembling as closely as possible those expected for the installed detector in OPAL (e.g. temperature, humidity, voltages, cycling of readout). Some ladders showed poor stability in either their leakage currents or readout quality but most showed no significant changes. The ladders were rated based on their readout quality, stability, and quality of the mechanical construction. Of 35 ladders, one was irreparably damaged before completion, two were completed but had significant damage or problems, and the remaining 32 were considered to be usable for installation but with varying levels of quality. The best 25 ladders were selected for use in the detector with the remaining seven being available as spares.

3.3   Overall System Structure, Assembly and Installation

The installed detector assembly has the 25 ladders carried by a structure of three polygonal aluminium support rings (Fig. 5). Each ring is split into two halves to allow fitting around the beam pipe. For the assembly operation, the detector array consists of two half shells fitted with all ladders except the four on the outer layer adjacent to the ring joints. The halves are joined *in situ* and then the remaining ladders are added. Rings 1 and 2 are rigidly linked by two beryllium shells that isolate the ladders from insertion loads. Ring 2 incorporates a water cooling manifold which was soldered in place with a high thermal conductivity alloy [14]. The readout ends of the ladders are attached to this ring by means of screws fixing the aluminium support plates to the ring for heat removal. To allow for tolerances in the lengths of individual ladders and for thermal contraction should the readout of a ladder not be powered, the ladders are rigidly clamped only to this cooled ring and to ring 3. Fixing to ring 1 (the end away from the readout electronics) is achieved by means of a spring-loaded clamping system and a dowel pin engaged in an elongated hole, which allows small longitudinal movements of the ladders with respect to the support structure. The clamping to ring 3 also acts to spread the mechanical loads generated by the cables.

The whole microvertex structure is supported externally from the inner wall of the central detector pressure vessel ('support') tube by sets of rolling bearings assembled to rings 1 and 3. These bearings are 9.5 mm diameter hollow aluminium spheres arranged to roll freely. There are four spheres at each ring, two fixed and two spring loaded. When the whole detector structure is inserted into the centre of the experiment, the position along the beam pipe is determined to a precision of about 1 mm by measuring the length of a wire passed out to the support tube end. This position is subsequently made more precise by the software alignment analysis (Sec. 7.3). When the array is in position further movement is inhibited by activating a band brake ring which locks onto the inner surface of the support tube wall. This brake mechanism is mounted on ring 3 and prevents the detector array from moving due to forces from the cables. The completed detector

assembly is shown ready for insertion into the centre of the experiment in Fig. 8.

Cables from the ladders are plugged into connectors on the interconnect ring (ICR) cards. The cables from the ICR cards to the external systems lead to the cable carrying structure where they are arranged uniformly around the beam pipe and routed out to the end of the support tube. The structure carrying the ICR cards and cables is split in two halves for assembly in a similar way to the detector structure. None of these structures is longer than 350 mm, owing to the insertion length about the beam pipe available for assembly. The component parts are assembled on this free length of beam pipe, then pushed into the support tube to free the space for the subsequent part. After the assembly and testing *in situ*, the volume between the beam pipe and the support tube is sealed and a dry nitrogen atmosphere is established around the detector array.

4 The Front-end Electronics and ICR Cards

4.1 Overview

The strips from each side of a ladder are connected to the front-end electronics located on the hybrids at the end of the ladder. The front-end electronics consists of 5 MX7 Microplex VLSI readout chips [15] which receive the detector signals and a Local Sequencer (digital logic array) chip to control them. The Local Sequencers themselves are controlled via the ICR card logic by the Fastbus Master Sequencer module which is located external to the OPAL detector. Analogue output signals from the front-end electronics pass via the ICR cards to the external electronics hut where they are processed by the Fastbus SIROCCO IV [16] modules which digitise, store and process the data (Sec. 5.3). The Local Sequencers and MX7 chips allow test calibration pulses to be injected into the front-end amplifiers of each readout channel. In addition the common backplane bias line of a ladder can be pulsed to check the functioning of the complete readout chain and to determine the ladder operating voltage as described in Sec. 3.2.6.

4.2 Thick Film Hybrid Printed Circuit Board

The thick film hybrid printed circuit board ('hybrid') carries the 5 MX7 readout chips, the Local Sequencer chip, and other surface mounted devices (SMDs) needed for the digital controls, the analogue readout, and the biasing voltage circuits. Identical hybrids are used for both the ϕ and z side readout. This board, shown in Fig. 9, is built on a beryllium oxide (BeO) ceramic substrate [17] of 380 μm thickness. This substance is chosen to minimise the radiation lengths of material and to optimise heat conduction. The MX7 chips are the major heat source in the internal microvertex system (about 60 W for the 25 ladders) and the high heat conductivity of BeO is desirable for transmitting the heat load to the water cooled support ring.

The hybrid is divided in three areas:

- the inner (the right side in Fig. 9), carrying unpackaged MX7 chips and some filter capacitors;

- the intermediate, with no components, which allows access to the fixing screws to the cooling and support ring;

- the outer, having the unpackaged Local Sequencer chip, many standard passive components and soldered wire connections.

The limited space available for the detector required that the smallest possible components be used. All necessary bias, calibration and filter components are mounted on the hybrid rather than on the ICR card to reduce the number of interconnecting wires. Very flexible wires, soldered to the hybrid and ending in one small 25-pin connector, bring the low voltage power, bias and control voltages, and digital TTL control signals from the ICR card. The multiplexed analogue output signals from the MX7s are passed to the ICR card via a shielded twisted pair cable that is also attached to this connector.

The hybrid layout, prototype and pre-series production were carried out at CERN, while series production was transferred to industry [18]. The line density and complexity of this hybrid requires special tools and techniques for the fabrication and component mounting. Photolithography, as opposed to a standard silk-screen technique, is used on the first metal layer to achieve high line density with high print quality and good metal adhesion. SMD components are reflow soldered to the hybrids in a machine using modified settings to achieve reliable solder connections. Preheating is needed for wire soldering, owing to the very good heat conductivity of the BeO substrate.

The hybrid has four metal layers and three intermediate insulation layers. Some lines must withstand full detector bias voltages with no leakage currents so special attention was paid to the electrical insulation between layers and adjacent lines. Insulation layers are always printed twice and with different masks to reduce the probability of having superposed holes which may lead to short circuits.

Quality control of the hybrid was performed on four separate occasions:

- optical inspection and electrical tests on component-less hybrids;

- tests on SMD mounted, cleaned and wired hybrids (without chips);

- tests on chip mounted and bonded hybrids;

- final tests on mounted and bonded hybrids glued to the ladder structure.

The first test included conductor resistance measurements and insulation tests between neighbouring lines and underlying or overlying conductors. The insulation test had the highest failure rate and almost 20% of the hybrids had one or more pinholes causing short circuits. These occurred mainly between large surface conductors such as power lines and the ground plane. Shorts were successfully eliminated using an electric discharge fusing technique with no loss of hybrids. Out of 86 component-less hybrids fabricated, only six were considered unusable for ladders due to defects, damage, or bonding problems.

4.3   The MX7 Chips

The MX7 VLSI readout chip is an improved version of the 128 channel MX5 chip used for μVTX1 [2]. Each channel consists of a charge amplifier and bandwidth limiting filter with the output connected by switches to two storage capacitors. One of these is isolated from the amplifier output immediately before the LEP bunch crossing and the other after integration of the detector signal. This double-correlated sampling technique reduces the low frequency noise sensitivity of the system. The two analogue samplings for each channel

are stored until a trigger decision is made. If a trigger occurs, the two samplings form a differential analogue output signal that is sent sequentially, one channel after another, at 1MHz through a common output bus. In the absence of a trigger, a reset clears the charge to be ready for the next bunch crossing.

The MX7 chip includes several design improvements on the MX5 device, and achieves better performance. A larger input FET with external bulk bias control results in a 20% improvement in noise performance. Radiation tolerance has been improved, mainly by the use of diode (rather than FoxFET) input protection. Degradation in performance is at the level of a few percent at 200 Gy and the chip functions beyond 500 Gy. Additional improvements, although not crucial for operation of the present detector, include more uniform response achieved by more robust bussing of ground and power lines, more reliable output multiplexing, and improved charge storage.

In OPAL, the MX7s are run in high power mode and dissipate about 2 mW per channel. The post-filter signal has a risetime of 400 ns and is integrated for about 1.8 μs. With these conditions the equivalent input noise charge as a function of input load capacitance is measured to be approximately $350 + 15/\text{pF}$ (rms) electrons. This is consistent with the measured noise for readout channels on the ladders given the expected capacitive loading due to interstrip capacitance on the detectors and prints.

4.4   The Local Sequencer Chip

The Local Sequencer is a gate array chip programmed to provide the necessary digital timing and control signals for the MX7 chips and is located close to them on the hybrid. This chip performs the same overall function as that used in μVTX1 but with many detailed changes, and in a new implementation.

The sequencer is a state machine that provides for signal sampling and readout operations, as well as a number of ancilliary functions such as calibration and adjustment of the MX7 operating voltages. It requires a minimal set of control signals and cables from the electronics hut to the detector. The new sequencer benefits from improved design implementation and optimisation, good latch-up[2] characteristics, and has an internal scan path for self-diagnosis. A redesigned state map allows a reduction in the time required for completing a capture cycle (signal sampling during the LEP beam bunch crossing), an essential feature should future LEP operation reduce the time between beam bunches.

The Local Sequencers are connected in chains of one or two allowing their associated five or ten MX7s to share an analogue readout path to a single SIROCCO channel. The sequencers have some independent control of the ladders; the control of the chains comes via the ICR card logic.

The sequencer is implemented on an ACTEL field programmable gate array [19] in unpackaged (die) form. These are n-well CMOS devices, having programmable 'anti-fuses', which are non-volatile and non-erasable, and were selected for this task as the only radiation-hard field programmable devices then available. They are measured to withstand up to 10 KGy of ionising radiation.

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[2]device failure in non-standard powering conditions

4.5   The ICR Cards

The interconnect ring (ICR) consists of seven identical rectangular multi-layer printed circuit boards (ICR cards), installed around the LEP beam pipe and forming a cylinder mounted on two support rings. The ICR is mounted as close to the ladders as possible to allow easy connection and disconnection of the flexible cables from the ladders. An ICR card buffers, distributes and controls signal flow, interconnects and filters voltages to individual ladders, amplifies the detector analogue output signals, collects many local temperatures, and transmits radiation monitoring signals.

The inner end of each ICR card has eight parallel mounted connectors, to which up to four ladders can be connected (one connector from each of the ϕ and z side hybrids). Two piggy-back analogue output signal amplifier cards, one control signal receiver card, and some SMD components are mounted in the middle of the ICR card. The outer end of the card contains a solder yard to which are connected the wires coming from four custom-built cables, which run out to the external powering and electronics systems.

The logic of each ICR card is implemented in a gate array chip, using the same device as that used for the Local Sequencer. However in this application a 44-pin PLCC package is used as there is less need to minimise the dimensions and material of the device. Only a small part of the logic modules of the chip is used but nearly all the available input/output channels are required.

One function of the gate array chip is to produce multiple copies of the chain control signals which are automatically individually inhibited if the logic power to the chain is not present. This removes any residual risk of causing latch-up in the Local Sequencer chips. The gate array chip also provides signals to each chain to allow individual control and it multiplexes the signals from each chain onto a single response line from the ICR card to the Fastbus Master Sequencer. The new ICR card logic eliminates one of the two response lines and the four enable lines needed in μVTX1, and has allowed each ICR card to have its own set of control signals.

5   Data Acquisition and Online Processing

5.1   Overview

The general layout of the digitising and readout electronics is shown in Fig. 10. The system is very similar to that in μVTX1 [2] and is again based on an OPAL VME Local System Crate [20] interfaced to a Fastbus crate. The Local System Crate controls the whole readout system and links the microvertex detector to the global OPAL trigger [21] and readout system [20]. These crates are located in one of the electronics huts just outside the OPAL detector. The analogue signals from the 30,325 active channels are digitised and preprocessed by digital signal processors (DSPs) [22] in the 14 SIROCCO Fastbus modules. A custom built Fastbus module, the Master Sequencer, steers the charge integration in all the MX7 chips (via the Local Sequencer) as well as the readout of the analogue data from the detector to the SIROCCO modules. Online processing of the data performed by the DSPs includes pedestal subtraction and cluster finding which results in a large data reduction factor.

5.2   The Fastbus Master Sequencer Module

The new Master Sequencer follows the same principles as that used in μVTX1 and is similarly packaged in a Fastbus module. This module is the central steering component of the readout system providing the overall timing and control signals needed for the front-end electronics and the digitising electronics (SIROCCOs).

The functions of the Master Sequencer include:

- a SETFLAG sequence to set flags in the Local Sequencers allowing for different modes of running;

- a CAPTURE sequence to provide the timing for the signal sampling sequence sent to the front-end electronics;

- a READOUT sequence to read out the data when a valid OPAL event trigger is generated.

- a DIAGNOSTIC READOUT sequence to allow the system to be driven in diagnostic mode so that diagnostic data can be read into the diagnostic memory.

Changes to the architecture of the Master Sequencer include increasing the number of output channels from four to eight, and using programmable delays to define the readout sequence timing used to read the data into the SIROCCOs. The readout sequence memory has been doubled and various diagnostic signals are now available on the front panel.

5.3   The Fastbus SIROCCO Modules

The Fastbus SIROCCO modules read the serial analogue data from the detector, digitise the signal from each strip, and store the data in memory. The on-board processors then perform signal processing on these stored data and transfer them to the OPAL acquisition system. Figure 11 illustrates the data flow.

Each of the 14 SIROCCO modules consists of two independent channels. Each of these channels processes the data of either the ϕ or the z side of up to two ladders (1280 MX7 channels) which are subsequently digitised by a 10-bit FADC and written to one of four front-end buffers. After data transfer is complete, the Master Sequencer writes a trigger code and the event number to the front-end queue (a FIFO memory) to assure data integrity. The front-end logic then sets one of the front-end flags, signalling the DSP to process and sparsify the data of the corresponding front-end buffer. The sparsified data are written to one of four crate-end buffers and the corresponding crate-end buffer flag is set. The data are then read out by the VME processor via a Fastbus to VME interface [23].

5.4   The VME Local System Crate

The VME Local System Crate contains two processor modules running the OS9 operating system [24]. One processor [25] is used for networking (OS9-Net, TCP/IP, NFS), histogramming, monitoring and software development. The second processor [26] handles the communication with the Fastbus modules. The Local Trigger Unit module is the link to the central trigger system. It distributes the beam crossing (BX) signal from LEP to the Master Sequencer to start the capture sequence, and when a trigger occurs, it initiates

the readout processes in the Fastbus interface processor by a VME interrupt. The data read out are transported via a VME Interconnect Module to the OPAL event builder [20].

5.5   Online Data Processing

The online processing of the raw data is performed in parallel by 28 DSPs in the 14 SIROCCO modules. Its main goal is an effective data reduction by two orders of magnitude without loss of relevant information. Details of the data processing algorithms can be found in Refs. [2, 27] for ϕ strip data and in Ref. [28] for both ϕ and z strip data. A brief description of the processing steps including the new cluster finding algorithm for the z strip data is given below.

The first processing step is the suppression of coherent noise by subtracting the mean signal of all strips read out by the same MX7 chip. Then strip specific pedestal values, which are kept in SIROCCO memory, are subtracted. A cluster search algorithm, which uses strip specific noise values (also kept in memory), marks the strips which show hits (defined below). Strips adjacent to hits are also marked for readout. The relevant data are reformatted and written to a crate-end buffer, together with the corresponding pedestal and noise values. Finally, the stored pedestal and noise values for strips without hits are recalculated and several histograms are filled which give information about suppressed data and processing performance. After every 25 events a search for noisy strips is performed.

The online cluster finding algorithm differs only slightly for ϕ and z coordinate information. In ϕ, hits are typically spread over two to three strips. The signals of two neighbouring strips are added and compared with the quadratically summed noise values of those strips. If the signal sum exceeds the noise by some factor (typically three), and if none of the strips is marked as bad, both strips are marked as hits. At wide polar angles, hits in z may be spread over up to five strips. A modified algorithm is implemented for z coordinate data which compares the sum of the signals of three neighbouring strips (rather than the two used for ϕ) with the resulting noise values.

5.6   Online processing performance

Early in the 1993 running period, some data were taken for selected ladders with no data sparsification to assess the algorithm efficiency. A Fortran version of the DSP algorithm was used to process these data offline with different parameter sets and different cluster finding algorithms. These studies verified the 100% efficiency of the online cluster finding algorithm and also showed that, for the standard parameter set run on z coordinate data, the three strip cluster finding algorithm worked better than the two strip algorithm. The better performance was due to the improved match to cluster size and to better rejection of noise fluctuations in the three strip algorithm. With the sparsification enabled the data volume was reduced by a factor of about 100.

The deadtime of the μVTX2 system for a typical 1993 OPAL trigger rate of 4–10 Hz is about 1.6 ms, which is small compared to the overall OPAL readout deadtime. The μVTX2 deadtime is dominated by the analogue readout and digitising sequence in the SIROCCO modules. Owing to the event buffering in the SIROCCO modules, the DSP processing time and the digital readout via Fastbus are not determining factors for the deadtime and studies indicate that this will continue to be the case at higher trigger rates

expected for future running. The typical DSP processing time for μVTX2 data is 15.5 ms per event. This could be further reduced to 10.6 ms by switching off histogramming and performing less frequent pedestal and noise updating.

After processing, the data are read out of the Fastbus SIROCCO modules through the Fastbus to VME interface, initiated by an interrupt from the Local Trigger Unit. Readout occurs when all DSP output buffers have their data ready. For μVTX1, the minimum time to read out one event was about 20 ms. For μVTX2, readout speed improvement was necessary to avoid it becoming a significant contribution to the deadtime. Improvements were made by reducing software overheads and by optimising code, flag handling, and other procedures, reducing the minimum time to read out an event to 9–18 ms. Thus, by software optimisation alone, the system now reads out double the amount of data in a shorter time.

6   Powering, Cooling, and Monitoring Systems

6.1   Service Systems Control

The control of the powering, cooling, and detector environmental monitoring systems is based in a VME crate (different from that of the data acquisition system) containing a processor [29], several interface modules, and two 32 channel VME ADC [30] modules as shown in Fig. 12. The processor runs under the OS9 operating system. The control hardware and detector powering system run on battery backed-up non-interruptable power supplies [31].

Power control, cooling control, and monitoring software communicate with the global OPAL Slow Controls system [32]. This allows control actions to be centralised and allows error messages to be entered into the error message utility [33] system and displayed on appropriate screens in the control room and elsewhere. A memory register in the VME cooling module is connected to a hardware system that can generate warning and alarm messages on a dedicated screen in the OPAL control room. The processor can be accessed remotely through the local area network.

6.2   The Powering System

A μVTX2 ladder requires nine different voltages which are divided into two groups. The first group includes +5 V, -5 V, and +7 V which provide the power and biasing for the MX7 chips and other digital logic. The second group provides five voltages which bias the silicon detectors: the common ladder backplane voltage and a drain and a gate voltage for each side of a ladder. The guard and drain bias lines from a ladder side are connected together at the ICR card and are both fed from the drain voltage. The detector bias voltages are individual to each ladder. The MX7 voltages are shared between two ladders, with the supplies to the ϕ and z sides separate. The power to the electronics on the seven ICR cards is provided for each card separately.

The power and bias voltages are provided by a LABEN powering system [34], which consists of 16 dual channel power supply modules. Each channel is capable of supplying the detector bias voltages to one ladder and the MX7 voltages to two ladders. In some of the modules the high-current supply voltages are used to power the electronics on the ICR cards. The LABEN system is interfaced to the detector through power interface modules

which regroup the voltages and protect detectors against overvoltages. These modules also generate the +7 V which is derived from the +5 V by an operational amplifier with a gain of 1.4. Passive networks with appropriate time constants are included in the power interface modules to ensure smooth ramp down if the input voltages are accidentally disconnected. The modules also allow detector bias currents to be measured by an ADC as a voltage drop over a known resistance in series.

The LABEN system is controlled from the processor via an RS232 interface which allows voltages and current limits to be loaded and continuously monitored by software control. This control software is split into three basic modules. The first is a program to ramp the voltages up and down with a menu-driven interface. The second continuously monitors the status of the supplies, the output voltages, and currents. The read values are stored in OS9 memory modules. The third can be called by other programs to perform an emergency ramp down. Overcurrents, voltages that are out of tolerance, or failure of the reference power supplies for the power interface modules lead to an automatic ramp down under software control. Such a ramp down is also initiated by a mains power failure or by a detector overtemperature alarm condition.

During early operation, some ladders exhibited high leakage currents after radiation incidents (see Sec. 8.2). A standby powering mode was introduced in which the backplane bias was set so that there was effectively no depletion voltage applied to the detectors. The standby mode was active within a running period outside data taking, for example when LEP beams were being prepared. The use of this standby mode eliminated the leakage current problems.

6.3   The Cooling System

About 60 W of electrical power is dissipated on the 25 detector ladders coming primarily from the MX7 chips mounted on the ceramic hybrids. This heat is conducted by the BeO hybrid substrates to the central aluminium support plate and then to the cooling ring via the two fixing screws threaded into the ring. Tests show a temperature drop of 7° C between the hottest point on the hybrid and the middle part of the cooling ring, and a further drop of 1.6° C between the ring and the circulating (60 l/hr) cooling water. The cooling water is in a closed circuit which passes outside the OPAL detector to be cooled by two heat exchanger modules and circulated by a small magnet-coupled gear pump. Water temperature is regulated electrically by means of Peltier elements [35] mounted between heat exchanger plates. With the primary cooling water kept at 16° C, the maximum cooling power available is 200 W at a 5° C temperature difference. The cooling system control electronics are interfaced to a VME module that is controlled and monitored by the processor. Water pressure, temperature and flow rate are continually measured and monitored.

The procedure for ramping the power up and down includes switching on and off cooling as needed to stabilise most quickly the temperature of the detector. In equilibrium conditions, a temperature difference of about 3° C exists between the two ends of the 180 mm long detector portion of the ladder. The power to the detector is ramped up about two hours before the start of a LEP run period to ensure stable temperature conditions for data-taking, and is ramped down only at the end of that period. Typical temperatures on a ladder during data taking are about 27° C next to the MX7 chips and about 24° C at the detectors.

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Initial problems with the growth of algae in the secondary cooling circuit in μVTX1 has been successfully eliminated by using only distilled water in the circuit. In addition, the oxygen content of the water is kept low by continuously bubbling nitrogen gas through the water in the cooling circuit reservoir.

6.4   The Temperature Monitoring System

Temperatures around the μVTX2 detector are monitored by thermistors. Each hybrid contains a thermistor close to the MX7 chips. The thermistors on the ϕ and z side hybrids on a ladder are connected in parallel and also the thermistors of two neigbouring ladders are often put in parallel. A total of 14 temperature readings are taken on the hybrids. Two thermistors measure temperatures on the cooling ring, three measure the temperatures of the LEP beam pipe along the cable trays, two measure the cooling water temperature just before and after the heat exchange modules, and four measure ladder temperatures at different positions on two ladders.

The thermistors are biased from a dedicated VME module and their voltages are digitised by the ADC module and monitored by the processor. Temperatures are measured to a precision better than 0.05 °C. In the event of overheating, a warning is first issued in the control room. If the temperature continues to rise, then power to the electronics is automatically ramped down by the software.

6.5   The Radiation Monitoring System

Four 9.5 mm $\times$ 9.5 mm $\times$ 400 μm radiation monitoring sensors are attached to four of the seven ICR cards. These measure radiation close to the beam pipe coming from the LEP machine in the horizontal and vertical planes. The sensors are semiconductor photocells [36] which were calibrated with a Cs^{137} source before installation. Radiation induced currents in these sensors are amplified and converted to a frequency in special amplifiers mounted on an interface panel just outside the OPAL detector. The frequency signal is transported to the electronics hut, where it is converted into a voltage in a custom-built module. This voltage is then digitised by the ADC module and the values are monitored by the processor. The radiation monitoring system can record levels of ionising radiation up to 1.6 Gy/h at a resolution of 0.0001 Gy/h.

High radiation levels result in warnings and alarms in the OPAL control room. Although the CMOS electronics on the ladder hybrids have greater radiation tolerance when unpowered, the voltages are not ramped down because these radiation bursts are of too short a duration to ramp down the voltages in a safe way. During LEP operation in 1993 the total radiation dose measured by the monitors was about 0.3 Gy for the horizontal and lower vertical directions and about 1.0 Gy for the upper vertical direction. The monitors are largely insensitive to the low level (mostly synchrotron) radiation which is always present when beams are circulating. The added contribution to the total dose from this source is estimated to be about 0.5 Gy from the number of hits recorded in μVTX2 data for random beam crossing events.

6.6   Gas Flow and Humidity Monitoring System

The microvertex system is kept in a dry nitrogen atmosphere by flowing nitrogen into the sealed volume containing the detector. As the seal is not completely hermetic, a slight

overpressure is maintained to reduce outside air seeping into the volume. A sensing tube is used to bring a small amount of the gas from the volume to an oxygen monitor and a humidity monitor. A water sensing device is also installed in the detector volume to warn of cooling water leaks. In normal running conditions, the relative humidity at the detector is less than 10% and the oxygen content less than 1%.

7 Offline Processing and Software Alignment

The offline processing of μVTX2 data is performed within the framework of the standard OPAL reconstruction [37] and detector simulation [38] programs. The microvertex detector pattern recognition consists of a cluster finding algorithm and the transformation of those clusters into hit positions in the OPAL coordinate system. The hits are then associated to tracks which have already been reconstructed in the central tracking chambers and finally included in an overall track fit. A software alignment procedure is used to obtain optimum geometrical position reconstruction for detector hits. The detector simulation programs have been modified to take into account the addition of the z coordinate information as well as the slightly different material distributions.

7.1 Cluster Finding

The offline cluster finding algorithm for μVTX2 is similar to that of μVTX1 [2]. The data available offline are the pedestal-subtracted pulse heights calculated by the DSP that pass the online cluster selection criteria (Sec. 5.5). The offline cluster finding is performed separately in ϕ and z. A ϕ cluster is required to have at least one strip (the 'seed') with a pedestal-subtracted pulse height of more than 4σ, where σ is the rms noise of the individual strip. One adjacent strip on each side of the seed strip is included in the cluster if its pulse height exceeds 2σ. In the case of a z cluster an allowance is made for particles traversing the 250 μm of the detector at a wide angle and therefore up to two neighbouring strips on each side are included in the cluster if their pulse height exceeds 2σ.

The particle impact points at the ϕ and z detector mid-planes are determined from the mean of the cluster strip positions weighted by their pulse heights. The ϕ and z impact points are then converted into hit positions within OPAL and result in one ϕ and three z hits, allowing for the three-fold z ambiguity due to the shared z readout for the three detectors on each ladder. The error assigned to each hit is the quadratic sum of the ϕ or z intrinsic resolutions, allowing for a dependence on polar angle in z, and the overall alignment uncertainties (Sec. 7.3).

7.2 Hit Association to Tracks

The association of μVTX2 hits to charged tracks reconstructed in the OPAL vertex, jet and z drift chambers is carried out independently for ϕ and z hits using a method similar to that used for μVTX1 [2]. Hit pairs (one from the inner layer, one from the outer layer), are associated to tracks only if their absolute and relative positions are consistent with the track extrapolation within specified tolerances. Single hits can be associated in cases where geometrically only one layer could have provided a coordinate. An iterative procedure is adopted whereby in early iterations only good quality tracks are considered

and the candidate association must be unique. In subsequent iterations poorer quality tracks and potentially ambiguous associations are treated.

Hit association in z is potentially more problematic than in ϕ owing both to the poorer resolution in z for charged track reconstruction in the OPAL drift chambers and to the three-fold ambiguity in the position of each z hit. However, for the majority of tracks with z drift chamber hits associated, the track polar angle (θ) is measured to millirad precision. Thus, although the absolute position of the track extrapolation at the microvertex detector coming from the central tracking chambers is known to only about 1 mm, the relative z positions of the track at the inner and outer layers of the detector can be determined to a precision of typically 30 μm.

The quality of the track-hit association in ϕ and z is illustrated in Fig. 13 which shows the reconstructed μVTX2 hits and the track extrapolation error ellipses for two ladders (one from each layer and with large geometrical overlap) in a typical multihadron event. The ladders shown in Fig. 13 have a hit multiplicity somewhat higher than average. The azimuthal segmentation of the detector into discrete ladders is important for the z hit association as it reduces the number of track-hit combinations to consider. For the event shown in Fig. 13, even for the inner or the outer layer alone, the hits can be matched unambiguously to the extrapolated tracks. In addition, the precise relative positioning of the hits in the inner and outer layers about the track extrapolation is used to suppress false associations. The spacing of the three-fold ambiguous hits in z is sufficiently large that it usually does not represent a significant problem.

7.3   The Software Alignment Procedure

The alignment of the microvertex detector array is determined using an extension of the procedure developed for μVTX1 [2]. The alignment is carried out in two stages. Initially, a set of global alignment constants which corresponds to the overall movement of the detector array with respect to the other OPAL tracking components, is determined. Then a set of local constants, which allow for variations of the relative positions of the ladders and of the detector wafers within the array, is optimised. The latter procedure is intended to absorb space-point reconstruction biases due, for example, to the clustering algorithm or incomplete depletion of the silicon wafers, in addition to true alignment effects.

The global alignment constants for ϕ and z are determined using a sample of dilepton events. The constants are obtained by minimising a chi-squared formed using the residuals between tracks reconstructed in the other OPAL tracking components with associated microvertex detector hits. The normalised residuals are determined for both the $r-\phi$ and $s-z$ projections[3] and combined linearly to form the chi-squared.

The local constants are initially determined from a metrological survey prior to the insertion of the detector into OPAL. The survey provides precision measurements of the relative positions of the wafers within ladders together with the ladder positions determined from the aluminium support rings. The alignment optimisation procedure uses both dilepton events and multihadronic Z^0 decays. In dilepton events the two back-to-back tracks are generally highly collinear. The relative positions of opposite pairs of overlapping ladders can therefore be constrained by performing a three dimensional helical fit to the microvertex detector hits. The curvature of the helix is constrained by the

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[3]s is defined as the arc-length in the $x-y$ plane along a reconstructed track measured from the point of closest approach to the vertex.

measurement in the OPAL jet chamber. In multihadronic Z^0 decays higher statistics and a more general constraint are obtained by requiring that all tracks share a common vertex. Tracks inconsistent with a common vertex due to heavy flavour decays for example, are removed iteratively until a satisfactory vertex is obtained. In both techniques the resulting constrained residuals are used iteratively to improve the alignment constants.

8   Performance

The new microvertex detector was installed in OPAL in March 1993 and has taken data throughout the 1993 LEP run. Using knowledge of the intrinsic detector precision from beam test studies and the alignment procedure already described, it was possible to have data available for initial physics studies at an early stage.

8.1   Single Hit Resolution

Back-to-back ladders, identical to those used in OPAL, were tested in a 5 GeV pion beam. The test beam apparatus consisted of three back-to-back ladders each separated by 15 mm. Hit positions were determined for each side of each ladder providing three ϕ and three z coordinates in total for a given track. The residual distribution of the hit position in the middle ladder with respect to the line joining the hits in the outer two ladders was obtained after alignment. The effective single hit resolution was determined from this distribution assuming identical resolutions in the three ladders for each coordinate.

The test beam measurements demonstrated that intrinsic resolutions close to 5 μm in ϕ and 13 μm in z were achieved for particle trajectories normal to the plane of the detectors (Fig. 14). Measurements with the beam oriented at different angles to the ladders were made to simulate the effect of tracks with varying polar angles in the experiment. The results of these studies showed that, as expected, the resolution in ϕ was unchanged as a function of polar angle. The resolution in z was found to degrade to about 15 μm at 30° and further to about 20 μm at 45°. Such a degradation is expected for two reasons: dilution of useful charge division information as the charge deposition extends over many strips and more non-uniform charge distributions in the cluster caused by more frequent occurrences of delta-ray electrons due to the extra material traversed.

8.2   Operational Experience

The commissioning of μVTX2 was completed rapidly, allowing routine data taking immediately at the start of the 1993 LEP physics running period. In general, the hardware and software systems in μVTX2 performed well, with the data taking efficiency with respect to the OPAL experiment as a whole being very close to 100%. However a few problems were encountered in the operation of μVTX2. One ladder suffered an open circuit on its backplane bias line that occurred about two weeks into the data taking thus rendering inactive all the channels in this ladder. The cause of this failure was a previously damaged bias line on the pitch adaptor changing from marginal contact to open circuit. Also, some ladders have shown significant increases in their leakage currents that were clearly associated with beam related radiation from LEP. These increases, although large, did not reach the point of degrading the quality of the data and may be due to radiation induced charge accumulation near detector guard rings. As noted in Sec. 6.2, this effect

has been prevented by having detector bias on only when the experiment is taking data with stable beam conditions (e.g. not during the beam setup phases when much of the radiation occurs).

8.3 Signal to Noise and Detection Efficiency

The peak of the distribution of the signal to noise (S/N) ratio[4] for all ϕ and all z readout channels is 24 and 20, respectively, as seen in Fig. 15. These results were obtained using Z^0 decay events from the 1993 LEP run. The slightly lower result for z with respect to ϕ is expected owing to the additional z channel noise contribution coming from the capacitance of the z-print.

The overall efficiency for detecting minimum ionising particles traversing the active area of working ladders is determined to be about 98% from dimuon events. This number is the product of the silicon detection efficiency, the fraction of good working readout channels, and the online and offline cluster finding efficiencies.

8.4 Impact Parameter Resolutions

The software alignment techniques described in section 7.3 result in an effective point resolution for μVTX2 hits of about 10 μm in ϕ and about 15 μm in z for tracks at normal incidence. An indication of how this improves the overall OPAL tracking resolution is given by the apparent separation at the interaction point of the two tracks in dilepton events, from which the impact parameter resolutions σ_{d_0} and σ_{z_0} can be derived. Using the μVTX2 information combined with the angular and curvature information from the other tracking components, a result of 18 μm for σ_{d_0} is obtained as shown in Fig. 16a. In the s-z projection, if the corresponding σ_{z_0} is determined using *only* the information provided by two μVTX2 hits, a value of about 85 μm for normal incident angle tracks is obtained, as shown in Fig. 16b. This is degraded to about 160 μm for tracks with an incident angle of 45°. These resolutions are in agreement with those anticipated from the measured point resolutions. In both ϕ and particularly z, the angular resolution, rather than the microvertex detector point resolution, is the limitation. Work is in progress to improve the calibration and alignment of the μVTX2 and the other OPAL tracking components. This should result in further improvements in tracking precision.

9 Conclusion

A new silicon strip microvertex detector has been operating successfully in OPAL since the start of the 1993 LEP run. This new detector obtains ϕ and z coordinate readout using back-to-back single-sided AC coupled silicon strip detectors. Readout of the z coordinate is routed to the front-end electronics, located at the end of the ladder, by means of a gold printed circuit on a thin glass substrate ('z-print'). The new MX7 front-end electronics chip has improved radiation hardness as well as better noise performance. The peak signal to noise ratios for minimum ionising particles as measured with Z^0 decay data in the new detector are 24 in ϕ and 20 in z. The intrinsic single hit resolutions at normal incidence are about 5 μm in ϕ and about 13 μm in z. Using the current alignment status, the values

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[4]The convention for S/N is the signal from all channels in the cluster, the noise is the average single channel noise for the channels in the cluster.

for the impact parameter resolutions are 18 μm for σ_{d_0} and 85 μm for σ_{z_0}, the latter using μVTX2 information alone.

The μVTX2 z coordinate provides major improvements in both the precision and overall quality of reconstructed tracks. Fig. 17 shows its effect in reducing the background in the K$\pi\pi$ mass spectrum by a factor of two with only a small loss of D$^+$ signal. The new detector is enhancing the OPAL potential in many physics analyses and will be particularly valuable in exploiting the wealth of data expected to be collected at the Z^0 peak in the near future. For completeness, a summary of parameters of the new OPAL microvertex detector ladders is given in Table 1 and parameters of the system as whole are given in Table 2.

10   Acknowledgements

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Ladder parameter	ϕ side	z side
Silicon thickness	250 μm	250 μm
Implant strip pitch	25 μm	25 μm
Readout strip pitch	50 μm	100 μm
Intrinsic resolution	$\approx$5 μm	$\approx$13 μm
Number of readout channels	629	584
Signal to noise ratio (peak)	24	20

Table 1: Characteristics of OPAL μVTX2 Ladders

μVTX2 parameter	value
Number of ladders/layer	11 (inner), 14 (outer)
Effective radius of layer	61 mm (inner), 75 mm (outer)
maximum $|cos\theta|$ acceptance	0.83 (inner), 0.77 (outer)
ϕ acceptance	88% (inner), 91% (outer)
Avg. material (rad. lengths)	1.5% at normal incidence
Strip biasing method	FoxFET (gated reachthrough channel)
2 coord. detection	back-to-back ϕ and z single-sided detectors
z readout scheme	gold printed circuit on 200 μm thick glass
Number of active channels	30,325
Readout chip, noise, power	MX7, 350 e + 15 e/pF, 2 mW/channel
Radiation hardness	about 500 Gy (MX7 chip)
Cooling method	water cooling
Number of good channels	$\approx$99%

Table 2: Characteristics of the new OPAL microvertex detector

Figure captions

Figure 1: Simplified schematic of an OPAL microvertex ladder. The ϕ readout side is facing up.

Figure 2: End-on view of the geometrical ladder configuration.

Figure 3: Close-up view of the corner of the z detector design. Note that one implant strip in four is read out. Details of the FoxFET biasing structure are not shown.

Figure 4: Distribution of total leakage currents for all detectors at the end of the long term test.

Figure 5: Cut-away view of the new OPAL silicon microvertex detector (μVTX2).

Figure 6: Exploded view of an μVTX2 ladder.

Figure 7: Schematic of the z coordinate signal routing using the z-print.

Figure 8: Photograph of the fully assembled microvertex detector ladder structure with its temporary assembly fixture mounted around the LEP beam pipe. The detector structure is about to be inserted into the centre of the OPAL detector.

Figure 9: Close-up photograph of a fully loaded ceramic substrate hybrid printed circuit board ('hybrid').

Figure 10: Schematic overview of the μVTX2 data acquisition system.

Figure 11: Block diagram of the major components of a SIROCCO module and the data flow.

Figure 12: Schematic overview of the powering, cooling, and environmental monitoring systems.

Figure 13: Reconstructed μVTX2 hit positions and track extrapolation error ellipses for one inner and one outer barrel ladder from a typical multihadron event. The two ladders have an almost complete geometrical overlap. The horizontal lines represent the ϕ hits and the vertical lines the z hits. Each z hit appears three times with a spacing of approximately 60 mm because of the shared z readout for the three daisy-chained detectors in each ladder.

Figure 14: Single hit resolutions obtained from test beam data taken at normal incident angle in OPAL μVTX2 ladders (a) for ϕ strips and (b) for z strips.

Figure 15: Distribution of the signal to noise ratio (a) for all ϕ readout hits and (b) for all z readout hits.

Figure 16: Distribution of the apparent separation at the interaction point of the two tracks in dilepton events (a) in the r–ϕ projection and (b) in the s–z projection for tracks close to normal incidence and using only μVTX2 information.

Figure 17: Invariant mass distributions for $K^-\pi^+\pi^+$ track candidates. (a) The upper points are obtained by reconstructing the decay vertex in two dimensions, requiring a vertex probability greater than 1% and requiring a decay length significance greater than 3σ. (b) The lower points are obtained by repeating the analysis in three dimensions and requiring at least two of the tracks to have associated microvertex z hits. The smooth curves represent fits to the D^+ signal together with the combinatorial background.