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The OPAL Silicon-Tungsten Calorimeter Front-End Electronics

B.E. Anderson[9], K. Anderson[5], A. Charalambous[9], A. Cotta-Ramusino[2], M. Dallavalle[2], H. Evans[5], A. Eyring[3], M. Foucher[6], R. Giacomelli[2], A. Giles[5], S. Gross[3], M. Guillot[4], W. Görlitz[4], R. Hammarström[4], J. Hart [4], P. Hart [5], S. Hillier[1], P. Jovanovic[1], T. Kawamoto[8], R.G. Kellogg[6], R. Lahmann[6], M. Mannelli[4], U. Mueller[3], J. Pilcher[5], Ö. Runolfsson[4], B. Schmitt[3], W. Springer[6], D. Strom[7], M. Tecchio[5], D. Wagner[5] and K. Zankel[4]

1 School of Physics and Space Research, University of Birmingham, Birmingham, UK
2 Dipartimento di Fisica dell'Università di Bologna and INFN, Bologna, Italy
3 Universität Bonn, Bonn, Germany
4 CERN, Geneva, Switzerland
5 E. Fermi Institute and Department of Physics, University of Chicago, Chicago, USA
6 Department of Physics, University of Maryland, College Park, USA
7 Department of Physics, University of Oregon, Eugene, USA
8 ICEPP, Elementary Particle Physics and Dept. of Phys., Tokyo University, Tokyo, Japan
9 Department of Physics and Astronomy, University College London, London, UK

Abstract

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Front End Electronics

B.E.Anderson [i], K.Anderson [e], A.Charalambous [i], A.Cotta-Ramusino [b], M.Dallavalle [b], H.Evans [e], A.Eyring [c], M.Foucher [f], R.Giacomelli [b], A.Giles [e], S.Gross [c], M.Guillot [d], W.Görlitz [d], R.Hammarström [d], J.Hart [d], P.Hart [e], S.Hillier [a], P.Jovanovic [a], T.Kawamoto [h], R.G.Kellogg [f], R.Lahmann [f], M.Mannelli [d], U.Mueller [c], J.Pilcher [e], Ö.Runolfsson [d], B.Schmitt [c], W.Springer [f], D.Strom [g], M.Tecchio [e], D.Wagner [e], K.Zankel [d]

[a] School of Physics and Space Research, University of Birmingham, Birmingham, B15 2TT, UK
[b] Dipartemento di Fisica dell' Università di Bologna and INFN, Bologna, 40126, Italy
[c] Universität Bonn, Nussallee 12, D-5300 Bonn1, Germany
[d] CERN, Geneva, Switzerland
[e] E.Fermi Institute and Department of Physics, University of Chicago, Chicago, IL 60637, USA
[f] Department of Physics, University of Maryland, College Park, MD 20742, USA
[g] Department of Physics, University of Oregon, Eugene, OR 97405, USA
[h] ICEPP, Elementary Particle Physics and Dept. of Physics, University of Tokyo, Tokyo 113, Japan
[i] Department of Physics and Astronomy, University College London, London WC1E 6BT, UK

Abstract

A pair of small angle silicon-tungsten (Si-W) calorimeters has been built to measure the luminosity to a precision better than 0.1% in the OPAL experiment at the Large Electron Positron (LEP) collider at CERN near Geneva. Each calorimeter contains 19 layers of tungsten (W) plates and silicon (Si) detectors, corresponding to a total of 22 radiation lengths, sampled by about 1 m^2 of detectors divided into 304 x 64 independently read out channels.

A complete electronics system has been developed, from the preamplifier up to the VME read out and control interface. It includes a fast trigger based on analogue sums.

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INTRODUCTION

Measurements of the Z^0 line shape in electron-positron annihilation at the LEP collider have already verified the Standard Model predictions for the electroweak couplings of quarks and leptons at an impressive level of precision, but the very success of the LEP program is taxing the four installed detectors to reduce the systematic errors of their measurements to remain compatible with the statistical errors inherent in samples of several million Z^0 decays. For example, measurement of the ratio between how often the Z^0 decays to neutrinos and how often it decays to charged leptons ($\Gamma_{\nu\nu}$ / Γ_{ll}) is of great interest, since it is a fundamental prediction of the Standard Model of Electroweak Interactions, free of significant QCD corrections or dependence on parameters such as the mass of the top quark or the Higgs boson.

The measurement of $\Gamma_{\nu\nu}$ / Γ_{ll} requires particularly precise measurement of the luminosity of the LEP beams. In order to approach the limiting statistical error of ± 0.04 on $\Gamma_{\nu\nu}$ / Γ_{ll} which is inherent in a sample of several million Z^0 decays, the luminosity must be known to 0.1% or better. The only practical method of measuring the luminosity at LEP is by counting the number of e^+e^- (Bhabha) pairs scattered at small (~40 mrad) angles with respect to the beam. A small-angle Bhabha detector, or luminometer, capable of 0.1% precision must not only be very efficient and background free, but must also measure the electron trajectories very precisely. A systematic error of only 13 μrad in the measurement of the inner acceptance edge corresponds to a 0.1% error in the luminosity.

The OPAL collaboration has therefore constructed a pair of highly segmented precision calorimeters using silicon solid-state detectors sandwiched between plates of tungsten radiator. The very compact Si-W design keeps the transverse size of the electromagnetic showers produced by the Bhabha electrons on the millimetre scale, and the photo-lithographic techniques used to fabricate the Si detectors themselves allow the detector geometry to be determined on the scale of microns.

This paper describes how micro-electronic techniques were used to achieve the conflicting constraints imposed by the high density of low-noise, large-dynamic range charge-sensitive preamps and the need to reduce thermal distortions of the operating detector to a bare minimum.

MECHANICS

Construction

The Silicon-Tungsten Luminometer consists of two cylindrical small angle calorimeters, encircling the beam pipe at ± 2389 mm from the OPAL interaction point. Each calorimeter is made of a stack of 18 tungsten plates, interleaved with 19 layers of silicon sampling wafers, and mounted as two interlocking C-shaped modules around the LEP beam pipe (fig.1). Electromagnetic showers, initiated by 45 GeV electrons, are almost totally contained within the 140 mm sensitive depth of the detector, which represents 22 radiation lengths (X_0). The sensitive area of the calorimeter

covers radii between 62 and 142 mm from the beam axis. The first 14 layers each represent 1 X_0, while the last 4 represent 2 X_0 per layer.

Mechanically each half calorimeter or "C" consists of 19 half-layer assemblies. Each half-layer consists of a precision machined tungsten half-disk, glued to the inner radius of a 2 mm thick aluminium support plate. The plate carries eight overlapping detector wedges and a semi-circular mother board. The 608 wedges themselves represent the heart of the detector. Each is a large thick film ceramic hybrid carrying a 64-pad Si detector, four Amplex readout chips and about 130 other electronic components.

Two 15 mm precision dowels penetrate the entire stack, including the aluminium front and rear plates, to hold the half-layers in precision alignment. Distortion of each half-layer out of a plane is limited by spacers at the inner and outer radii. Spring loaded clamps on each cooling pipe constrain the axial position of each layer. These clamps also ensure adequate thermal conductivity to the cooling water.

The two "C"s slide together on two massive brass dowels which ensure that the Si-wafers, which overlap as the detector is closed, do not violate their 300 μm clearances during assembly around the beam pipe.

Every 2nd layer is rotated by 11.25° (half the silicon wafer angle), to reduce systematic effects introduced by the physical overlapping of adjacent Si wafers in each layer.

The overall dimension of a calorimeter (two half modules) is : inner radius =57.5 mm, outer radius =370 mm and total depth =170 mm. Each calorimeter weighs about 100 kg.

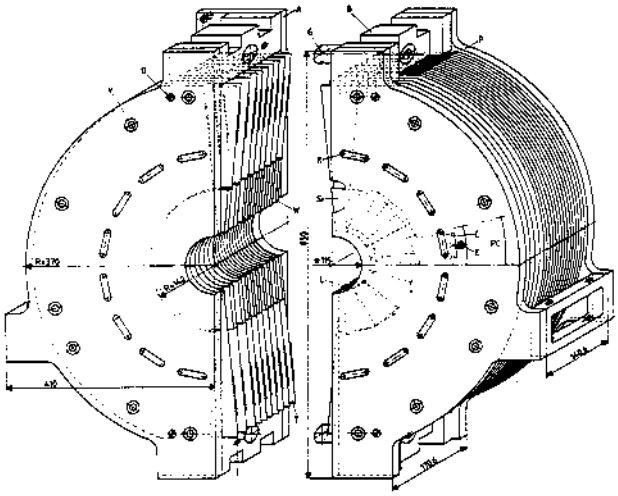

Fig. 1 Isometric view of a Silicon Calorimeter Module.

Cooling

Sixteen 3 mm water cooling pipes penetrate each calorimeter "C" at a radius of 220 mm to remove the 170 watts generated by the front end electronics as close as possible to the source. During operation 3 l/min of 16 °C water per calorimeter "C" maintains the average temperature of the half-planes at 21.5±0.2 °C, which is within 0.5°C of the mean temperature at which the detector was assembled.

Maximum temperature differences within the support plates for each layer are 2.0 °C. The resulting thermal distortion of the average detector radius has been measured to be -6±1 μm with respect to the standard metrology conditions.

The whole calorimeter was made gas tight and flushed with dry N_2 gas at room temperature to reduce humidity absorption and oxidation in the silicon wafers and unprotected semiconductor devices.

Metrology

The silicon detector assemblies (wedges) were positioned on their support plates using micro-manipulators attached to a precision rotating arm, whose axis was indexed with respect to the support plate alignment bushings. Two microscopes with graticules[#1] were also affixed to the rotating arm and set to observe photo-lithographic features on the silicon wafers themselves. The wedges were adjusted until the microscopes indicated that they were aligned radially and azimuthally, within viewing errors of about 2 μm, then screwed down to the support plate with four screws.

Completed half-plane assemblies were then lowered onto the growing calorimeter stack on a special stacking table equipped with our reference metrology instrument. This consists of two microscopes, identical to the ones described above, mounted at precise radii on an arm which could both rotate and slide axially on a precisely vertical pillar.

After the two half-planes of each layer were stacked, the two halves of the calorimeter were brought together and the radial positions of the 16 silicon wafers were measured with 2 μm precision. The absolute radius of the circle swept out by the outer metrology microscope was established as 142.031±0.004 mm including all thermal uncertainties with respect to a CERN metrological standard, and checked directly with laser interferometry.

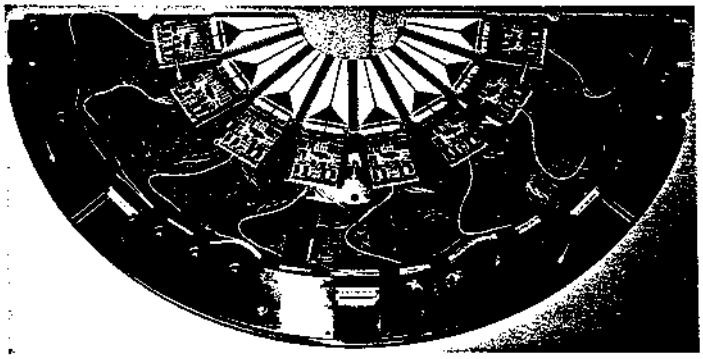

Fig. 2 One completed calorimeter half-layer, with mounted wedges and interfacing motherboard electronics.

Reference marks were glued on the inner radius of several tungsten plates to allow the motions of internal layers to be monitored after assembly and holes drilled in the front plate allowed optical access to the normal metrology references on the first layer. Final measurements were made on the modules in both horizontal and vertical positions, with and without electrical power and cooling, and also after transportation to the experimental area.

#1 Model MA113, 2μm precision microscope with incorporated ocular graticule, Marcel Aubert, CH-2501 Bienne, Switzerland

Analysis of the results shows that the relative position of any silicon wafer in the calorimeter is known to a precision of <10 μm and the rms dispersion of the radii of the 38 layers is 2.3 μm. A temperature change of 3 °C changes the wafer positions by less than 7 μm while there is no measurable change when the calorimeter is rotated from horizontal to vertical.

SILICON PAD DETECTOR

Each layer of the calorimeter contains 16 silicon wafers made by the Hamamatsu Corporation. The wafers are low conductivity n^+ silicon 310.8±1.5 μm thick in the shape of a trapezoid. The front side is implanted with a p^+ diode pattern shown in fig.3. This diode pattern is made up of 2 columns 11.25° wide in azimuthal angle and 32 rows of radial pads 2.5 mm wide. The radius of the pads extends from 62.0 mm to 142.0 mm.

Electrostatic calculations show that the sensitive region of each pad is sharply defined at the centre of the 50 μm gap between implants. A deposited layer of Aluminium, coincident with the implants, provides a visible reference for metrology. A protective layer of polyimide is then applied on the front side everywhere except on a 2x5 mm^2 section on each pad, which is used for bonding the pads ultrasonically with Al wire to the readout electronics.

A guard ring structure is implanted on the front surface of the wafer just outside the diode implants to control the surface potential outside the active area of the wafer. The back side of the silicon wafer is n^+ implanted and an evaporated gold layer is applied for back biasing the detector.

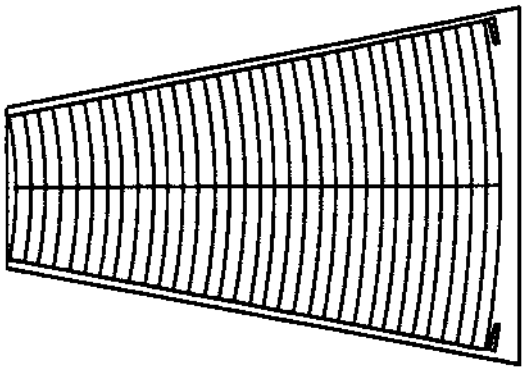

Fig. 3 Silicon wafer, having two rows of 32 pads each.

After receiving the detectors from the manufacturer each wafer was tested, in an automatic test station, to determine its leakage current and depletion voltage. The leakage current must be ≤100 nA/pad to insure the front end amplifiers operate within specifications.

The average leakage current was about 0.7 nA/pad at 80 V bias voltage, with only one out of 785 delivered wafers not passing the specification. The depletion voltage is the voltage beyond which the capacitance does not change for an increase in bias voltage. Shown in fig.4 is a plot of $1/(\Sigma Cpad)^2$ versus bias voltage. The average depletion voltage of our wafers is 62 Volts.

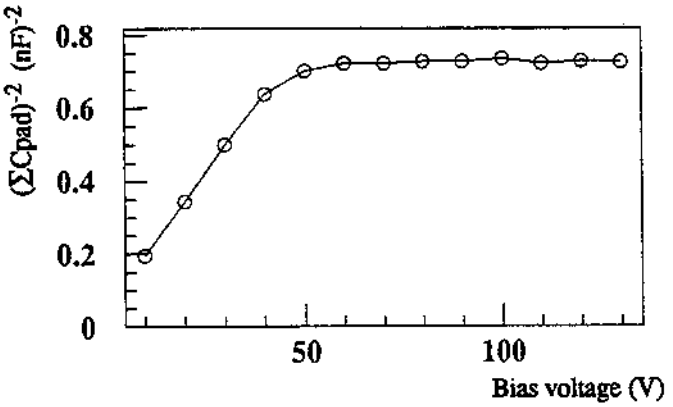

Fig. 4 Silicon detector total capacitance (ΣCpad) as a function of its depletion voltage.

The implant side of the silicon wafer was glued to the thick film hybrid using Dow Corning Q1-9226 adhesive. After experimenting with several different techniques a procedure was found such that the leakage currents did not increase after gluing.

ELECTRONICS

The OPAL data acquisition system is implemented in a VMEbus architecture [1]. The two Silicon Calorimeters are powered, controlled and read out by two identical VME based systems, housed in a counting room. Sequencer and 14 bit ADC modules [2] were developed to meet the requirements on sensitivity, resolution, conversion and acquisition speed.

Independent analogue sums from 9 odd and 9 even layers, grouped into 2 sets of 16 overlapping towers each, are used to generate fast energy triggers at each beam crossing.

Readout of the entire OPAL detector is initiated when more than 15 GeV is deposited in back-to-back calorimeter segments or when more than 5 GeV is seen in coincidence with more than 35 GeV without the back-to-back requirement. Accidental backgrounds due primarily to electrons scattered from residual gas in the LEP beam pipe are monitored by triggering the detector also on delayed energy coincidences.

LV, Bias and cooling systems have been developed for the calorimeters, which meet our needs on stability, sensitivity and flexibility. Slow controls software programs were written for run control and power down emergency actions, as well as for monitoring and logging tasks.

A radiation protection circuit which monitors the calorimeter bias currents causes a fast dump of the LEP beams if the calorimeter accidentally receives more than $3x10^8$ GeV within one second.

Signals generated in the Silicon wafers by electro-magnetic showers are amplified and stored in analogue memories in the front end amplifier chips before being read out and digitised. The entire system contains 2x19 layers of 16 wafers each, subdivided into 64 pads, which gives a total of 38'912 multiplexed signals to read out. The dynamic range of these signals extends from <1 to ~600 MIPs[#2]. The total effective

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#2 One MIP (minimum ionising particle) liberates ~23,500 electrons in the 300 μm thick silicon wafer, equivalent to an

input noise level of the installed calorimeter, including pedestal drift, is below 0.12 MIP per channel, which is equivalent to 3000 electrons at the input of the front-end chips. This noise level contributes negligibly to the resolution of the calorimeter and even allows tracking of non-interacting particles through the detector.

Functional description

The signals generated in the Si wafers are amplified, shaped, sampled synchronously every 11 μs in response to the LEP bunch crossing signal, and stored on capacitors within each Amplex chip. Signal sums from 4 Amplex outputs propagate through the multiplexer (MUX), mother board and 25 m long cables up to the trigger and data acquisition systems (DAQ). The trigger electronics (TRG) sum odd and even tower signals and discriminate them to generate a fast energy trigger output. Upon an OPAL trigger, the Sequencer (SEQ) sets up the calorimeter front end electronics for a readout, synchronising the transmission of the multiplexed signals from the front ends with the conversion and storage cycles of the ADCs. After the readout is complete, the SEQ reconfigures the front ends for trigger generation, and recommences synchronous samplings.

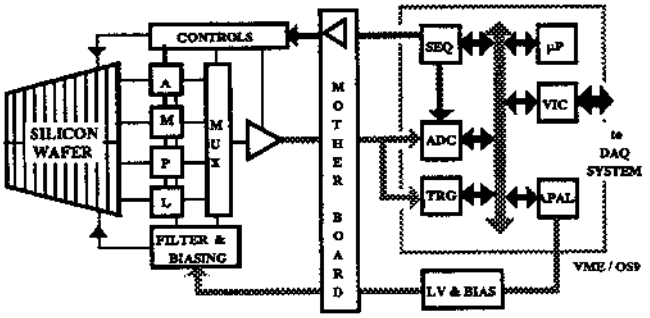

Fig. 5 Front end readout electronics, block diagram

The motherboard of each half-layer receives, level shifts and distributes all necessary digital and analogue control signals to 8 wedges. It also distributes LV and bias voltages, and collects and passes 8 multiplexed detector signals to the DAQ system. Three cables per board connect the calorimeter to the counting room electronics. Special care has been taken to avoid ground loops between the calorimeters and power and readout systems. The electronics is grounded only at the calorimeter, inside the experiment magnet.

Amplex chip

The Amplex is a monolithic analogue signal processor, fabricated in 3 μm n-well CMOS process[#3] on a die size of 4.7 x 4.3 mm. It was originally designed for the UA2 experiment in 1988 and has since been redesigned several times. The OPAL version is a minor modification of the ALEPH SiCAL chip [4,5,6]. The chip (fig.6) contains 16 identical analogue channels, each having input and shaping amplifiers followed by track and hold (T&H) buffers. Each buffer output can be connected, via multiplexed switches, to a common internal analogue bus, which drives the chip output buffer.

An input multiplexer controls the 16 input calibration capacitors (Ccal), which allow any of the channels to be accurately pulsed. The output multiplexer controls the interconnection between the T&H buffers and the chip output buffer and allows the chip to output either the sum of all channels for trigger purposes or the signal of one channel at a time during normal readout. The gain of a channel depends on the number of T&H buffers connected to the internal analogue bus [3]. Preamplifiers, shapers and buffers [4] are all designed as operational transconductance amplifiers, using folded cascode stage and stacked current mirror biasing techniques.

Low input noise figures are obtained by using a p-channel transistor in the preamp input stage with high channel w/l-ratio, which gives high g_m and low 1/f noise.

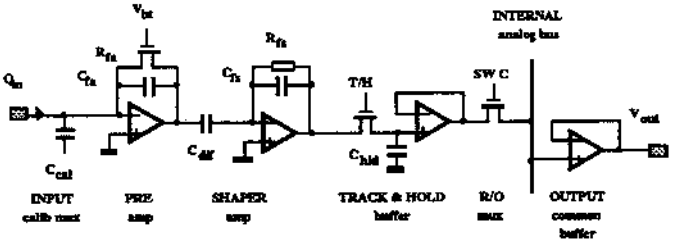

Fig. 6 Amplex chip, 1 channel block diagram.

Total inherent noise referred to the preamp input is quoted to be ~800e⁻ with a slope of 20e⁻/pF x Cpad [5]. The output voltage swing of the shaper is optimised by using n-channel type input transistors and shifted bias voltages. The swing is ≥5.8 volts and the non linearity is ≤1%.

The preamp uses a "long channel" MOS transistor as feedback element, which has two important functions :

- to keep the dc-coupled preamp at an optimal working point, almost independent of the silicon detector leakage current (<100 nA per channel)
- to discharge the signal integrating capacitor (Cfs) fast enough to avoid excessive signal pile-up.

In our design the working point (Vbt) of the MOS transistor can be adjusted remotely from the counting room.

The shaper stage works as a pole-zero cancellation circuit, which normalises the preamp pulse shape and assures fast baseline restoration. The pulse peak occurs ~ 250 ns after charge injection but is somewhat channel and detector capacitance dependent, both in time and amplitude. A typical shaped output pulse is ~500 ns wide, having a rise time of ~200 ns and fall time of ~400 ns.

The hold signal timing is adjusted to fall after the signal peak, at the point which minimises gain variation over the 16 channels in a chip (fig.7). The T&H switches are designed to give a minimum of charge injection from the hold signal onto the signal storage capacitor (Chld). Although this results in a step of only 1 mV on the output trigger signal of each Amplex, the coherent sum of these steps over the whole detector reaches the equivalent of 150 GeV, and requires the

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electrical charge of 3.8 fC. A 45 GeV electron incident on the detector generates a signal of about 3500 MIPs.

#3 IMEC vzw, Kapeldreef 75, B-3001 Heverlee, Belgium

trigger system to have a dynamic range much larger than would be required by the electron shower signals themselves.

A small rate dependence in the T&H shift causes a disturbing 11 GeV negative shift in the total trigger energy on the ~1% of beam crossings immediately following an OPAL pretrigger. Fortunately, the shift in the segment energies is a manageable 1.5 GeV.

Chip screening

Before using the Amplex chips for wedge production, it was necessary to select and calibrate them. They were delivered from the factory in the form of untested diced wafers still attached to their plastic film backing.

A fully automated probe station with microscope, probe-card[#4] and associated interfacing electronics was constructed, using x/y/z and ø-motion tables[#5] for accurate computer controlled positioning. The programming of this probe station, wafer testing and data analysis was done within the collaboration [6]. The complete testing results were stored on disk to allow final selection criteria to be established after knowing the characteristics of the ensemble. In total, 32 wafers each with 315 chips were tested and classified according to our needs.

Internal calibration capacitors (Ccal) as well as external reference capacitors (Cref) on the probe card were used for injecting a range of known charges which extended from 0 to 3 pC. The following four functional parameters were used as chip criteria:

- average internal calibration gain (Gint)
- internal trigger gain (Gtrg)
- external calibration gain (Gext)
- average internal cross-talk (Xtlk).

Gain refers here to the ratio of the Amplex output voltage change to the calibration voltage applied to the 1.8 pF calibration capacitors.

The trigger gain is measured by pulsing a single internal capacitor with all T&H buffer outputs connected to the internal analogue bus. It is ~24x (instead of 16x) lower than the single channel internal gain, which is due to negative crosstalk onto the 15 neighbour channels. In addition, the single-channel response saturates at about 2 pC input charge, half the saturation charge for the normal readout. The external gain is measured by pulsing all channels simultaneously with 16 external thick film capacitors and is used to normalise the internal gains of each chip. The variation of internal gain found in a batch of 2600 accepted chips was 2.9% (rms. of average chip gains) but by selecting similar chips in groups of 4, and trimming their average gain to a common value, this was effectively reduced to less than 1% in the completed calorimeter.

Cross-talk is measured by injecting charge, via Ccal, into one channel at a time and looking at the output response of all other channels. The average cross-talk measured is -1.8% and is virtually independent of channel position or proximity.

Cuts were made on each of the four critical quantities, averaged over the 16 channels on a chip, as well as their spreads within the chip expressed as percentages of the chip averages.

	Chip average			16 channel spread (%)		
Parameter	Min V/V	Mean V/V	Max V/V	Mean rms	max rms	worst cha
Gint	2.70	2.95	3.20	0.73	<1.5	<4
Gtrg	0.11	0.122	0.14	3.03	<6.0	<16
Gext	1.80	2.07	2.40	2.92	<5.0	<12
Xtlk	-.024	-.018	-.012	9.2	<14	—

Tab. 1 Criteria for the Amplex chip selection.

The average Amplex wafer yield, obtained with these criteria, was around 41%, where the worst wafer had only 2% and the best over 75% good chips.

The amplifier and buffer stages were biased with 1% resistors connected to -5 volts. Corresponding bias currents, measured on all good chips at ±5.0 volt nominal supply voltage, were :

Ipre=44.0±1.1μA, Isha=38.3±0.9μA, Ihld=78.0±2.7μA, Ibuf=55.4±0.9μA, Iecl=6.86±0.05μA.

The Amplex chip output signal power supply CMRR is found to be -3% for the +Vcc and +1.25% for -Vee, which has negative consequences on trigger level and signal pedestal stability (see Mother board).

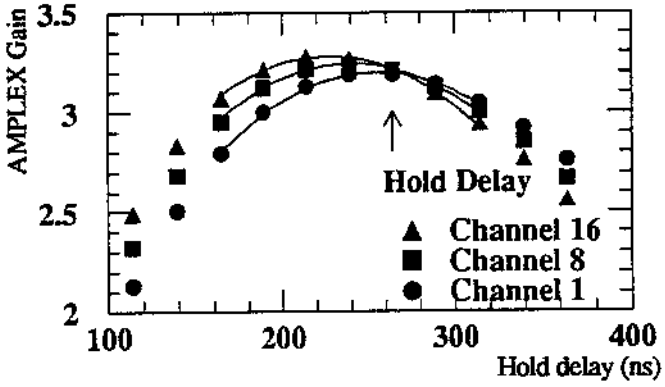

Fig. 7 Amplex chip: channels 1, 8 and 16 outputs versus T&H timing at constant calibration input voltage and 33 pF input load capacitances.

Thick Film Hybrid

To minimise the space between calorimeter layers we adopted a design in which a single circuit board carries both the silicon wafer and its associated electronics. In the completed calorimeter overlapping detector layers fit within a nominal gap height of 4.6 mm. A large thick-film hybrid built on a thin ceramic substrate[#6] carries all the electrical components plus their interconnections and bonding pads on

#4 Micro-Probe Inc, 11031 via Frontera, San Diego, CA 92127-1704, USA. Card type 70XXL 50 ohm (id: CERN43P).

#5 Modules: TL78, UE30PP and IP28, Tables: 5μm precision, Micro-Controle Electronique, F-91006 EVRY Cedex, France.

#6 Rubalit 708, Al2O3, 3"x 6", 275 μm thick, Hoechst Ceramtec, F-75015 Paris, France.

its upper surface. The anode side of the Si wafer is glued to the under side of this ceramic, with its bond pads extending beyond the ceramic's edge (fig.8). This reversal of normal hybrid geometry allows the edges of adjacent detectors to be overlapped with 300 μm clearance. An Al fixture plate is glued under the outer portion of the ceramic, beneath the Amplexes and other electrical components. This plate serves to mount the wedge on the half-layer support plate and to conduct heat away from the hybrid. A short ceramic stiffening bridge is glued between the silicon wafer back plane and a lip on the fixture plate.

The 64 silicon wafer pads are bonded[#7] to the hybrid input pads and thin lines bring the signals to the Amplex inputs. The outputs of the Amplex chips are buffered by emitter followers and connected to a multiplexer, which has 5 externally controlled switches used for trigger summing and chip output selection. Signals from a complete wafer are summed and pedestal corrected in an operational amplifier (AD848). The result is sent on a balanced shielded TWP cable to a 14 bit ADC, located in the counting room.

The effective trigger gain of each wedge is adjusted to a common value by a single trimming resistor. Amplex chips are individually biased to achieve best parameter uniformity, by means of 4 independent sets of resistors and filter capacitors.

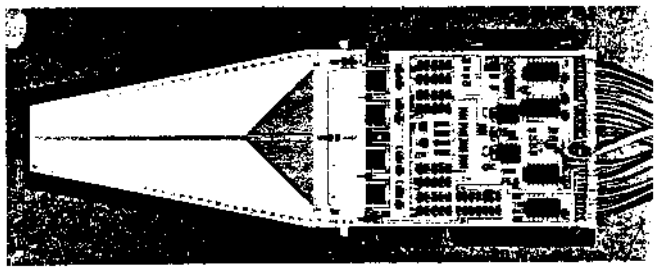

Fig. 8 Calorimeter hybrid, with detector and associated electronics, mounted on an aluminium support plate.

Calibration signals are generated onboard for checking the wedge in situ. Test charges can be selectively injected at three different places: internally on all Amplex calibration buses, externally at the Amplex inputs, and on the Silicon wafer back plane. Multiplexer and calibration switches are controlled externally via 8 digital CMOS signals and the 4 Amplex chips, driven in parallel, are controlled by an additional 9 external signals. The total hybrid power consumption is 1.0 watts, mainly dissipated in the Amplex chips.

Small standard SMD components (type 0805) and naked Amplex and transistor chips are used. On board mounted connectors were excluded to minimise the space between layers. All wires joining the hybrid to the outside world are soldered directly between the outer edge of the hybrid and two low profile 20 pin SIL connectors, which mate with connectors on the motherboard. The wires are sufficiently long and flexible to fit well in all jigs during assembly and testing of the wedge.

The hybrid contains 4 metal layers and 3 intermediate insulation layers. A small part of the first metal layer, in the vicinity of the Amplexes, is etched to obtain thin (~6μm), flat, bondable lines of well defined width. The other lines, and all insulating layers are screen printed, after the etching and thorough cleaning of the substrate. Finest pitch mesh and fine grain pastes are used on all layers.

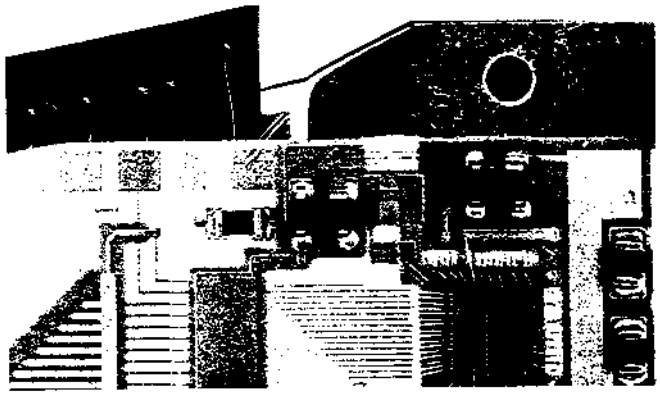

Fig. 9 Details on the wedge, showing bonds between substrate and silicon wafer, chips and stiffening bridge.

Some lines must withstand detector bias voltages with nA leakage currents and special attention was paid to the electrical insulation between layers and adjacent lines : insulation layers are always printed twice and with different masks, to reduce the defect rate due to punch-through holes.

The hybrid layout, prototyping and pre-series production were done at CERN, while series production and SMD mounting were transferred to industry. The dimensions of the hybrid is rather unusual and special tools and techniques were developed for the fabrication[#8] and component mounting[#9]. 977 bare hybrids were fabricated, and 644 were brought to completion for inclusion in the calorimeters.

The production, assembling and testing of complete silicon wedges was all done at CERN within the collaboration. The fabrication entailed 17 separate steps, including four quality assurance tests:

- visual inspection and insulation tests on the naked hybrid
- functional test after SMD mounting
- calibration test after Amplex mounting and bonding
- full test after Si wafer mounting and bonding

We found that small-batch production, coupled with rapid feedback from testing was crucial to the success of the project. Hybrid production occupied a team of 12 people over a period of 14 weeks. The peak production rate was 16 hybrids per day.

The first test included conductor resistance measurements and insulation tests between neighbouring lines and under/over lying conductors. The insulation test showed the highest failure rate and about 15% of the hybrids had ≥1 pinholes, mainly between large surface conductors, such as power lines and ground plane. Most such chorts could be eliminated in an effective and sometimes spectacular manner by discharging a 47 μF capacitor, charged to 10-100 volts, through them.

Thick film calibration capacitors, having <2% relative tolerance, are printed on top of the 64 etched input lines. They

#7 Hughes Model 2470 ultrassonic wedge bonder, using 17.5 and 25 μm aluminium wires.

#8 Ascom Favag AG, CH-2022 Bevaix, Switzerland

#9 Milpuce Electronic SA, CH-2336 Les Bois, Switzerland

are very temperature stable and used to check the long term stability of the calorimeter electronics.

The capacitance value of the 64 sector-shaped silicon wafer pads vary at full depletion voltage from 11 to 24 pF, depending on their radial position. To normalise the capacitive load on all Amplex inputs to ~28 pF, thick film compensating capacitors connected to ground are printed on top of each input line. This equalises Amplex amplification and detector signal pulse shaping in a simple and economic way.

Mother board

Eight wedges in a half-layer (fig.2) are connected to one motherboard (MB) via special cables and low profile connectors, over which all necessary signals and voltages are supplied. The MB is a C-shaped multi-layer printed circuit carrying analogue and digital control busses, LV supply and detector bias lines and associated active electronic circuits. The 8 outgoing analogue signals are transmitted over individually insulated shielded TWP cables, attached to the top of the MB.

Three cables : control, LV and bias, and analogue output connect each MB to its corresponding electronics in the counting room. Ground loops are avoided by using high impedance receivers for both digital (RS422) and analogue control signals. The control cable transports 16 signals from the Sequencer to one MB, where they are discriminated and buffered in low power ICs which drive the wedges. LV to each MB is supplied from a remote sensing power regulator module. One MB dissipates less than 1 watt which is absorbed by the temperature stabilised aluminium plate.

Due to the poor power supply CMRR of the Amplex chips and the large number of channels summed in the trigger, sensitivity to dynamic changes in supply voltage becomes critical. A circuit was included on the MB to compensate for these variations by injecting a common correction signal into the analogue summing points of the eight hybrids.

CALORIMETER PERFORMANCE

The two silicon-tungsten calorimeters were installed in OPAL at the beginning of the 1993 LEP run. Prior to the installation, valuable experience was gained by operating a partial calorimeter in a test beam run during the summer of 1992 [7]. Several parameters, important to understanding the final detector, were directly measured. Possible local hardening effects [8] due to the relative positioning of silicon and ceramic material in the calorimeter was found to be <3.9% at the 90% confidence level. Systematic shifts in reconstructed pad boundary positions, due to the curved pad geometry used on the silicon wafers, were measured at 4, 6 and 8 X_0. The shift at 4 X_0 was measured to be 8.0±2.5 (stat.) ±5.5 (syst.) μm.

During the 1993 data taking the individual pad gains have been stable to 0.3% over periods of weeks. The pad-to-pad gain uniformity, expressed as the ratio between the gains of adjacent pads, was 0.6% rms. Only 2 of the 608 wedges have become defective subsequent to installation. A single pad was lost due to radiation damage before the beam dump interlock was installed. The high degree of redundancy in the detector allowed us to compensate for the 0.3% of defective channels using the properties of longitudinal shower development. Studies of well contained Bhabha events show that the energy resolution is consistent with expectations, $\sigma E/E = 25\%/\sqrt{E}$. The radial position resolution for individual electron showers, is found to be ±0.2 mm.

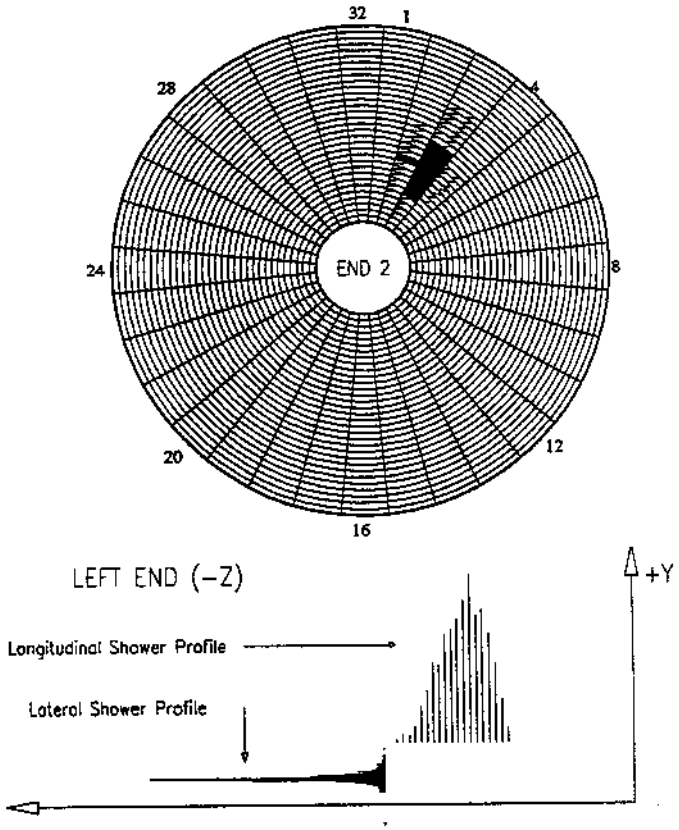

Fig. 10 Typical shower profiles in the left calorimeter.

COSTING

A first cost estimation was done in conjunction with the proposal in September 1991 and a second after project completion in May 1993. The final costs were within the projection and distributed as follows :

ITEM	QTY	PRICE	price
	units	Sfr / unit	Sfr / ch
Silicon wafer	608	650.	10.16
Equipped Hybrid	608	405.	6.32
Mechanics, sets	4	50,848.	5.23
Trigger and DAQ systems	2	91,455.	4.70
Interconnections	76	2,217.	4.33
Power and Bias modules	76	746.	1.46
Cooling systems	4	2,185.	0.22
TOTAL COST	Sfr =>	1,261,042	

Tab. 2 Cost breakdown of two completed Si-Tungsten Calorimeter modules, per unit and per Si-pad (in total 38912 analogue channels).

The whole project and practical work was proposed, initiated, scheduled and performed by the authors themselves, who also wrote specifications for, and negotiated with external firms. Institute workshop and hired manpower costs are included in the calculations as well as services executed by industry.

CONCLUSIONS

Two small-angle high precision, compact Si-W calorimeters were built and put into operation in the OPAL experiment in a very short period of time. They are used to measure the luminosity at LEP by counting the number of e^+e^- (Bhabha) pairs scattered at small angles with respect to the beam.

The calorimeter is made of a stack of 18 tungsten plates, interleaved with 19 layers of silicon sampling wafers, and mounted as two interlocking C-shaped modules around the LEP beam pipe. The very tight tolerances on the calorimeter geometry forced us to construct special tools for the precision adjustment of various components and for the assembly of complete modules. The rigidity and thermal stability of the calorimeter mechanics assures that the position of each Si wafer is known to better than 10 μm.

The very limited space available inside the calorimeter demanded inventive solutions for the electronics, ensuring low power consumption, high stability and reliability. A large size thick film hybrid was developed carrying both the silicon detector and electronic components. The effective electronics noise in the ~39,000 channels is below 0.12 MIP and signals up to 1000 MIPs are amplified linearly. The digitised silicon pad detector signals allow us to determine the radial positions of individual 45GeV showers in the calorimeter with a precision of ±0.2 mm and their energies with a precision of ±4 %.

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