

# The Questions of Circuitry Design when Forming the Switching Functions of the Control System of the Matrix Frequency Converter

Andrei Vladimirovich Bondarev<sup>1</sup>, Sergey Vitalyevich Fedorov<sup>1\*</sup>, Elena Aleksandrovna Muravyova<sup>2</sup>, Ramil Rimovich Kadyrov<sup>2</sup> and Ekaterina Anatolyevna Shulaeva<sup>2</sup>

<sup>1</sup>Kumertau Branch of Orenburg State University, Russian Federation

<sup>2</sup>Ufa State Petroleum Technological University, Russian Federation;  
proinfosystem@gmail.com

## Abstract

The switching function generator of the matrix frequency converter control system is described. This device can be used in the control systems of frequency-controlled AC drives and special consumers. The output voltage of the matrix frequency converter is generated by this device on the principle of amplitude modulation of the reference sinusoid by steps that are formed from the twelve-phase input voltage sections. The described device enables to generate the output voltage in the range from extremely low frequencies up to the frequency of 150 Hz. At the same time in the low frequency region up to 15 Hz the total harmonic distortion of output voltage complies with the value specified in GOST 13109-97. The frequency range above 15 Hz requires the use of pulse-width modulation to shift the higher harmonics to the high frequency region. The device design consisting of individual identical blocks allows simplifying the manufacturing process, and applying modular technology in the manufacture and maintenance of the device itself and the entire control system in general.

**Keywords:** Amplitude Modulation, Harmonic, Matrix Frequency Converter

## 1. Introduction

Now the majority of technological processes are carried out by means of electric drives which are the main consumers of the electric power in many industrialized countries. The latest technologies allow applying the automated control systems enabling to lower considerably the electric power costs due to optimization of productions, and also to ensure trouble-free operation of the electric drive mechanism for these purposes. The greatest distribution was gained by alternating current frequency and adjustable electric drives. The main device providing frequency regulation of the electric drive is a frequency converter.

When designing Frequency Converter (FC) the main criteria are the quality of output voltage, price and mass-

dimensional indicators. In spite of the fact that the state standard specification and the international standards provide a number of the electric power quality criteria, the basic one is a spectral criterion – voltage waveform distortion factor<sup>1</sup>.

As a result of electric drive voltage non-sinusoidality, the highest positive-sequence harmonics create useful torque, the negative-sequence ones create retarding torque, and zero sequence ones generate the pulsing field. They cause additional losses in the electric motor, the electrical machine overheating, decrease in the torque, very strong hindrances in the power line.

To improve harmonious structure of output voltage in frequency converters either the power scheme, or algorithm of control system modulation, or both are changed.

\* Author for correspondence

These circumstances stimulate use of input filters in their structure which partially solve the problems noted above, but thus increase the cost and worsen mass-dimensional and dynamic indicators. Therefore, the issues of FC harmonization with a power line are especially noteworthy. In addition to the requirements for the consumed electric power quality, modern FC also should provide possibility of energy recovery in the power line.

One of the promising directions for reducing consumption of wattless power of the power line with simultaneous possibility of energy recovery and decrease in the level of the network current highest harmonics is application of the Matrix Converter (MFC) schemes using completely controlled switches in their scheme. Development of modern element base and new technical capabilities gave an impetus to the development of the new principles of control, unrealizable in view of the complexity earlier. All this makes it possible to develop control systems, enabling to lower the harmonic distortion factor of the FC output voltage.

The research objective is to reduce output voltage harmonic distortion factor of matrix frequency converters based on the development of the generator of switching functions of the control system with amplitude modulation.

## 2. Literary Review

The switching function generator is a basic element of the control system applied both in the Direct Frequency Converters (DFC) in general and in DFC of matrix type in particular. The task of this device is to generate switching functions, the representing pulse signals accepting values 1 or 0. In modern control systems the switching function generators have a similar structure consisting of three identical channels. The comparison element is a basis of these channels. Operation of the generator is based on comparison of the modulating and synchronizing signals according to a certain algorithm.

The design of the modern device, as well as the algorithms of switching functions generation based on comparison of signals does not allow obtaining voltage at the output of the Frequency Converters (FC) with the required value of harmonic factor. In turn development of modern electronic components led to emergence of the new principles of control which could not be realized until recently. This makes possible to develop the control systems, enabling to lower output voltage harmonic distortion factor voltage.

Works of such scientists as G. G. Zhemerov, R. P. Kartashov, A. K. Kulish, E. M. Chekhet, E. E. Chaplygin, D. Casadei, G. Grandi, G. Serra, A. Tani, L. Gjugyi and B. R. Pelly are devoted to the investigations in this field.

Now the majority of technological processes are carried out by means of electric drives which are the main consumers of the electric power in many industrialized countries. The latest technologies allow applying the automated control systems enabling to lower considerably the electric power costs due to process optimization, and also to ensure trouble-free operation of the electric drive mechanism for these purposes. AC variable-frequency electric drives became the most widespread currently. Frequency converters used in their operation are divided into two groups:

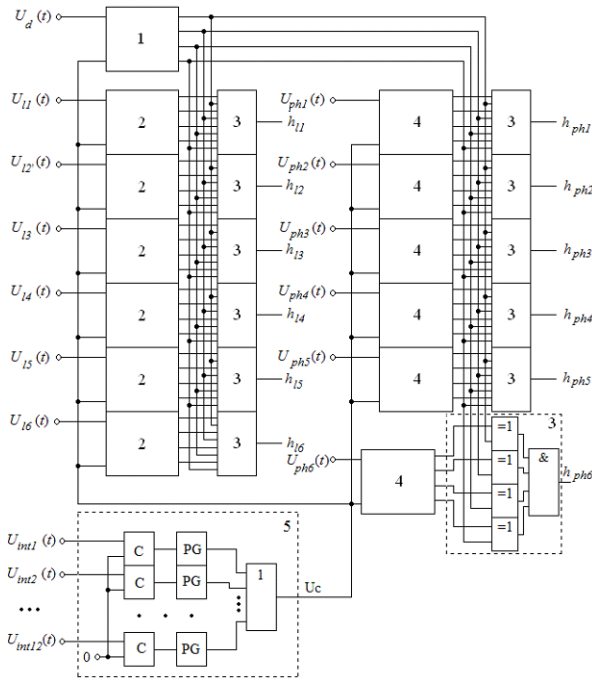
- Indirect Converters (IFC) where the first unit is the rectifier having an input filter, and the independent inverter acts as the second unit. Thus, there is a double conversion of the electric power. Units are controlled independently from each other as power consumption is identical for the inverter and the rectifier. Between the main units of IFC an intermediate DC element is installed which stabilizes instant value of input and output power difference, accumulating electric energy. This promotes significant increase in wattless power indicator and decrease in energy efficiency. As frequency converters of this kind are non-linear consumers of the electric power, they distort the power line, which is detrimental to the operation of the entire system and adversely affects external environment.
- Direct Frequency Converters (DFC) carry out single power conversion. There is no need for intermediate accumulation of power during operation of such converters. The most promising development of DFC is the Matrix Frequency Converter (MFC).

The recent inventions in the field of FC production allow reducing overall dimensions of these devices with improvement of technical characteristics and without considerable switching loss. The most advanced method for reducing wattless power consumption and ensuring energy recovery is use of active frequency converters. These FCs are controlled by pulse and modulation or relay methods.

## 3. Method

The objective is solved by the switching function generator of the matrix frequency converter control system (Figure 1.) with the power scheme on the basis of the three-

phase-to-single-phase converter. The FC power scheme contains the main first–sixth fully controllable switches having bilateral conductivity with three-phase bridge connection, its input being connected to phase wires of the three-phase alternating current main via reactors, and output – to the load, and the additional seventh and eighth fully controllable switches with bilateral conductivity<sup>4</sup>.



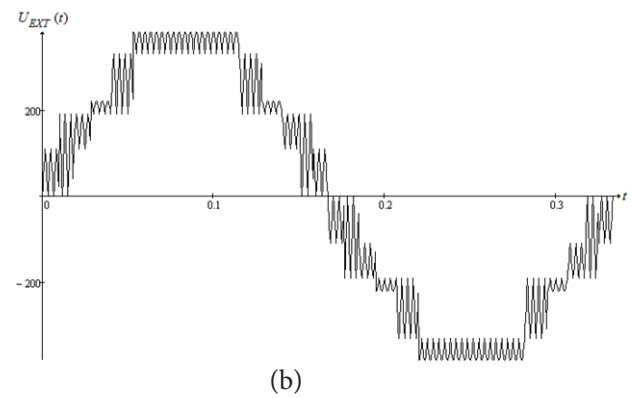
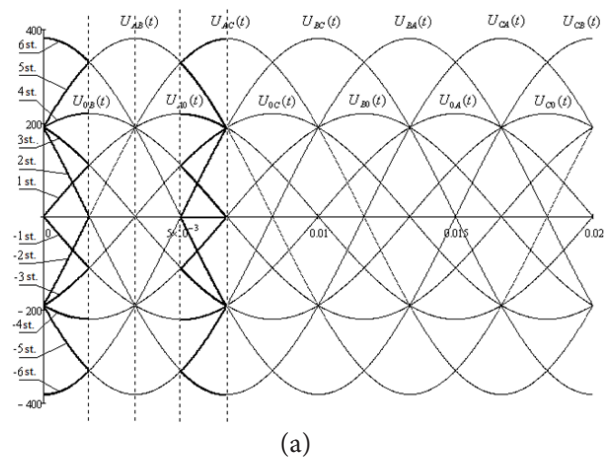
**Figure 1.** The switching function generator of a MFC control system with amplitude modulation-based algorithm.

The switching functions  $h_{11}, h_{12}, h_{13}, h_{14}, h_{15}, h_{16}, h_{ph1}, h_{ph2}, h_{ph3}, h_{ph4}, h_{ph5}, h_{ph6}$  are the output of the switching function generator of the MFC control system. Value of any of these functions is equal to 1 if the four-digit code of the set step at the output of the modulating signal quantization and record block (the Block 1 in Figure 1.) coincides with the four-digit code of the identified step (created by any input voltage) at the output of one of the phase voltage quantization and record blocks (Blocks 4 in Figure 1.) or of linear voltage quantization and record blocks (Blocks 2 in Figure 1). Thus, this switching function unlocks the corresponding power switches which connect the corresponding input voltage to the frequency converter output. All other switching functions are equal to 0<sup>2</sup>.

The output voltage of the frequency converter is formed by the principle of amplitude modulation of a reference sinusoid by the steps received from sections of 12-phase voltage with duration equal to the sampling

period  $T_d$ . Time between crossing zero value by any of 12 phases of is accepted as the sampling period  $T_d$ . Sampling time  $T_0$  makes the value equal to, where  $T_0/12$ , is  $T_0$  the input 12 phase signal period.

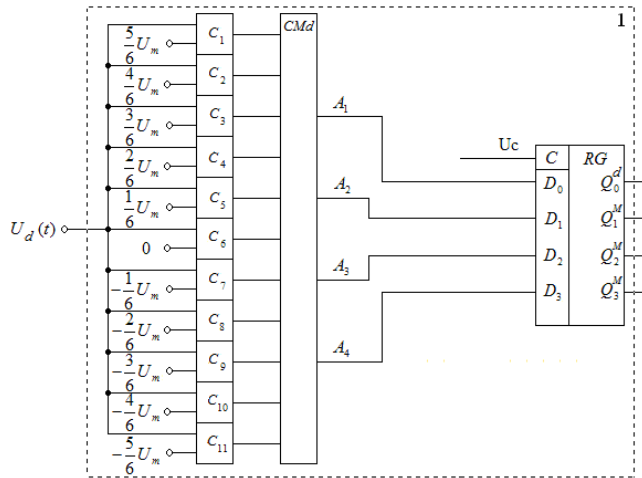
Amplitude modulation of sinusoidal voltage is carried out by 6 positive and 6 negative levels (12 levels in total). It means that output voltage will be step one with 6 positive and 6 negative steps. The choice of such quantity of steps is determined by the fact that throughout the entire sampling period  $T_d$  12 phase input voltage is presented by 12 sections with different average values (Figure 2(a)). Output voltage is shown in Figure 2(b).



**Figure 2.** The sections of 12-phase voltage input used as steps when forming output voltage (and), output voltage with a frequency of 3 Hz

The switching function generator of the MFC control system frequency converter realizing the principle described above consists of the following blocks.

The first part is a *modulating voltage quantization and record block*  $U_M(t) = U_m \sin(\omega t + \varphi)$  (the Block 1 in Figure 1). Figure 3 shows the scheme of the modulating voltage quantization and record block.



**Figure 3.** The scheme of the modulating voltage quantization and record block.

Since the number of output voltage steps is equal to 12, the number of quantization levels is also equal to 12.

A scheme consisting of 11 voltage comparators is used as a device realizing this quantization ( $K_1, K_2, K_3, K_4, K_5, K_6, K_7, K_8, K_9, K_{10}, K_{11}$ ). Each comparator is adjusted on a certain level of input voltage so that the output signal changed from 0 to 1 every time when input voltage exceeds the set level.

Since the number of output voltage quantization levels totals to 12, 4-digit code ( $2^4 = 16$  values) is required to code them. Therefore at the output of comparators it is necessary to synthesize the coding device  $CM_d$ . This device has to convert 11-digit code from the output of comparators in 4-digit one, i.e., have 11 inputs and 4 outputs. The equations of the coding device  $CM_d$  in the form of PDNF<sup>3</sup>:

$$A_1 = \bar{K}_1 \bar{K}_2 K_3 K_4 K_5 K_6 K_7 K_8 K_9 K_{10} K_{11} + K_2 K_3 K_4 K_5 K_6 K_7 K_8 K_9 K_{10} K_{11}$$

$$A_2 = \bar{K}_1 \bar{K}_2 \bar{K}_3 \bar{K}_4 \bar{K}_5 \bar{K}_6 K_7 K_8 K_9 K_{10} K_{11} + \bar{K}_1 \bar{K}_2 \bar{K}_3 \bar{K}_4 K_5 K_6 K_7 K_8 K_9 K_{10} K_{11}$$

$$A_3 = \bar{K}_1 \bar{K}_2 \bar{K}_3 \bar{K}_4 \bar{K}_5 \bar{K}_6 \bar{K}_7 K_8 K_9 K_{10} K_{11} + \bar{K}_1 \bar{K}_2 \bar{K}_3 \bar{K}_4 K_5 K_6 K_7 K_8 K_9 K_{10} K_{11} + K_2 K_3 K_4 K_5 K_6 K_7 K_8 K_9 K_{10} K_{11}$$

$$A_4 = \bar{K}_1 \bar{K}_2 \bar{K}_3 \bar{K}_4 \bar{K}_5 \bar{K}_6 \bar{K}_7 \bar{K}_8 K_9 K_{10} K_{11} + \bar{K}_1 \bar{K}_2 \bar{K}_3 \bar{K}_4 \bar{K}_5 \bar{K}_6 K_7 K_8 K_9 K_{10} K_{11} + \bar{K}_1 \bar{K}_2 \bar{K}_3 \bar{K}_4 K_5 K_6 K_7 K_8 K_9 K_{10} K_{11} + \bar{K}_1 \bar{K}_2 \bar{K}_3 K_4 K_5 K_6 K_7 K_8 K_9 K_{10} K_{11} + \bar{K}_1 \bar{K}_2 K_3 K_4 K_5 K_6 K_7 K_8 K_9 K_{10} K_{11} + \bar{K}_1 K_2 K_3 K_4 K_5 K_6 K_7 K_8 K_9 K_{10} K_{11} + K_2 K_3 K_4 K_5 K_6 K_7 K_8 K_9 K_{10} K_{11}$$

These equations are realized by means of digital circuitry engineering methods<sup>3</sup>.

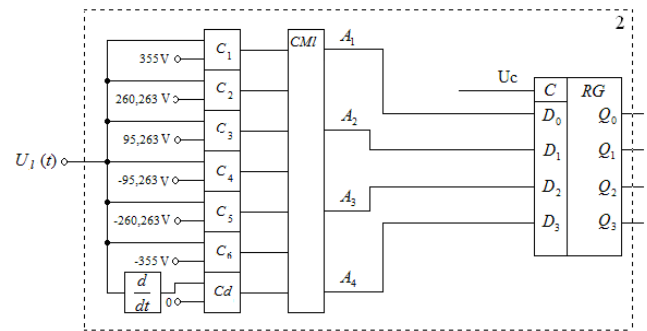
The operating principle of this system is as follows. Input twelve-phase voltage (on the scheme,  $U_{in1}(t), U_{in2}(t), \dots, U_{in12}(t)$ ) is supplied on the synchronization block input (Block 5 in Figure 1). At the synchronization block output impulse  $U_c$  fixing zero crossing of any voltage  $U_{in1}(t) - U_{in12}(t)$  is formed. Further this impulse arrives

on the synchronizing input  $C$  of register  $RG$  of Block 1 (the modulating signal quantization and record block). At the time of this impulse arrival the binary four-digit code is recorded in the register from the output  $CM_d$ , i.e., the code of the current step of quantized voltage  $U_d(t)$  is recorded.

Further task is to define what of input voltages  $U_{in1}(t) - U_{in13}(t)$  forms this step at the given moment and, respectively, to connect this voltage to the frequency converter output. This problem is solved by the second part of the switching function generator of the frequency converter control system frequency converter which is carrying out number identification of the step formed by each of 12 input voltages.

According to Figure 2a, at the sampling moments input linear voltages form the following steps: 6, 5, 2, -2, -5, -6. Phase voltage forms the steps: 4, 3, 1, -1, -3, -4.

The next block is the linear voltage quantization and record block (Block 2 in Figure 1). The scheme of the linear voltage quantization and record block is shown in Figure 4.



**Figure 4.** Scheme of the linear voltage quantization and record block

The number of the step formed by linear voltage can unambiguously be determined by the voltage value at the time of switching and by the sign of a derivative of this voltage.

That is the identification problem reduces to determining the voltage value and the derivative sign. The value is determined by means of level quantization. Since there are 7 values of voltage, the entire range of the input signal will be divided into sections so that all these values appeared in the middle of these sections. As a result, we obtain 6 quantization levels: 355 V; 260,263 V; 95,263 V; -95,263 V; -260,263 V; -355 V.

The scheme including 6 voltage comparators ( $K_1, K_2, K_3, K_4, K_5, K_6$ ) and the speed comparator consisting of the



differentiator and the comparator  $K_A$  is taken as a device realizing this quantization. Each comparator is adjusted on a certain level of input voltage so that the output signal would change from 0 to 1 every time when input voltage exceeds the set level.

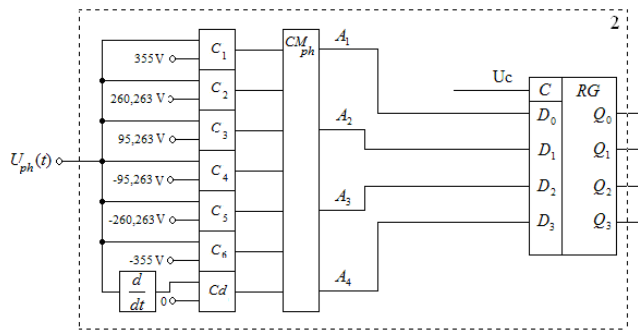
As all 12 quantization levels are coded by the 4-digit code, it is necessary to connect the device with 7 inputs and 4 outputs to the output of comparators  $K_1 - K_6, K_d$ . This coding device  $CM_l$  has to convert a seven-digit code of each step created by linear voltage to the four-digit. The equations of the coding device  $CM_l$  can be written in PDNF form as follows<sup>3</sup>:

$$\begin{aligned}
 A_1 &= \bar{K}_1 \bar{K}_2 K_3 K_4 K_5 K_6 K_d + \bar{K}_1 K_2 K_3 K_4 K_5 K_6 \bar{K}_d + \bar{K}_1 K_2 K_3 K_4 K_5 K_6 K_d + K_1 K_2 K_3 K_4 K_5 K_6; \\
 A_2 &= \bar{K}_1 \bar{K}_2 \bar{K}_3 K_4 K_5 K_6 K_d + \bar{K}_1 \bar{K}_2 K_3 K_4 K_5 K_6 \bar{K}_d + \bar{K}_1 \bar{K}_2 \bar{K}_3 K_4 K_5 K_6 \bar{K}_d + \bar{K}_1 \bar{K}_2 \bar{K}_3 \bar{K}_4 K_5 K_6 K_d; \\
 A_3 &= \bar{K}_1 \bar{K}_2 \bar{K}_3 K_4 K_5 K_6 K_d + \bar{K}_1 \bar{K}_2 K_3 K_4 K_5 K_6 \bar{K}_d + \bar{K}_1 \bar{K}_2 K_3 K_4 K_5 K_6 K_d \\
 &\quad + \bar{K}_1 K_2 K_3 K_4 K_5 K_6 \bar{K}_d + \bar{K}_1 K_2 K_3 K_4 K_5 K_6 K_d + K_1 K_2 K_3 K_4 K_5 K_6; \\
 A_4 &= \bar{K}_1 \bar{K}_2 \bar{K}_3 K_4 K_5 K_6 K_d + \bar{K}_1 \bar{K}_2 K_3 K_4 K_5 K_6 \bar{K}_d + \bar{K}_1 K_2 K_3 K_4 K_5 K_6 K_d \\
 &\quad + K_1 K_2 K_3 K_4 K_5 K_6 + \bar{K}_1 \bar{K}_2 \bar{K}_3 \bar{K}_4 K_5 K_6 \bar{K}_d + \bar{K}_1 \bar{K}_2 \bar{K}_3 \bar{K}_4 K_5 K_6 K_d.
 \end{aligned}$$

These equations are realized by means of digital circuitry engineering methods<sup>3</sup>.

Further the *phase voltage quantization and record block* follows (Block 4 in Figure 1). The scheme of the phase voltage quantization and record block is shown in Figure 5.

The number of the step formed by phase voltage  $U_{ph}(t)$  can also unambiguously be determined by value of voltage at the time of switching and by the sign of a derivative of this voltage.



**Figure 5.** Scheme of the phase voltage quantization and record block

This means that the identification problem reduces to determining the voltage value and the derivative sign of the voltage value is determined by means of level quantization. Since there are 7 values of voltage, the entire range of the input signal will be divided into sections so that all these values appeared in the middle of these sections.

As a result, we obtain 6 quantization levels: 205,263 V; 150,263 V; 55 V; -55 V; -150,263 V; -205,263 V.

The scheme including 6 voltage comparators of ( $K_1, K_2, K_3, K_4, K_5, K_6$ ) and the speed comparator consisting of the differentiator and the comparator  $K_d$ , will be taken as a device realizing this quantization. Each comparator is adjusted on a certain level of input voltage so that the output signal would change from 0 to 1 every time when input voltage exceeds the set level. As all 12 quantization levels are coded by the 4-digit code, it is necessary to connect the device with 7 inputs and 4 outputs to the output of comparators  $K_1 - K_6, K_d$ . This coding device  $CM_{ph}$  has to convert a seven-digit code of each step created by phase voltage to the four-digit. The equations of the coding device  $CM_{ph}$  can be written in PDNF form<sup>3</sup> as follows:

$$\begin{aligned}
 A_1 &= \bar{K}_1 \bar{K}_2 K_3 K_4 K_5 K_6 K_d + \bar{K}_1 K_2 K_3 K_4 K_5 K_6 \bar{K}_d + \bar{K}_1 K_2 K_3 K_4 K_5 K_6 K_d + K_1 K_2 K_3 K_4 K_5 K_6; \\
 A_2 &= \bar{K}_1 \bar{K}_2 \bar{K}_3 K_4 K_5 K_6 K_d + \bar{K}_1 \bar{K}_2 K_3 K_4 K_5 K_6 \bar{K}_d + \bar{K}_1 \bar{K}_2 \bar{K}_3 K_4 K_5 K_6 \bar{K}_d + \bar{K}_1 \bar{K}_2 \bar{K}_3 \bar{K}_4 K_5 K_6 K_d; \\
 A_3 &= \bar{K}_1 \bar{K}_2 \bar{K}_3 K_4 K_5 K_6 K_d + \bar{K}_1 \bar{K}_2 K_3 K_4 K_5 K_6 \bar{K}_d + \bar{K}_1 \bar{K}_2 \bar{K}_3 K_4 K_5 K_6 \bar{K}_d \\
 &\quad + \bar{K}_1 \bar{K}_2 \bar{K}_3 \bar{K}_4 K_5 K_6 K_d + \bar{K}_1 \bar{K}_2 \bar{K}_3 \bar{K}_4 K_5 K_6 \bar{K}_d + \bar{K}_1 \bar{K}_2 \bar{K}_3 \bar{K}_4 K_5 K_6 K_d; \\
 A_4 &= \bar{K}_1 K_2 K_3 K_4 K_5 K_6 K_d + K_1 K_2 K_3 K_4 K_5 K_6 + \bar{K}_1 \bar{K}_2 \bar{K}_3 K_4 K_5 K_6 \bar{K}_d \\
 &\quad + \bar{K}_1 \bar{K}_2 \bar{K}_3 \bar{K}_4 K_5 K_6 K_d + \bar{K}_1 \bar{K}_2 \bar{K}_3 \bar{K}_4 K_5 K_6 \bar{K}_d + \bar{K}_1 \bar{K}_2 \bar{K}_3 \bar{K}_4 K_5 K_6 K_d.
 \end{aligned}$$

These equations are realized by means of digital circuitry engineering methods<sup>3</sup>.

The four-digit codes of numbers of the steps formed by linear and phase input voltage obtained at the output of six blocks 2 and six blocks 4 need to be compared by means of the comparison block (Block 3 in Figure 1.) to the four-digit code of the step number obtained by modulating signal quantization. If the code at the output of any 12 blocks coincides with the code at the reference modulating voltage quantization scheme output, this means that the step formed by this input voltage coincides with the required step obtained as a result of the reference modulating voltage quantization. And, therefore, it is necessary to connect this input voltage to the frequency converter output.

Since the set and identified codes of steps are presented in the form of a four-digit code, digit-by-digit comparison requires 4 logical equivalence elements.

Signals  $Q_0^M, Q_1^M, Q_2^M, Q_3^M$  are those obtained at the output of reference modulating voltage quantization scheme (Figure 3). Signals  $Q_0, Q_1, Q_2, Q_3$  are those obtained at the output of one of blocks 2 or 4 (Figure 4, 5). If they coincide, a logical unit is formed at the output of comparison block 3. This means that the phase section of which forms the required step at the given moment should be connected to the frequency converter output.

**Table 1.** Values of output voltage harmonic distortion factor

Type of Modulation	Values of Output Voltage Harmonic Distortion Factor		
	From 50 Hz to 15 Hz	From 13.636 Hz to 5.357 Hz	To 5.172 Hz
PWM	Ranging within $64.9\% \geq K_g \geq 63.5\%$		
Direct frequency conversion	Not less than 53.9% at 3-phase input voltage		
	At 6-phase voltage $K_g$ changes within $31.8\% \geq K_g \geq 27.3\%$		
	At 9-phase voltage $K_g$ changes within $21.1\% \geq K_g \geq 16\%$		
	At 12-phase voltage $K_g$ changes within $15\% \geq K_g \geq 11.9\%$		
	At 18-phase voltage $K_g$ changes within $9.8\% \geq K_g \geq 7.9\%$		
Amplitude modulation	At 24-phase voltage $K_g$ changes within $7.3\% \geq K_g \geq 4.3\%$		
	ranging from 16.8% to 13.1%, which requires application of pulse-width modulation for shift of harmonics to the high frequency region	not exceeding maximum permissible value of 12% according to GOST 13109-97	not exceeding 8% according to GOST 13109-97

In total there should be 12 of such comparison blocks according to the number of input voltage phases.

Input twelve-phase voltage ( $U_{int1}(t), U_{int2}(t), \dots, U_{int12}(t)$ ) is supplied to the inputs of null detectors (comparators) C of the synchronization block. Comparators K are adjusted so that their output signals would change from 0 to 1 every time when the sign of their input signals changes from negative to positive in the vicinity of zero volts intercept point, i.e., when crossing any input voltage of zero. A unit formed at the time of the input signal crossing with zero comes from the comparator to the pulse generator, PG. The pulse generator generates a unit pulse. The unit pulses from PG outputs formed by crossing of input voltages of zero volts arrive to the OR (1) logical element which results in generation of pulse  $U_C$  fixing zero crossing of any voltage  $U_{int1}(t) - U_{int12}(t)$ . Figure 1 shows the synchronization block scheme (5)

## 4. Results

A technique is proposed to form switching functions of the sinusoidal signal providing synthesis for the electric drive on the basis of amplitude modulation. It allows receiving a signal of the following quality:

- In the frequency range below 5.2 Hz harmonic distortion factor  $K_g$  does not exceed 8%.
- In the frequency range from 13.6 Hz to 5.4 Hz  $K_g$  factor does not exceed maximum permissible value of 12% according to GOST 32144-2013.
- In the frequency range from 50 Hz to 15 Hz  $K_g$  factor varies from 16.8% to 13.1% which requires application of Pulse Width Modulation (PWM) for shift of harmonics in the high frequency region.

This technique enables to lower significantly  $K_g$  factor of the signal, and to obtain the operating signal of the demanded quality in the frequency range below 13.6 Hz.

A scheme has been developed for the switching function generator of the MFC control system with amplitude modulation-based algorithm consisting of 6 identical linear voltage quantization and record blocks and 6 identical phase voltage quantization and record blocks, and also the modulating voltage quantization block, the synchronization block and 12 comparison blocks. The structure consisting of separate identical blocks allows simplifying the production and maintenance process.

The results of comparing the output voltage quality obtained by means of amplitude modulation with the existing modulation methods<sup>6,7</sup> are given in Table 1.

## 5. Discussion

This device allows receiving at MFC output voltage of the following quality<sup>5</sup>:

- In the frequency range from 5.172 Hz and lower harmonic distortion factor  $K_g$  does not exceed 8%. According to GOST 13109-97 normally admissible value of voltage waveform distortion factor at  $U_n = 380$  V makes 8%.
- In the frequency range from 13.636 Hz to 5.357 Hz the harmonic distortion factor  $K_g$  does not exceed maximum permissible value of 12% according to GOST 13109-97. This means that no additional techniques (for example, pulse-width modulation) for output voltage improvement are required.
- In the frequency range from 50 Hz to 15 Hz the harmonic distortion factor varies from 16.8% to 13.1%,

which requires application of pulse-width modulation for shift of harmonics in the high frequency region.

The structure consisting of separate identical blocks allows simplifying the production process and also applying modular technology in production and maintenance of the device and the entire control system in general.

This technique allows reducing considerably the value of MFC voltage waveform distortion factor, and receiving the output voltage of the demanded quality in the low frequency region (to 13.6 Hz) according to the requirements of GOST 32144-2013.

## 6. Conclusion

As a result of the conducted research, the following opportunities of the control principles have been established for improvement of electric drive signal quality, which proves that achievement of the required quality of a signal according to GOST 13109-97 is possible only by means of considerable complication of power section of converters:

- The switching function generator with direct signal formation does not allow receiving a qualitative signal due to change of modulation algorithms: the smallest value of harmonic distortion factor is obtained at trapezoidal modulation for sinusoidal positive and negative synchronization. The value of harmonic distortion factor  $K_g$  thus makes not less than 53.9% (at 50 Hz  $\geq v > 1.5$  Hz).
- Values of the harmonic distortion factor at linear modulation and linear synchronization for direct transformation of frequency are as follows:

At 6-phase voltage  $K_g$  varies within  $31.8\% \geq K_g \geq 27.3\%$ .

At 9-phase voltage  $K_g$  varies within  $21.1\% \geq K_g \geq 16\%$ .

At 12-phase voltage  $K_g$  varies within  $15\% \geq K_g \geq 11.9\%$ .

At 18-phase voltage  $K_g$  varies within  $9.8\% \geq K_g \geq 7.9\%$ .

At 24-phase voltage  $K_g$  varies within  $7.3\% \geq K_g \geq 4.3\%$ .

- The In the electric drive frequency control system constructed by the PWM principle the switching function generator leads rather to the shift of harmonics in the range of frequencies multiple of the carrier frequency, than to reduction of sinusoid signal distortion. The harmonic distortion factor takes on values within  $64.9\% \geq K_g \geq 63.5\%$  for the frequency range of 50 Hz  $\geq v > 5$  Hz.
- PWM contributes to additional distortions of a signal and, as a result, increases in harmonic distortion factor. Thus, factor  $K_T$  takes on values within  $51.1\% \geq$

$K_g \geq 39.1\%$  for the frequency range of 50 Hz  $\geq v > 5$  Hz without PWM.

Therefore, significant improvement of signal quality for the electric drive on the basis of direct frequency conversion is possible only when increasing the number of input voltage phases, i.e., due to change of the converter power section. PWM does not provide the quality of a signal required according to GOST 13109-97. Application of PWM is possible only as an additional technique for shift of separate harmonics to the high-frequency region.

A technique is proposed to form switching functions of the sinusoidal signal providing synthesis for the electric drive on the basis of amplitude modulation. It allows receiving a signal of the following quality:

- In the frequency range below 5.2 Hz the harmonic distortion factor  $K_g$  does not exceed 8%.
- In the frequency range from 13.6 Hz to 5.4 Hz  $K_g$  does not exceed maximum permissible value of 12% according to GOST 32144-2013.
- In the frequency range from 50 Hz to 15 Hz  $K_g$  changes from 16.8% to 13.1%, which requires application of PWM for shift of harmonics to the high-frequency region.

This technique allows reducing considerably the value of MFC voltage waveform distortion factor, and receiving the output voltage of the demanded quality in the low frequency region (to 13,6 Hz). This way enables to lower significantly  $K_g$  of the signal, and to receive the operating signal of the required quality in the frequency range below 13.6 Hz.

The switching function generator in frequency control system of electric drives with amplitude modulation-based algorithm consisting of separate identical blocks is developed. Its structure consisting of separate identical blocks allows simplifying the production and maintenance process. As a result of research the authors succeeded to obtain qualitative output voltage of MFC without changing the power scheme, but only due to the development of switching function generator of the control system realizing amplitude modulation algorithm. Comparison of this technique with others, used in frequency converters, showed its advantage in terms of ensuring quality of output voltage.

## 7. Acknowledgment

The research was performed within R&D No. 115011460049 of 14.01.2015 "The switching function

generator of the matrix frequency converter control system” at the chair of Industrial Power Supply of Federal Public Budgetary Educational Institution of Higher Education “Orenburg State University” branch in Kumertau.

## 8. References

---

1. GOST 13109-97. Electric energy. Compatibility of technical means the electromagnetic. Standards of quality of electric energy in systems of power supply of general purpose. Moscow: Standartinform; 2006.
2. Gjugyi L, Pelly B. Static power frequency changers: Theory, characteristics, application. Translated from English. Moscow: Energoatomizdat; 1983.
3. Lanchin VI, Savyolov NS. Electronics: Textbook. Rostov-on-Don: Phoenix; 2007.
4. Piyanykh BE, Chekhet EM, Mikhalsky VM, Mordach VP, Sobolev VN, Korolkov KM. Method for output voltage formation of the three-phase and single-phase frequency converter. Patent USSR No. 1617572. 1990. Bulletin No. 48.
5. Fedorov SV, Bondarev AV. Ways of pulse-width modulation based on comparison of the synchronizing signals with signals of matrix frequency converter modulation. Bulletin of the Orenburg State University. 2014; 3(164):180–6.
6. Fedorov SV, Roginskaya LE, Bondarev AV. Influence of algorithms of control system output voltage formation on the qualitative indicators of matrix frequency converter. Practical Power Electronics. 2014; 4:27–31.