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The Road to Fully Integrated DC–DC Conversion via the Switched-Capacitor Approach

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***Abstract*—This paper provides a perspective on progress toward realization of efficient, fully integrated dc–dc conversion and regulation functionality in CMOS platforms. In providing a comparative assessment between the inductor-based and switched-capacitor approaches, the presentation reviews the salient features in effectiveness in utilization of switch technology and in use and implementation of passives. The analytical conclusions point toward the strong advantages of the switched-capacitor (SC) approach with respect to both switch utilization and much higher energy densities of capacitors versus inductors. The analysis is substantiated with a review of recently developed and published integrated dc–dc converters of both the inductor-based and SC types.**

***Index Terms*—Charge-pump, high power density, power supply on chip, switched-capacitor (SC) dc–dc converters.**

I. Introduction

THE demand for integrated power conversion, regulation, and management functions has progressed along with advances in computing, communicating, and other integrated circuit technologies. Nevertheless, efficient integrated power conversion is now at its infancy in relation to the maturing development of the system-on-chip (SOC) functions that would be best served by such converters. Since present day multicore processors dissipate power in the range of 1 W/mm^2, and would also ideally utilize many independently controlled voltage rails, a target benchmark is an integrated dc–dc conversion and regulation design that 1) handles about 10 W/mm^2 [1]; 2) steps down from a conveniently chosen voltage above typical CMOS core operating voltages; 3) provides high efficiency over a wide load and voltage range; 4) provides tight regulation; and 5) is highly scalable for granular implementation. Although there are now promising paths toward this set of goals, with both inductor-based and switched-capacitor (SC) dc–dc conversion methodologies, the path ahead remains very challenging.

This paper provides an overview of the key technological considerations needed to make a comparative analysis between the potential for full or near-full integration of SC and inductor-based dc–dc converters. As a side note, it is worth noting that linear regulation (e.g., the low-drop-out (LDO) regulator [20]) is a mature technology that mostly meets the aforementioned objectives, except for the impossibility of achieving high efficiency across a wide range of conversion ratios. By full integration, we refer to an implementation using a production CMOS process, and by "near full integration," we refer to either the use of nonstandard CMOS process steps or the use of a limited number of off-chip components. Common examples of "near-full integration" are CMOS processes augmented with backend magnetic and thick metal conductor layers, or augmented with high-density deep-trench capacitors.

The traditional inductor-based buck converter has been the default design for most switched-mode voltage regulators for decades, as it has dominated the moderate- to high-power ($>$100 mW) applications. However, the buck converter requires either a technologically intensive integrated inductor (i.e., non-production CMOS) or a bulky off-chip inductor, and transistors rated for the full input voltage and the full output current of the application. In contrast to the buck converter, an SC converter requires only capacitors as passives, which have significantly higher energy and power densities, and are also more easily integrated than inductors. Historically, SC converters have been used in integrated circuits [1] to provide programmable voltages to memories, but have mostly been limited to low-power ($<$100 mW) applications. However, SC converters theoretically have lower intrinsic conduction loss than inductor-based converters for a given total rating (e.g., V-A product) of switches for certain converters or applications [2]. This advantage of the SC converters, among others, can begin to be elucidated by the following idealized example.

Fig. 1 shows, side by side, an ideal buck converter and an ideal ladder SC converter for 10 V to 1 V conversion into a 1 A load. A simple analysis based on peak voltage and current stresses, summed over switches, yields a value of 20 V-A for the buck converter and of 7.2 V-A for the ladder SC converter. In the case of the buck converter, inductor ripple current is neglected assuming an idealized best case, and for the SC converter, ripple current is also neglected during each phase (50% duty cycle) of switch conduction. The rational for this latter assumption is that this is actually a worst case for conduction losses, corresponding to the "fast switching limit" (FSL) where switch conduction

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Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

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[1] 10 W/mm^2 is a good target for utilization of additional *active* silicon area since passives like magnetics and/or MIM capacitors can possibly be implemented above existing active circuitry.

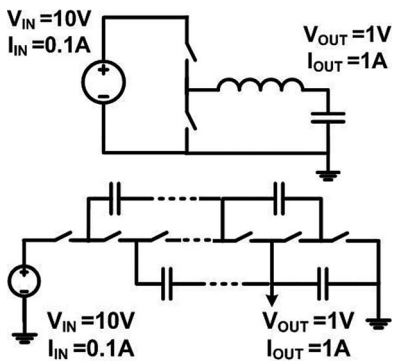

Fig. 1. 10:1 step-down buck and ladder-type SC converters.

losses are dominant [2]. More details appear in the following sections. This substantially reduced switch V-A stress total is a first apparent advantage for the SC converters. A second advantage of the SC converter, also evident in the diagram, is the fact that each switch in the ladder SC circuit need be rated only for the 1 V output voltage, and hence can be implemented with a high-performance NMOS transistor if triple-well isolation or some other voltage stacking capability [e.g., silicon on insulator (SOI)] is available. In contrast, the switches in the buck converter need to be implemented with devices that are safely rated to handle the 10 V input voltage.

A third point, also in favor of the SC ladder circuit, is that the circuit incurs no inductive switching losses, and thus the related design problems including overshoots, body diode conduction, and timing issues associated with deadtimes are either entirely avoided or substantially mitigated. A fourth point is that inductor ac and dc conduction losses are inherently not present in the SC ladder circuit. A fifth point, crucial for SOC applications, is that each load circuit requires bypass capacitance. Generalizing, many SC circuits, especially the series–parallel types, place half of their working (or flying) capacitors across the output terminal at each instant, thus mitigating the need for substantial additional bypass capacitance. Finally, the SC circuit readily admits low-power operation without need for any control complexity, simply by reducing clock rate to arbitrarily low frequencies. In contrast, the buck converter needs to be operated in some pulsed discontinuous conduction mode (DCM) or use complicated loss reduction techniques [3] to effect high efficiency at light load. As will be elaborated in Section IV, the practical energy density of small capacitors, both surface mount and IC based, is many orders of magnitude greater than that of their inductive counterparts. Consequently, it will be argued that the SC converters enjoy an even greater advantage when considering a comparison of utilization of passive components.

These advantages of the SC conversion approach are now being exploited by many practitioners, including [4], [5], [6], [7], [8], and [32]. These works further demonstrate that SC converters can achieve high power density and high efficiency in moderate power applications (e.g., >1 W).

Common complaints about SC dc–dc converters concern ripple and regulation, i.e., the challenge of maintaining reasonable efficiency over a range of conversion ratios. Examples in the literature [4], [5], [8], [17], and [21] show that these concerns are not blocking issues, but do require attention, and will be discussed. The analysis and examples point to the conclusion that SC converters can and will surpass their magnetic counterparts in overall performance.

Seeman and Sanders [2] discuss a methodology to analyze and optimize SC converters, and compare the SC converter with the buck converter in terms of switch utilization. This paper expands on the discussion in [2], but especially focuses on utilization of reactive elements. Section II first gives a brief review of the results in [2], and introduces common metrics to compare switch utilization in both SC and inductor-based converters. Section III expands on this discussion, providing a framework for comparison of utilization of passives among both SC and inductor-based converters. Section IV details the comparative merits of numerous SC and inductor-based converters, but still at a general level. Section V then reports on specific published works that substantiate the comparisons developed in the prior sections. Some details on progress on control and regulation of SC converters are given in Section VI. Concluding remarks and speculation on future directions are given in Section VII.

II. SC Converter Modeling

Neglecting frequency-dependent parasitic losses, the steady-state behavior of a SC converter can be modeled as an ideal transformer with a series output impedance [2], [24], [25]. In this model, the turns ratio, n, represents the conversion ratio, determined by the converter topology and switching pattern. The output impedance represents the requisite output voltage drop used to move charge in the circuit. The output impedance is a function of converter topology, switching frequency, and component sizes.

SC converters can operate in one of two asymptotic operating conditions, or in the region between them. At low switching frequencies, the converter losses and output impedance are dominated by the amount of charge that can be transferred by capacitors. This asymptotic regime is denoted by the slow switching limit (SSL). At high frequencies, the switch on-state resistance prevents the capacitors from completely transferring their charge each period, and thus, the switch resistance dominates the converter's loss. This asymptotic operating regime is denoted by the FSL.

This discussion assumes two-phase converters operating at 50% duty cycle and insignificant parasitic equivalent series resistance (ESR) of the capacitors. The asymptotic SSL (capacitor-dominated) and FSL (switch-dominated) output impedances are given by the following equations [2]:

$$R_{\mathrm{SSL}} = \frac{1}{f_{\mathrm{sw}}} \sum_{i \in \mathrm{caps}} \frac{\left(a_{c,i}\right)^2}{2C_i} \tag{1}$$

$$R_{\mathrm{FSL}} = 2 \sum_{i \in \mathrm{switches}} R_i \left(a_{r,i}\right)^2. \tag{2}$$

In (1), f_{sw} represents the switching frequency, C_i is the value of capacitor i, and $a_{c,i}$ is the charge multiplier of capacitor i. The charge multiplier is defined as the ratio between the charge

flowing in capacitor i during a single period and the average output charge during that period. Similarly, in (2), R_i and $a_{r,i}$ are the on-state resistance and charge multiplier for switch i, respectively. It is straightforward to fold in the contribution to loss and output resistance from capacitor ESR, as done for switch resistances in (2). This is not done here in order to keep the presentation simple, and because many integrated circuit capacitors have ESR corner frequencies well above the practical converter operating frequencies, keeping capacitor ESR loss as only a very small fractional loss component.

These expressions for an SC converter's output impedance explicitly allow for its optimization. By constraining total switch V-A product (related to area for integrated implementations) or capacitor energy storage, each circuit element can be sized proportionally to its charge multiplier and inversely to its blocking voltage. This optimization yields the smallest output impedance for a given allotment of switch V-A product or capacitor energy storage.

After carrying out the aforementioned optimization steps, a pair of performance metrics can be developed from the output impedance expressions in (1) and (2) to express the ratio of the optimized performance of an SC converter to the cost of the components used. In the case of the SSL, the dimensionless metric in (3) is the ratio of the converter output capability per unit clock frequency $GV^2/f_{\rm sw}$ (where G is the output-referred converter conductance) to the total energy storage. In the case of the FSL, the metric in (4) is the ratio of the converter output capability GV^2 to the value of the GV^2 ratings of the switches, totaled over the switches. Converter output capability GV^2 is a precise metric, the product of the squared open-circuit output voltage and the output conductance, that allows an exact computation of a power delivered versus loss relationship [2]. The metrics (3) and (4) assume that the switches and capacitors are sized optimally as described previously and in [2]. The SSL and FSL metrics are given as follows:

$$M_{\rm SSL} = \frac{2V_{\rm OUT}^2}{\left(\sum_{k\in{\rm caps}} \left|a_{c,k} v_{c,k({\rm rated})}\right|\right)^2} \tag{3}$$

$$M_{\rm FSL} = \frac{V_{\rm OUT}^2}{2\left(\sum_{k\in sw} \left|a_{r,k} v_{r,k({\rm rated})}\right|\right)^2}. \tag{4}$$

Notice that each of these dimensionless metrics depends only on the squared absolute sum of the V-A products for the relevant circuit elements—capacitors or switches—normalized by squared output power. Thus, the performance metrics relate directly to the fundamental operation of the underlying circuit. In these metrics, the voltage used for characterization is the component voltage rating, since this sets the cost of the device. [2] In all cases, the maximum expected working voltage must be less than this rated voltage.

In the previous discussion, it was implied that the switch V-A product, equivalently switch GV^2 rating, scales linearly with integrated circuit die area. There is undoubtedly a monotonic dependence between the die area and the V-A product. The simplifying assumption of a linear relationship is made to allow a fairly general discussion and presentation. Caveats occur first due to the discretization of available device voltage ratings in any given integrated circuit process. Thus, when evaluating the quantity in (4), one needs to carefully select the process and device type to sustain the maximum working voltage.

A more detailed scaling study of V-A rating with respect to voltage rating would need to take into account device family type and technology details. Such a study is beyond the practical scope of this paper. Nevertheless, we note that the metric in classical references [26], [27], for assessing asymptotic performance of power semiconductor device platforms in terms of $R_{\rm ds-on}$–Area product, do call out exactly the GV^2 rating as the fundamental quantity relevant for this evaluation.

III. Fundamental Limits

The metric $M_{\rm FSL}$ introduced in (4) provides an effective metric for comparison among SC converters. It turns out that the same metric can be computed for any standard inductor-based converter, as has been done in [2]. An analysis using the results reported in [2] (and alluded to in Section I) that compares relative switch utilization effectiveness in SC and inductor-based converters appears in Section IV.

Of greater interest in this paper is an analysis of relative utilization and requirements for passive components. For this analysis, we refer to the seminal work of Wolaver [9]. Wolaver [9] developed fundamental limits on the component stresses in any dc–dc converter. For the reactive elements in any dc–dc converter, Wolaver [9] states and proves the following relation:

$$\frac{1}{2}\sum_{k\in{\rm reactances}} \overline{|v_k i_k|} \geq \frac{n-1}{n}\overline{P_{\rm OUT}} \tag{5}$$

where n is the current or voltage step-up ratio (whichever is greater than one) and v_k and i_k are, respectively, the instantaneous voltage across and current through reactive element k, with the overbar indicating a time-averaged quantity for periodic steady-state operation. This is a compact constraint on total reactive element V-A stress. Specializing to steady-state operation of conventional two-phase SC or inductor-based dc–dc converters, the quantity on the left-hand side of (5) is the total time-averaged absolute energy absorbed by the reactive elements.

For a conventional two-phase SC circuit, the one-period time-averaged absolute current through a capacitor can be represented in terms of its charge multiplier

$$\overline{|i_k|} = 2\left|a_{c,k}\right| I_{\rm OUT}. \tag{6}$$

Substituting (6) into (5), and assuming linear capacitors, yields

$$I_{\rm OUT}\sum_{k\in{\rm caps}} \overline{v_k}\left|a_{c,k}\right| \geq \frac{n-1}{n} V_{\rm OUT} I_{\rm OUT} \tag{7}$$

[2] A similar analysis has been used to co-optimize for efficiency and power density, while considering dynamic losses associated with capacitor bottom plate and device gate capacitances [5].

or equivalently

$$\sum_{k\in\text{caps}} \frac{\overline{v_k}}{V_{\text{OUT}}} |a_{c,k}| \geq \frac{n-1}{n}. \tag{8}$$

This fundamental limit effectively restates the Wolaver inequality limit (5) in terms of the capacitor charge multipliers and average capacitor working voltages, expressed as a ratio with the output voltage. The dimensionless quantity appearing on the left-hand side of inequality (8) is computed for the most frequently used SC converters in the dissertation [12]. As will be discussed in the next section, the series–parallel converter meets the limit (8) with equality. Since the series–parallel converter achieves the fundamental limit, it is capable of the highest ideal performance of any capacitor-limited SC converter.

Analogously, when the reactance-based performance limit, considering only the power inductor, is found for the buck converter, it meets the Wolaver limit in (5) with equality. It is reasonable to focus only on the inductor for this high-level analysis, since for steady-state operation, the input and output capacitance can be made arbitrarily small, in principle, by using a sufficiently large number of interleaved converter phases. Of course, even without considering input or output voltage ripple, some bypass capacitance will still be required. We note that inductor peak energy storage is minimized with a design choice that corresponds to operation at the edge of DCM, also known as critical conduction, though this choice does not typically correspond to minimal inductor size given a loss constraint. Thus, in the sense of the fundamental Wolaver inequality (5), the buck (and boost) converter is also optimally effective in its use of its key reactive element.

We note for completeness here that Wolaver's results also include inequality bounds analogous to (5), but applicable to the switches. We omit discussion of these since we have already introduced an effective metric in (4) for comparison among all circuits, and because Wolaver's results provide bounds on the product of averaged absolute voltage and averaged absolute current. We do not believe, in general, that averaged absolute voltage is a useful metric for a switch in a dc–dc converter, since in some instances a switch may block a large voltage, but for only a small fraction of a period.

IV. Comparison of Topologies

This section provides a comparative analysis of the SC and inductor-based converters in terms of the metrics and fundamental limits introduced in the prior two sections.

A. Switch Utilization

The limits on converter performance developed in Sections II and III utilize properties that apply to all dc–dc converters. Thus, it is highly informative to use these metrics to compare SC and traditional buck converters. The FSL metric for a buck converter (and equivalently the boost converter) can be derived [2], and is given by

$$M_{\text{FSL,buck}} = \frac{1}{n\left(\sqrt{n-1}+1\right)^2}. \tag{9}$$

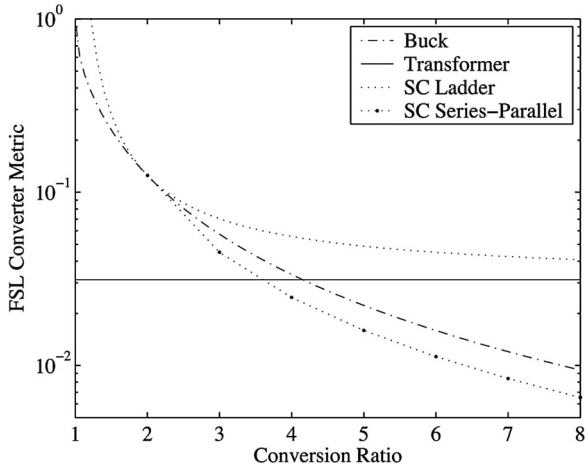

Fig. 2. FSL switch metric versus conversion ratio. Data plotted for buck (equivalent to boost), ideal transformer bridge converter, SC ladder (equivalent to Dickson), and SC series–parallel converter.

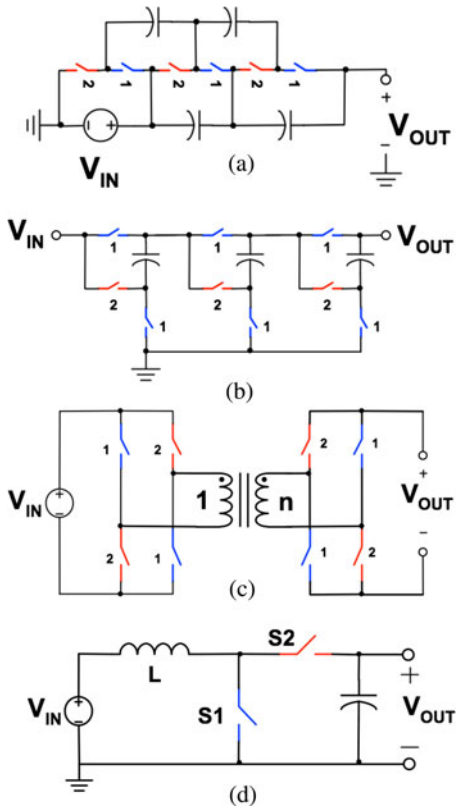

Fig. 3. Four basic converters: (a) ladder, (b) series–parallel, (c) ideal transformer, and (d) boost (buck).

When finding this metric, the converter's total switch GV^2 rating is constrained, and the two switches' relative sizes are jointly optimized to minimize conduction loss for each specific conversion ratio to develop this expression. Fig. 2 provides a graphical comparison of the resulting optimized switch conduction metrics for four representative converters: the SC ladder (equivalently Dickson), the SC series–parallel, the buck (equivalently boost), and a basic ideal-transformer bridge converter. Fig. 3 illustrates these four representative converter circuits.

As is evident from Fig. 2, the ladder (and also equivalently the Dickson) converter is best at all conversion ratios. This result was foreshadowed in Section I. Also of interest, the three nontransformer-isolated circuits perform equivalently at a conversion ratio of 2 ($n = 2$). The transformer-isolated circuit has an equal metric at all conversion ratios since the conversion ratio is readily achieved by simply adjusting the ideal transformer turns ratio, keeping switch stresses invariant. Although further discussion might be of interest, we note that [2] includes some of this discussion. With present day technological concerns, we believe that the differentiation in utilization of passive elements is now of greatest interest, and so turn to this topic.

B. Passive Element Utilization

As discussed in Section III, the Wolaver bound in (5) provides an effective metric to begin comparisons of passive element utilization across topologies and technologies. First, as introduced in Section III, the time-averaged absolute V-A stress product on the capacitors in the series–parallel SC converter meets the Wolaver bound with equality. And, this is also the case for the buck converter when considering its key component, the inductor. In the case of the ladder SC converter, the quantity on the left-hand side of (5) takes the value $((n–1)^2/n)P_{\rm OUT}$ [12], and thus, the working capacitors in the ladder circuit need to handle more reactive power in an overall assessment for conversion ratios greater than 2. (For conversion ratio 2, the series–parallel and ladder circuits are actually identical circuits.) Thus, for a relatively high conversion ratio example with $n = 10$, as introduced in Section I, the net average absolute V-A stress on the capacitors is nine times larger than would be the case in an optimally effective circuit. The discussion will be completed here by: 1) assessing the practical relationship between the time-averaged absolute V-A stress product and the required energy storage in each type of circuit; and 2) by giving a comparative assessment of reactive component energy density.

When comparing reactive element usage, we see that SC converters are similar to inductor-based converters in terms of required V-A product for the best topologies in each class. However, the electrical utilization of the energy of the reactive elements differs significantly. Inductor-based converters, such as the buck and boost topologies, can, in principle, fully magnetize and demagnetize a lossless inductor each period in the case of discontinuous or critical conduction without incurring loss. This is not usually the case in practice, since there are significant losses associated with ripple current and ripple flux. Typical flux swings are in the range of 20%–40% peak to peak for representative buck converter designs. SC converters, on the other hand, ideally only utilize a small fractional ripple voltage on their capacitors, since this ripple corresponds to loss, also known as charge-sharing (or SSL) loss. A representative high-efficiency design allotting 5% loss to charge-sharing (or SSL) loss might call for about 10% peak-to-peak voltage ripple. It is the fractional ripple that defines the ratio between the time-averaged absolute V-A stress and the required energy storage. Thus, in order to meet representative efficiency objectives, the SC converters generally require an additional multiplicative factor in the range of about four times more energy storage than that required in an inductor-based converter. This ratio may be as high as 20 in the case of a comparison between a very high efficiency SC converter, and a buck converter designed to operate at the critical conduction limit.

Despite the potential need to store some additional energy in SC converters, the dominantly superior energy density of capacitors with respect to inductors for practical frequencies and implementations allow SC circuits to provide substantially higher power density at equal efficiency, or substantially higher efficiency at equal power density. The energy density advantage for a representative sampling of surface mount capacitors is captured in Table I. As can be seen in the table, the energy density of these small discrete capacitors is generally in the range of more than three orders of magnitude greater than that of similarly scaled inductors. For the inductors, energy is limited by the manufacturers' specified current limits, whether these arise from a thermal limit or magnetic saturation.

A fair comparison between integrated inductors and integrated capacitors requires a consideration of the technology used in the two relative converter types. With an initial implementation goal to ensure no additional cost for special process steps, we consider the use of gate dielectric to implement capacitors. Given an area of 1 mm^2 in today's CMOS technology, a capacitance of about 10 nF can be obtained to achieve an energy density of 5 nJ/mm^2 at 1 V of operation. Analogously, for an inductor, we restrict an example implementation to use a 3-μm-thick[3] top metal layer. For a planar spiral inductor implementation with 1 mm diameter, two turns, 100-μm line width[4] and 50-μm line spacing, approximately 4 nH can be achieved, but with a dc resistance of 400 mΩ. Allowing for 5% power loss due to dc conduction (while still neglecting all other loss mechanisms) into a representative 1 V load restricts maximum dc current to 125 mA. As such, this inductor realizes an areal energy density of 31 pJ/mm^2, based on dc conduction. Note that the value of 4 nH would result in operation at critical conduction at 500 MHz, a rather high frequency for state-of-the-art CMOS-based converters, in a 2 V to 1 V buck application. Thus, for this representative comparison of readily available CMOS capacitors and inductors, the pattern of orders of magnitude greater energy density in the favor of capacitors prevails.

In summary, the prevailing superior available energy (and power) density of integrated and small surface mount capacitors, in comparison to inductors, drives an expectation that SC converters should outperform inductor-based converters when making comparisons on charts of efficiency and power density. This is the subject of Section V.

C. Switching Loss Discussion

Although the comparative analysis in this section does not comprehensively address switching losses, it is appropriate to provide some commentary. In the discussion of switch

[3]The top metal in most of the standard processes today is usually thinner than this example (e.g., 1 μm thick).

[4]In practice, certain process rules usually limit a single line width to a smaller number, leading to a higher dc resistance.

TABLE I
DIMENSIONS (mm) AND VOLUMETRIC ENERGY DENSITIES (μJ/mm^3) OF SOME REPRESENTATIVE SURFACE MOUNT CAPACITORS AND INDUCTORS

Type	Manufacturer	Value	Dimension (mm)	Energy Density (μ J/mm^3)
Ceramic Cap	Taiyo-Yuden	22μF@4V	1.6 x 0.8 x 0.8	172
Ceramic Cap	Taiyo-Yuden	1μF@35V	1.6 x 0.8 x 0.8	598
Tantalum Cap	Vishay	10μF@4V	1.0 x 0.5 x 0.6	266
Tantalum Cap	Vishay	100μF@6.3V	2.4 x 1.45 x 1.1	518
Electrolytic Cap	Kemet	22μF@16V	7.3 x 4.3 x 1.9	47.2
Electrolytic Cap	C.D.E	210mF@50V	76Φ x 219	87.8
Shielded SMT Inductor	Coilcraft	10μH@0.21A	2.6 x 2.1 x 1.8	0.02
Shielded SMT Inductor	Coilcraft	100μH@0.1A	3.4 x 3.0 x 2.0	0.02
Shielded Inductor	Coilcraft	170μH@1.0A	11 x 11 x 9.5	0.07
Shielded Inductor	Murata	1mH@2.4A	29.8Φ x 21.8	0.19

Note that energy densities of capacitors are more than three ordersof magnitude greater than those of inductors.

utilization and inductor utilization in the inductor-based circuits (i.e., buck converter), conventional switching losses associated with gate drive, hard switching, and potential body diode conduction were not explicitly considered. Two reasons for this neglect are that best-in-class control strategies minimize conventional switching losses (e.g., adaptive deadtime schemes), and gate drive losses are directly related to the switch V-A intensity. Larger switch V-A stress requires greater die area, and in turn greater gate drive power per unit frequency. In the case of the SC converters, again, the gate drive power scales directly with the required switch V-A, and so, this requirement has been factored in indirectly.

Although charge-sharing or SSL losses can be thought of as switching losses, these losses are really fundamental to the operation (and an inefficiency) of the SC converters, and have already been considered in the discussion of the passive utilization. Specifically, in the previous discussion where the capacitor ripple ratio was constrained to the range of 5%–10%, this was done to keep the SSL loss component to a very small fraction of the output power.

An important additional switching loss in the SC converters is that associated with dynamic power loss in charging and discharging parasitic (e.g., bottom plate) capacitances of the on-die integrated capacitors. Since this loss term is highly process dependent, it is not directly addressed here. Rather, the authors of [5] provide a design optimization process that fully comprises these parasitic capacitances. After optimization, the bottom plate loss term only comprises a few percentage points of the output power.

V. COMPARATIVE STUDY OF FULLY INTEGRATED IMPLEMENTATIONS

With increasing levels of integration of digital processing cores and functional blocks in SOC implementations, multiple independent power rails need to be implemented on-die to actively optimize the whole system's power and circuit performance. Simply adding off-chip supplies will not only incur serious degradations of supply impedance due to split package power planes, but also additional cost due to increased motherboard size and package complexity. Therefore, there is a strong motivation to fully integrate voltage conversion on the CMOS chip using a point-of-load strategy, as shown in Fig. 4. Toward this end goal, we study existing fully integrated CMOS converters in this section.

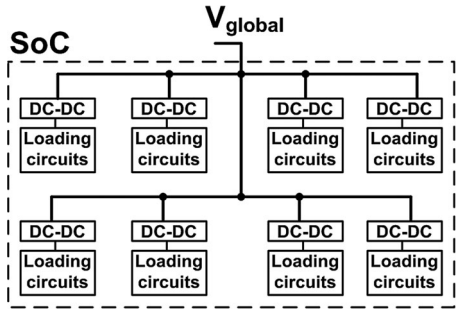

Fig. 4. On-die point-of-load power distribution.

Fig. 5 provides a two-axis chart for comparison of performance metrics for a series of experimentally tested and published fully integrated dc–dc converters, of both the SC and inductor-based types. For each circuit, a single operating point characterizing a representative best case is selected. The chart plots, for each circuit at its selected operating point, efficiency on the vertical axis versus power density on the horizontal axis on log scale. Inductor-based converters are represented with diamonds in this chart. Data points labeled [11], [22], and [23] in Fig. 5 correspond to buck converters (three-level buck for [23]) fabricated with standard CMOS processes, with no special technologies included to help with inductor implementation. For these examples, efficiencies are bounded below 80% while power densities come in at below 0.3 W/mm^2. The

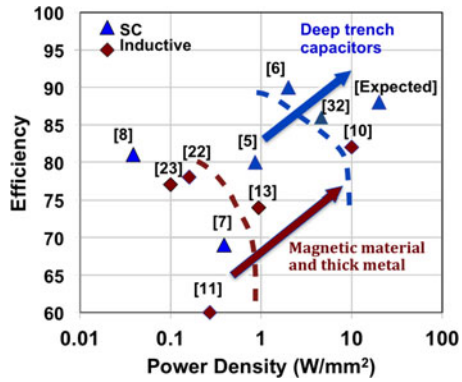

Fig. 5. Performance of fully integrated converters in production CMOS and in processes where extra steps allowed.

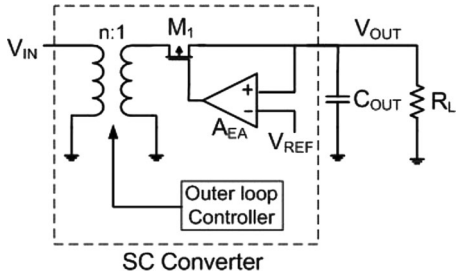

Fig. 6. Model of a regulated SC converter. Outer loop adjusts the conversion ratio, while minor loop provides fine-scale regulation.

chart illustrates a conceptual performance "front" for these data points that is then exceeded with two example circuits that do include advanced magnetics processes. The point labeled [13] corresponds to a recent effort that utilizes a plated Cu and NiFe coupled-inductor structure, implemented in an interposer layer, resulting in an areal density of about 1 W/mm^2 at 75% efficiency when considering the interposer area required for the inductor structure. The authors of [13] indicate that if only active silicon area was considered, the power density would be 10 W/mm^2. So, this point could equally well have been placed at a position corresponding to 10 W/mm^2. Finally, the data point [10] represents a complete very high power integrated buck converter that also uses a thick plated Cu (10 μm) and NiFe (4 μm) backend process to realize a 32-phase coupled-inductor structure. This backend process is applied to a standard production 90-nm CMOS process, and results in the leading buck converter data point on the chart, corresponding to 10 W/mm^2 and 82% efficiency.

On the SC side, data points [8], [7], and [5], represented with triangles in Fig. 5, correspond to SC dc–dc converters built in standard CMOS processes. The highest performance of these three examples [5] achieves efficiency of 80% at 0.86 W/mm^2 of output power density with no additional fabrication steps in a commercial 32-nm CMOS process. The work also illustrates methodologies to address several well-known issues associated with SC converters, including limited output voltage range and voltage ripple. The chart in Fig. 5 has a second performance "front" sketched in corresponding to a boundary between SC converters built in standard CMOS and those that incorporate special capacitor processes, e.g., deep trench capacitors. The data point labeled [6] corresponds to a fully integrated 2-to-1 SC converter implemented with $\sim$200 fF/μm^2 deep trench capacitors, and achieving efficiency of 90% at a power density of 2 W/mm^2. Data point [32], indicative of better than 85% efficiency at 5 Wmm^2, also corresponds to a similar fully integrated 2-to-1 SC converter, also implemented with $\sim$200 fF/ μm^2 deep trench capacitor technology. An analysis based on the experimentally verified design process described in [5] predicts that with 200 fF/μm^2 deep trench capacitors and modern CMOS switches, an optimized SC design can achieve above 88% efficiency for power densities up to 10 W/mm^2—i.e., notably higher efficiency than that of the highest performing buck converter [10] while utilizing only relatively standard processing techniques. Data points [5], [6], [32], and their extrapolation shown in Fig. 5 largely confirm the assertions made in the prior sections.

VI. Ripple and Regulation of SC Converters

Two of the typically noted challenges of SC converters are that they supposedly suffer from voltage ripple at input and output rails, and that they do not nominally provide an efficient means for regulation over a wide range of input and/or output voltages. Much progress has been made to mitigate these concerns, as outlined in this section.

With respect to voltage ripple, there are a few very successful approaches that have been applied to mitigate this concern. First, we note that the potential origin of large voltage ripple is from the approximately impulsive charge transfers that occur at low clock rates, i.e., in the asymptotic SSL. By simply operating at higher clock rates, or by designing so that resistive impedances are significant, these impulsive charge transfers can be substantially mitigated. Variations of this approach, that combine with a voltage regulation strategy, have been applied in [17], [21], and [19]. In these works, fine-scale voltage regulation is achieved by actively modulating some of the switch impedances, and as such, these modulated switch impedances dominate and control the overall output referred resistance. This operation corresponds to behavior best described by the asymptotic FSL, with current flow nearly constant during each clock phase of the circuit operation.

The utilization of multiphase circuit architectures is a most effective methodology for essentially obviating voltage ripple. A striking example of this is the 32-phase test circuit developed in [5], where voltage ripple in the single millivolt range is attained at input and output terminals, *without use of any dedicated input or output bypass capacitance*. Rather, the working (or flying) capacitors function as effective input and output capacitances. Many other practitioners (e.g., [8] and [7]) who have developed fully integrated SC converters have recognized the strong advantages of the multiphase strategy.

Regulation of an SC converter can be achieved through modulating the output referred resistance $R_{\rm OUT}$ of the converter, dynamically adjusting the unloaded conversion ratio n [14] and ideally by combination of these two mechanisms. Since the maximum achievable efficiency of an SC converter is

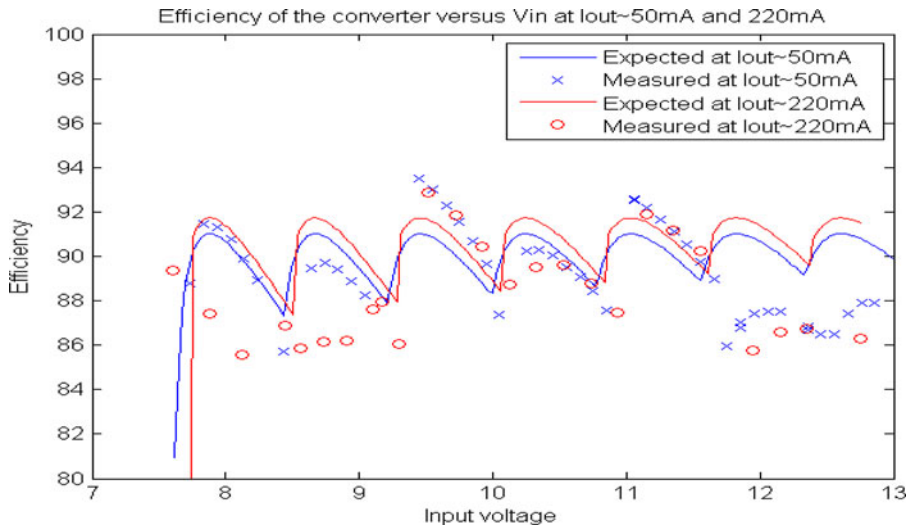

Fig. 7. Efficiency plots of regulated step-down Dickson converter of [19]. Output tightly regulated to 1.5 V.

limited by the voltage drop across the output referred resistance $R_{\rm OUT}$, changing n is desired when the ratio $V_{\rm IN}/V_{\rm OUT}$ varies substantially.

There are numerous ways to modulate $R_{\rm OUT}$ [15]–[18]. All of these methods can be categorized as either modulating the SSL impedance $R_{\rm SSL}$ or the FSL impedance $R_{\rm FSL}$. Bayer [15] implements clock pulse skipping, and Seeman [16] proposes controlling the clock hysteretically, with both of these approaches effectively adjusting switching frequency to modulate $R_{\rm OUT}$ via $R_{\rm SSL}$. Gregoire [17] varies switch conductance and Zhu [18] varies switch duty ratios, with both schemes effectively controlling switch resistances to modulate $R_{\rm OUT}$ via $R_{\rm FSL}$.

One successful implementation strategy for achieving regulation over a wide input voltage range is illustrated in the example circuit in [19] and [33]. This example circuit realizes a variable ratio step-down Dickson converter. This circuit is organized for seven step-down ratios in half-integer steps from 5:1 to 8:1, corresponding to a practical input range of 7.5–13 V, while providing a precisely regulated 1.5 V output. The overall regulation strategy combines an outer loop for conversion ratio selection and a minor loop for precise regulation of output voltage via switch conduction modulation. This strategy is illustrated in Fig. 6. Fig. 7 compares computed efficiency plots with measured data points for loads of 50 and 220 mA. Efficiencies in the range of 90% are maintained over the entire range of input voltages.

We conclude this section by noting that although ripple and regulation have been noted as challenges for the SC converters, there are actually very effective solutions addressing each of these potential concerns.

VII. Conclusion and Future Considerations

This paper provides a perspective on progress toward realization of efficient, fully integrated dc–dc conversion and regulation functionality in CMOS platforms. In providing a comparative assessment between the inductor-based and SC approaches, the presentation reviews the salient features in effectiveness in utilization of switch technology and in use and implementation of passives. The analytical conclusions point toward the strong advantages of the SC approach with respect to both switch utilization and much higher energy densities of capacitors versus inductors. The analysis is substantiated with a review of recently developed and published integrated dc–dc converters of both the inductor-based and SC types.

Undoubtedly, we shall continue to see progress on both fully integrated inductor-based and SC dc–dc converters. Fundamental to this progress is the continued development of suitable inductor and capacitor technologies.

In the case of SC converters, there is certainly more room for work on circuit strategies that enable very high efficiency over strategic ranges of input and output voltages, and over a wide load range. Associated with these circuit strategies, wideband control strategies that effect load and line transient performances equal to those achieved with loadline strategies applied in the buck converter domain are emerging. Moving away from pure SC and pure inductor-based circuits are families of hybrid circuits, which may enjoy advantages from both domains. Multilevel inductor-based circuits, e.g., the three-level buck [23], [28], are examples of these. Generalizing, cascades of SC and inductor-based converters have shown promise in mitigating charge sharing losses, since charges may be moved with a compliant inductive element, rather than through direct (resistive) transfer to another capacitor or voltage source [29]. Still, another promising hybrid is the family of resonant SC converters [30], [31], where capacitors are effectively replaced by resonant $L-C$ elements to effect nominally lossless charge transfers.

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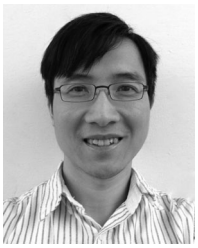

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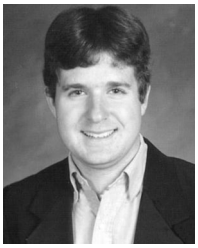

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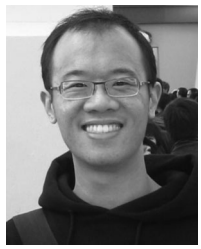

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