The Threshold–Voltage Model of MOSFET Devices with Localized Interface Charge

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***Abstract*—A new analytic threshold–voltage model for a MOSFET device with localized interface charges is presented. Dividing the damaged MOSFET device into three zones, the surface potential is obtained by solving the two-dimensional (2-D) Poisson's equation. Calculating the minimum surface potential, the analytic threshold–voltage model is derived. It is verified that the model accurately predicts the threshold voltage for not only the fresh devices but also the damaged devices. Moreover, the Drain-Induced Barrier Lowering (DIBL) and substrate bias effects are also included in this model. It is shown that the screening effects due to built-in potential and drain bias dominate the impact of the localized interface charge on the threshold voltage. Calculation results show that the extension, position and density of localized interface charge are the main issues to influence the threshold voltage of a damaged MOSFET device. Simulation results using a 2-D device simulator are used to verify the validity of this model, and quite good agreements are obtained for various cases.**

I. Introduction

IT IS WELL KNOWN that the hot-carrier effect becomes a great obstacle as the dimensions of the MOSFET devices are scaled down to submicrometer or deep submicrometer level. The hot-carrier effect is mainly caused by the high electric field in the channel near the drain junction for a short channel device. This high field provides enough energy to the channel electrons which may generate electron-hole pairs through impact ionization. The generated holes are attracted to the substrate to form the substrate current and the electrons are swept toward to the drain. If the electrons get enough energy to reach the S_i–S_iO_2 interface and surmount the barrier, the gate current is resulted. This gate current more or less creates damage in the oxide or on the interface near the drain junction and device performance is degraded. Characteristics degradation of short-channel MOSFET devices due to hot-carrier injection has attracted many comprehensive studies in recent years [1]–[12]. It is known that the degradation is attributed to the interface-trap generation and electron/hole trapping in the gate oxide [1]–[4]. Due to its strong impacts on device and circuit reliability, the hot-carrier effect becomes an important research topic for submicrometer and deep submicrometer MOSFET devices.

The hot-carrier-induced degradations include transconductance (g_m) degradation, drain conductance (g_d) degradation and threshold–voltage shift. Many models have been proposed to describe device performance degradations [5]–[9]. Moreover, different charge pumping methods have been proposed to measure the interface trap and oxide-trapped charge [10]–[12]. Unfortunately, all of the previous analytic models [5]–[8] didn't consider the two-dimensional (2-D) effects. Furthermore, the degradations of I–V characteristic in damaged MOSFET's were comprehensively studied [6], [9] only by using the 2-D device simulator.

In this paper, we devote our efforts on the threshold–voltage shift due to the hot-carrier-induced localized interface charges. The surface potential distribution along the channel of a MOSFET with localized interface fixed charge has been analytically derived by using proper assumptions and boundary conditions, based on solving the simplified 2-D Poisson's equation. The minimum surface potential along the channel is then used to calculate the threshold voltage. Depletion depth under the channel is also properly modified by the geometric factor using the charge sharing scheme. Consequently, the effects of drain bias and source/drain junction depth have been elegantly included. If the interface trap or oxide-trapped charge exists, it can be transformed into equivalent interface fixed charge. In addition, the effects of the extension, position and density of localized interface charges, drain bias, substrate bias on the threshold voltage are also investigated. Comparisons between the developed threshold–voltage model and the results of the 2-D numerical analysis have been made and quite good agreements have been obtained. Although our discussions are focused on n-channel MOSFET devices, similar results can be extended to p-channel MOSFET devices straightforwardly after polarity change.

II. Model Descriptions

The 2-D Poisson's equation can be written as

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2} = \frac{q}{\epsilon_s}[N_A(y)+N_D(y)+n(x,y)+p(x,y)] \qquad (1)$$

where $N_A(y)$ and $N_D(y)$ are the acceptor and donor concentrations in the substrate, respectively; $n(x,y)$ and $p(x,y)$ are the electron and hole concentrations, respectively; ϵ_s is the dielectric permittivity of the substrate; $\phi(x,y)$ is the electrostatic potential in the substrate; and the coordinate system is shown in Fig. 1. To a first-order approximation, the potential distribution is assumed to have the following form

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[13]:

$$\phi(x,y) = a_0 + a_1 y + a_2 y^2 + a_3 y^3 \tag{2}$$

where the $a's$ may be a function of x and can be determined by the boundary conditions. Substituting (2) into (1) and integrating y from 0 to y_d, we have

$$\frac{\partial^2 a_0}{\partial x^2} + \frac{\partial^2 a_1}{\partial x^2}\frac{y_d}{2} + \frac{\partial^2 a_2}{\partial x^2}\frac{y_d^2}{3} + \frac{\partial^2 a_3}{\partial x^2}\frac{y_d^3}{4} + 2a_2 + 3a_3 y_d = \frac{q}{\epsilon_s y_d}\left[\int_0^{y_d} N_A(y)dy + n_s(x)\right] \tag{3}$$

where y_d is the depletion depth; $N_D(y)$ is neglected in a n-channel MOSFET device; $p(x,y)$ is also ignored in the depletion and/or inversion region; $n_s(x)$ is the electron concentration per unit area. The boundary conditions on the interface and depletion edges are given as

$$\begin{cases} \phi(x,0) &= \phi_s(x) \\ \phi(x,y_d) &= V_{BS} \\ \frac{d\phi(x,y)}{dy}|_{y=0} &= \frac{C_{\rm ox}}{\epsilon_s}[\phi_s(x) - V_{GS} + V_{FB}] \\ \frac{d\phi(x,y)}{dy}|_{y=y_d} &= 0 \end{cases} \tag{4}$$

where V_{GS} and V_{BS} are the gate and substrate biases, respectively; $\phi_s(x)$ is the surface potential; $C_{\rm ox}$ is the gate oxide capacitance per unit area; V_{FB} is the flat-band voltage. Note that if the interface fixed charge density N_f appears uniformly in this device, V_{FB} should be replaced by $V_{FB} + \frac{qN_f}{C_{\rm ox}}$. From (2)–(4), we can obtain

$$\phi_s''(x) - k^2\phi_s(x) = -k^2\left[V_{GS} - V_{FB} - \frac{Q_{\rm dep}}{C_{\rm ox}} - \frac{qn_s(x)}{C_{\rm ox}}\right] \tag{5}$$

where

$$k^2 = 12C_{\rm ox}/[(6\epsilon_s + C_{\rm ox}y_d)y_d] \tag{6}$$

and $Q_{\rm dep} = q\int_0^{y_d} N_A(y)dy$. The representation of k in (6) is slightly different from that in [13], due to the fact that we integrate y from 0 to y_d in (4) to include the coupling effect of depletion charge. Actually, the terms in the bracket in the right side of (5) is the surface potential of a long channel device. While the device is operated in the depletion region, the electron concentration can be neglected. Therefore, the bracket in the right side of (5) is reduced to $[V_{GS} - V_{FB} - \frac{qQ_{\rm dep}}{C_{\rm ox}}]$, which is just the surface potential under depletion approximation. However, if the gate bias V_{GS} is larger than the threshold voltage V_T, it is nearly fixed at $2\phi_B (= 2\frac{kT}{q}\ln(\frac{N_A}{n_i}))$, the approximated surface potential at strong inversion.

For a damaged MOSFET device shown in Fig. 1, an n-channel MOSFET device with a damaged zone L_d (where interface fixed charges are described by a step function for simplicity) is illustrated. In general, the stress-induced interface charges in an n-channel MOSFET are almost negative charges and/or acceptor-type interface trap. Therefore, the increasing gate bias turns on the damage-free zones before the damaged one. However, no matter what type of the localized interface charge is, in order to turn on this device, the damaged and damage-free zones must be considered separately.

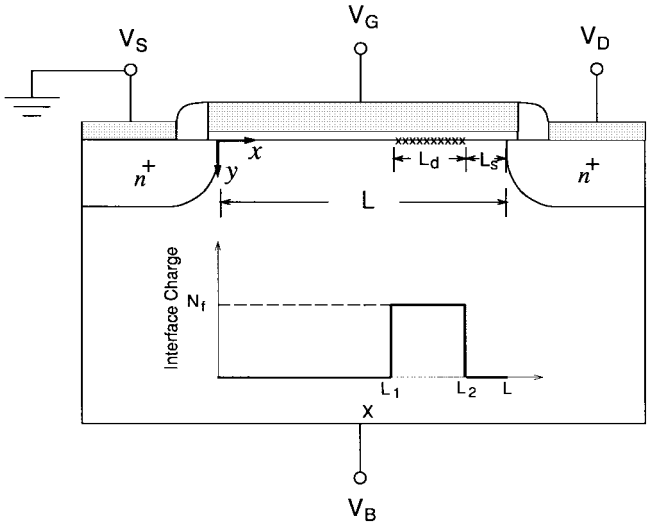

Fig. 1. Illustration of a damaged nMOSFET.

Applying (5) to this device, we have

$$\phi_s''(x) - k^2\phi_s(x) = \begin{cases} -k^2\phi_1 & 0 \le x \le L - L_d - L_s \\ -k^2\phi_2 & L - L_d - L_s \le x \le L - L_s \\ -k^2\phi_3 & L - L_s \le x \le L \end{cases} \tag{7}$$

where $\phi_1 = \phi_3 = V_{GS} - V_{FB} - \frac{Q_{\rm dep}}{C_{\rm ox}}$, which represents the surface potential in the damage-free zones; $\phi_2 = \phi_1 - \frac{qN_f}{C_{\rm ox}}$ is the surface potential in the damaged zone. However, if ϕ_1, ϕ_2, or ϕ_3 are larger than $2\phi_B$, it will be set to $2\phi_B$. Note that the density N_f can be negative or positive for different types of interface fixed charge. Solving (7), the solution of the surface potential is (see the Appendix)

$$\phi_{si}(x) = b_i e^{kx} + c_i e^{-kx} + \phi_i, \quad i = 1,2,3 \tag{8}$$

where b_i and c_i are represented in the Appendix. In general, the threshold voltage is defined as the gate bias at which the minimum surface potential is $2\phi_B$. This definition is also adopted in this paper. In order to calculate the threshold voltage, the minimum potential of (8) is represented as

$$\phi_{{\rm min},i} = 2\sqrt{b_i c_i} + \phi_i, \quad i = 1,2,3\,. \tag{9}$$

If the criterion $\phi_{{\rm min},i} = 2\phi_B$ is used, and substituting b_i, c_i and ϕ_i into (9), we can obtain the threshold voltage

$$V_T = V_{T0} + \frac{qN_f}{C_{\rm ox}}\delta(i-2) - 2\sqrt{b_i c_i}, \quad i = 1,2,3 \tag{10}$$

where $V_{T0} = V_{FB} + 2\phi_B + \frac{Q_{\rm dep}}{C_{\rm ox}}$; $\delta(i-2)$ is equal to 1 for $i = 2$ and 0 for $i = 1,3$, respectively. Note that even though b_i and c_i are functions of V_{GS}, (10) will reduce to the analytic form as proposed in [13] if the damaged zone is vanished. In the cases of the damaged devices, we give an initial guess of $V_{GS} = V_{T0}$ into (10), it will converge after few iterations. Due to the three zones of the device, there are three values of V_T in (10). However, only one of them is the correct value, the others are the larger one or an unreasonable one.

Similar to [13], $Q_{\rm dep}$ and k in (5) are modified and the depletion depth $y_{d,\rm eff}$ (effective depletion depth) is modified as

$$y_{d,\rm eff} = y_d \cdot f \tag{11}$$

where f is the geometric factor of the charge sharing scheme [13,] [14], which is functions of channel length L, substrate bias V_{BS}, drain bias V_{DS} and S/D junction depth R_j.

So far, we have developed the threshold–voltage model for the devices with interface fixed charge. As the interface trap appears at the S_i–S_iO_2 interface, it is known that it will accept an electron if the trap level locates beneath the Fermi level for an acceptor-type interface trap. In this situation, it acts as negative interface fixed charge. Therefore, it can be approximated to equivalent interface fixed charge by

$$N_f = \int_{E_V}^{E_{F\rm inv}} D_{\rm it}(E)dE \tag{12}$$

where $D_{\rm it}(E)$ is the interface trap density per energy interval per area; E_V is the energy level of valence band; $E_{F\rm inv}$ is the Fermi level as the device is operated at threshold voltage, and can be expressed as

$$E_{F\rm inv} = E_V + \frac{E_G}{2} + kT\ln\frac{N_A}{n_i} \tag{13}$$

where E_G is the bandgap of silicon. For a donor-type interface trap, (12) will be integrated from $E_{F\rm inv}$ to E_C(energy level of conduction band) and it acts as positive interface fixed charge. However, E_V in (13) should be replaced by E_C and positive sign will be replaced by negative sign. Similarly, the oxide-trapped charge can be treated as equivalent interface fixed charge if it locates near and not far away from the S_i–S_iO_2 interface. This behavior is very similar to that of interface fixed charge and can be approximated by

$$N_f = \frac{1}{qT_{\rm ox}}\int_{-T_{\rm ox}}^{0}(T_{\rm ox}+y)\rho_{\rm ox}(y)dy \tag{14}$$

where $\rho_{\rm ox}(y)$ is the volume oxide-trap density. In general, the localized distributions of hot-carrier-induced interface traps and oxide-trapped charge densities can be profiled by the well-known charge-pumping technique [10]–[12]. The energy distribution in the bandgap of interface traps is treated by (12) and (13), while the spatial distributions of interface-traps and oxide-trapped charge can be approximated by an equivalent step function by using the principle of charge conservation. Using these simple transformations as described above, we can extend our model to all general cases for hot-carrier-induced damages.

III. Numerical Results and Comparisons

In this section, a 2-D device simulator—SUMMOS [15] is used to verify the validity of the analytic model as described in the last section. The important device parameters used in this paper are listed in Table I. The channel doping of these devices is uniform to simplify the calculation. Using (10), we calculate the threshold voltage of damaged-free device. The threshold voltage of both analytic model and 2-D device simulator are defined by the minimum surface potential equal to $2\phi_B$. The results are the filled circles as shown in Fig. 2, in which the drain voltage is 50 mV. It is shown that the calculation results of the analytic model fits well with the simulation results for fresh devices. These facts indicate that our analytic model is also suited to predict the short-channel effect of the MOSFET's.

TABLE I
The Structure Parameters of Mosfet Devices Used for This Model and 2-D Device Simulator

Gate Oxide Thickness T_{ox}	100 Å
Flat-band Voltage V_{FB}	-0.84 V
Channel Doping N_A	1.0×10^{17} cm^{-3}
S/D Doping N_{SD}	1.0×10^{20} cm^{-3}
S/D Junction Depth R_j	0.2 μm
Interface Charge Density N_f	$\pm 1.0 \times 10^{12}$ cm^{-2}

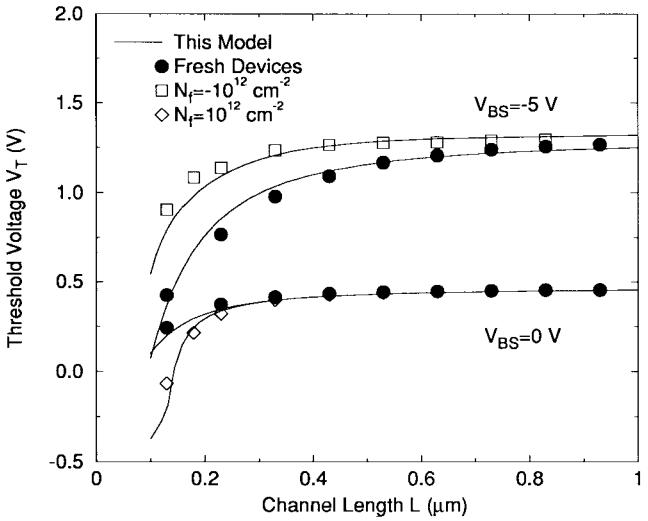

Fig. 2. Calculated threshold voltage versus channel length for both damage-free and damaged MOSFET devices, where the drain bias is 50 mV. The marks are the simulation results while the lines are the results of our model. For damaged devices, the $L_d = 0.1$ μm and $L_s = 0$ μm.

If the interface charge appears in the S_i–S_iO_2 interface or in oxide, as shown in Fig. 1, the surface potential of this device is distorted. As the negative interface charge occurs near the drain side, the surface potential in the damaged zone is lowered. The lower curves in Fig. 3 show that the surface potential is gradually lowered by increasing the extension (L_d) of interface fixed charge but keeping the gate bias at 0 V. The minimum surface potential is therefore shifted from the source side to the damaged zone. Due to the screening effects of built-in potential and applied bias in the drain side, the lowered potential is not considerable until L_d is large. Moreover, the lowered potential becomes saturated as L_d is large enough, this phenomenon reflects to the threshold voltage shown the middle curve in Fig. 4. As L_d is small, due to the influences of built-in potential and drain bias in the drain side, the threshold voltage is only slightly increased. However, while L_d is large enough, the threshold voltage is increased drastically. Finally,

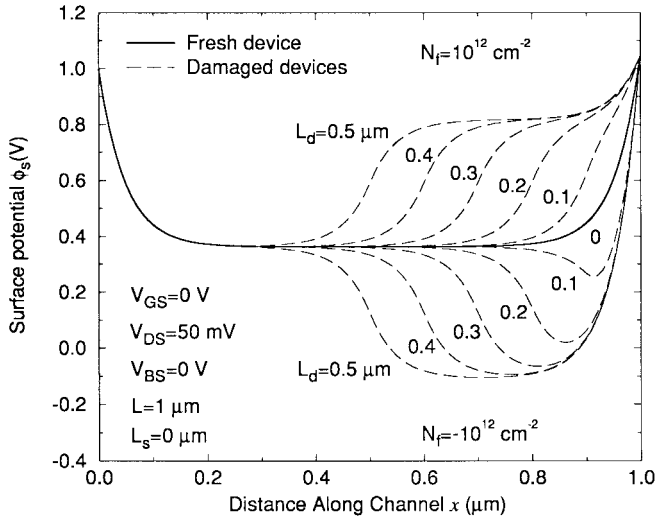

Fig. 3. Surface potential distribution for various extensions of positive (upper curves) and negative (lower curves) interface fixed charge.

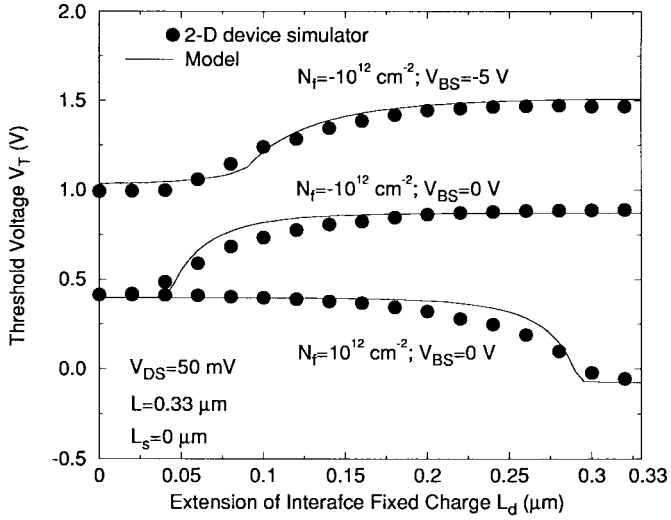

Fig. 4. Threshold–voltage variation versus extension for various conditions.

the threshold voltage is saturated to the value $V_{T0} + \frac{qN_f}{C_{ox}}$, which is the maximum threshold voltage of a given negative interface fixed charge density. As indicated in the upper curve in Fig. 4, it shows the similar results while the substrate bias is raised to -5 V. The difference is that, it needs larger L_d to raise V_T due to the stronger screening effect as the substrate bias is raised.

For a positive interface fixed charge, the surface potential is raised, as shown in the upper curves of Fig. 3. The channel length seems to be reduced and the minimum surface potential is nearly unchanged. Nevertheless, as L_d is large enough or the channel length is short, the minimum surface potential is raised. Therefore, the threshold voltage is unchanged initially and then is lowered as L_d is large. Similar to the negative charge, it becomes saturated to the value $V_{T0} - \frac{qN_f}{C_{ox}}$, which is the minimum threshold voltage of a given positive interface fixed charge density. The lower curve in Fig. 4 indicates these phenomena. As the channel length is shortened, the influences of the damages on the V_T become more apparent, as shown

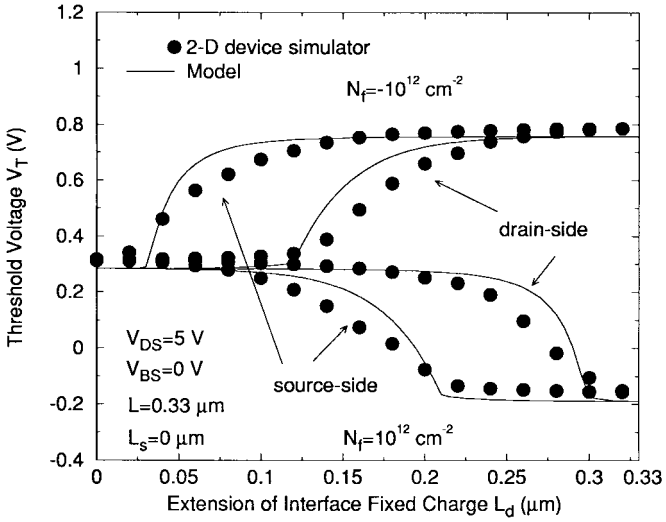

Fig. 5. Threshold voltage variation versus extension for various conditions.

in Fig. 2. As seen from Fig. 2, the negative charge increases V_T even the channel length is long while the positive charge decreases V_T only as the channel length is very short. In either case, the V_T shift increases as the channel is shortened. It can also be easily understood from the explanations as mentioned above.

In general, the position (L_s) of damages for a stressed MOSFET device is located near the drain side, and the reason is that the gate oxide near the drain suffers the most strongest electric field and the high field-induced hot-carriers will attack this region to create permanent damages. However, the device is measured reversely(source and drain exchanged) or worked as a pass transistor, the damages may be regarded as located near the source side. If the drain bias is small, the surface potentials for the interface fixed charge in the source and drain are nearly symmetrical. The position of minimum surface potential for them may be different, but the minimum surface potential is nearly the same for those two cases. As a consequence, the variations of threshold voltage make no difference between the interface fixed charge near the source and drain sides as the drain bias is small. While the drain bias is large, in addition to the built-in potential, the damage near the drain side suffers the strongest screening effect for the drain bias, therefore its influence on V_T is reduced. On the contrary, the damage near the source side only suffers the screening effect for the built-in potential, therefore the threshold voltage raises at $L_d \simeq 0.03\,\mu$m while it raises at $L_d \simeq 0.12\,\mu$m for the damage near the drain side as shown in Fig. 5.

The stress-induced damage is not always located near the drain (or source) side and may be located in the channel region i.e., L_s in Fig. 1 is not zero. For negative interface fixed charge, the screening effects for drain bias and built-in potential are gradually reduced by increasing L_s, the minimum potential is lowered as the solid curves shown in Fig. 6. This effect is apparent, especially as L_s is small or drain bias is large, because the screening effects are large in these cases. The upper curves in Fig. 7 show that the variations of the threshold voltage with the position of the negative interface fixed charge. Note that $L_s = 0\,\mu$m and $L_s = 0.23\,\mu$m

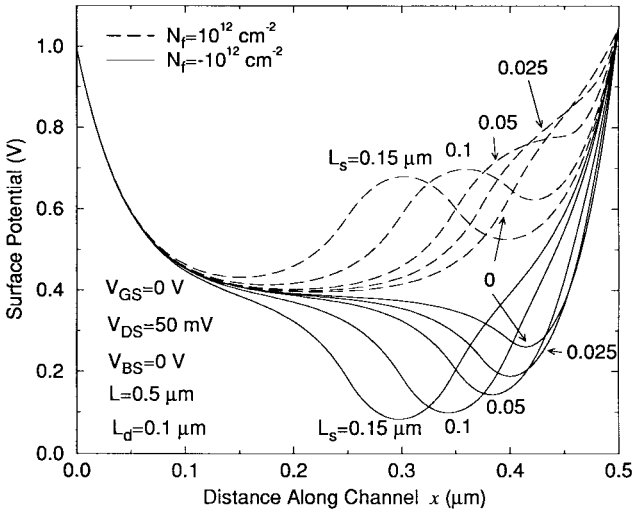

Fig. 6. Surface potential distribution for various positions. The solid and dashed curves are with negative and positive interface fixed charges, respectively.

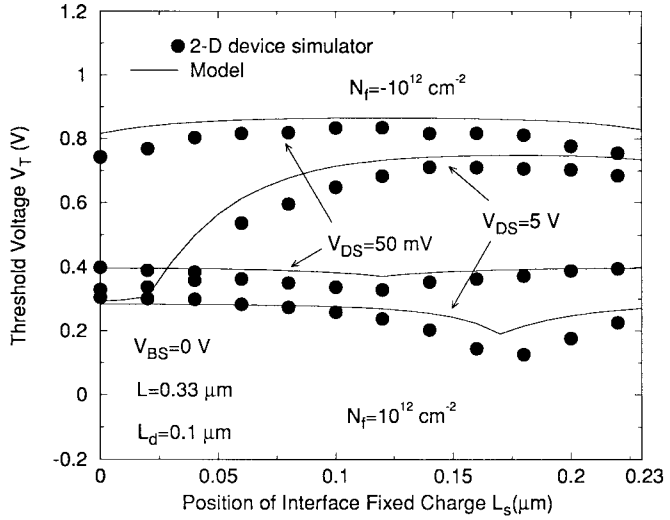

Fig. 7. Threshold voltage versus position for drain bias at 50 mV and 5 V. The upper and lower curves are with negative and positive interface fixed charges, respectively.

represent that the damage is located near the drain and source sides, respectively. As the drain bias is small, the variation of V_T is not apparent. It slightly increases with L_s and then decreases slightly as the interface fixed charge is shifted to the source side, which is nearly symmetrical in the drain side as the drain bias is small. A totally different aspect can be observed for a large drain bias. Because the screening effect in the drain side is much larger than that in the source side, the damage in the drain side will not cause V_T shift much until the damage is shifted toward to the source. As it reaches the source side, V_T is slightly lowered due to the weak screening effect in the source side.

For positive interface fixed charge, as the dashed curves in Fig. 6, the minimum potential is raised as L_s increases. The positive charge acts as a new source of the screening effect. If it is located in the source or drain side, its influence is not apparent as it is located in the center of channel. However,

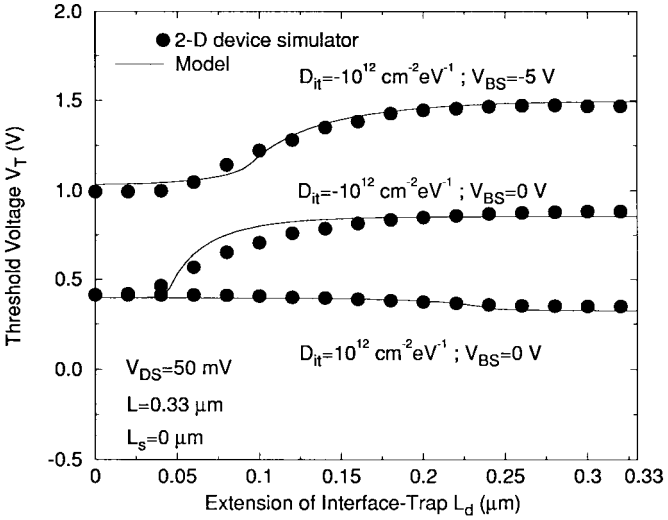

Fig. 8. Threshold voltage variation versus extension for various conditions of interface trap.

as the channel length is small or L_s is comparable to channel length, its strong screening effect is visible. As the damaged zone is gradually moving from the drain side to the center of channel, the minimum potential is located in the source side and is gradually raised as the screening effect of positive interface fixed charge. While the damaged zone is gradually moving from the center of channel to the source side, the minimum potential is located in the drain side and is gradually lowered as the screening effect of positive interface fixed charge is away. Therefore, the threshold voltage in Fig. 7 is nearly symmetrical as V_{DS} is 50 mV. Similar results are expected as V_{DS} is large, except that it is not symmetrical due to the larger screening effect in the drain side than that in the source side.

In Fig. 8, we implement uniform interface trap to 2-D device simulator, and the interface traps are distributed in the bandgap with negative (acceptor-type) and positive (donor-type) $D_{\rm it}$ of $10^{12}{\rm cm}^{-2}eV^{-1}$. For acceptor-type interface trap, according to (12) and (13), the equivalent interface fixed charge is approximated to be $-9.7\times10^{11}{\rm cm}^{-2}$. On the other hand, it is $1.5\times10^{11}{\rm cm}^{-2}$ for donor-type interface trap. Both of their effects on the threshold voltages are well-predicted by our model. It is worth noting that the donor-type interface trap has minor influence on nMOSFET devices unless its density is very high.

IV. Conclusions

Based on the simplified 2-D Poisson's equation, a new analytic threshold–voltage model for a MOSFET device with localized interface charge is derived. The MOSFET device is divided into three zones and each zone has a second-order differential equation. Applying the constraints of potential and electric field continuity to solve these equations, combined with the boundary conditions in the source and drain boundaries, the surface potential is obtained. In addition, the minimum surface potential is set to $2\phi_B$ to define the threshold voltage, the analytic threshold–voltage model is then derived and few iterations are needed to calculate it. In addition,

the interface trap and oxide-trapped charge can be treated as effective interface fixed charge. The derived threshold–voltage model is related to the extension, position, type, and density of localized interface charges, drain bias, substrate bias, and other basic structure parameters of MOSFET devices.

The typical behavior of threshold voltage for damage-free MOSFET device is easily obtained by our model. Simulation results by a 2-D device simulator are demonstrated to verify the validity of this model. The substrate-bias and DIBL effects are also well predicted. As the localized interface charge occurs, the screening effects in the source and drain sides dominate the impacts of localized interface charge on the threshold voltage. The larger drain bias make the screening effect stronger, but the damaged zone out of the influence of the screening effect dominates the threshold–voltage shift. In addition, the calculation results are verified by a 2-D numerical device simulator, and quite good agreements are obtained.

APPENDIX

The continuity of surface potential and electric field in (8) must satisfy at $x = L - L_d - L_s$ and $x = L - L_s$, i.e.,

$$\phi_{s1}(L - L_d - L_s) = \phi_{s2}(L - L_d - L_s) \quad \text{(A-1)}$$

$$\phi_{s2}(L - L_s) = \phi_{s3}(L - Ls) \quad \text{(A-2)}$$

$$\phi'_{s1}(L - L_d - L_s) = \phi'_{s2}(L - L_d - L_s) \quad \text{(A-3)}$$

$$\phi'_{s2}(L - L_s) = \phi'_{s3}(L - L_s) \quad \text{(A-4)}$$

and the boundary conditions at the source and drain edges are

$$\phi_{s1}(0) = V_{\text{bi}} \quad \text{(A-5)}$$

$$\phi_{s3}(L) = V_{\text{bi}} + V_{DS} \quad \text{(A-6)}$$

where V_{bi} is the built-in potential of the source/drain junction. From (A-1) to (A-6), there are six unknown parameters and six independent equations. Therefore, we can solve the b_i and c_i as follows:

$$b_2 = \frac{d_3 d_5 - d_2 d_6}{d_1 d_5 - d_2 d_4} \quad \text{(A-7)}$$

$$c_2 = \frac{d_1 d_6 - d_3 d_4}{d_1 d_5 - d_2 d_4} \quad \text{(A-8)}$$

$$b_1 = \frac{(V_{\text{bi}} - \phi_1)e^{-kL_1} + b_2 e^{kL_1} - c_2 e^{-kL_1}}{2\cosh kL_1} \quad \text{(A-9)}$$

$$c_1 = \frac{(V_{\text{bi}} - \phi_1)e^{kL_1} - b_2 e^{kL_1} + c_2 e^{-kL_1}}{2\cosh kL_1} \quad \text{(A-10)}$$

$$b_3 = \frac{(V_{\text{bi}} + V_{DS} - \phi_1)e^{-kL_2} + (b_2 e^{kL_2} - c_2 e^{-kL_2})e^{-kL}}{2\cosh kL_s} \quad \text{(A-11)}$$

$$c_3 = \frac{(V_{\text{bi}} + V_{DS} - \phi_1)e^{kL_2} - (b_2 e^{kL_2} - c_2 e^{-kL_2})e^{kL}}{2\cosh kL_s} \quad \text{(A-12)}$$

where

$$d_1 = (1 - \tanh kL_1)e^{kL_1} \quad \text{(A-13)}$$

$$d_2 = (1 + \tanh kL_1)e^{-kL_1} \quad \text{(A-14)}$$

$$d_3 = \phi_1 - \phi_2 + \frac{V_{\text{bi}} - \phi_1}{\cosh kL_1} \quad \text{(A-15)}$$

$$d_4 = (1 + \tanh kL_s)e^{kL_2} \quad \text{(A-16)}$$

$$d_5 = (1 - \tanh kL_s)e^{-kL_2} \quad \text{(A-17)}$$

$$d_6 = \phi_1 - \phi_2 + \frac{V_{DS} - V_{\text{bi}} - \phi_1}{\cosh kL_s} \quad \text{(A-18)}$$

$$L_1 = L - L_d - L_s \quad \text{(A-19)}$$

$$L_2 = L - L_s. \quad \text{(A-20)}$$

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