Thermal Analysis of GaN/SiC-on-Si Assemblies: Effect of Bump Pitch and Thickness of SiC Layer

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Abstract

The ever-increasing requirements for high device performance and compact size drive the communications industry to look for new materials, technologies, and integration concepts. This simulation-based study investigates the thermal properties of a compact, heterogeneously integrated gallium nitride on silicon carbide (GaN-on-SiC) and silicon (Si) assembly. Thermal simulations and parametric studies are used to determine how the heat spreading and temperature levels in the lateral and vertical directions are affected by the thickness of the SiC layer and the distribution of the thermal interconnects. Results show that a SiC layer thinned down to 100 μm shows more pronounced differences in its thermal characteristics compared to thicker ones, especially in terms of its backside heating. Aspects related to practical implementations are also considered.

1 Introduction

Current and future communications systems should provide more advanced functionality, improved energy efficiency, and smaller devices. As an example, the upcoming fifth generation (5G) communications systems [1], [2] require better spatial control of the radiated power by means of, e.g., beam steering and other sophisticated techniques. This increases the requirements for the electronics and typically also the power consumption. Combining high power levels and compact designs is not a trivial task, and this has become a hot research topic in the electronics packaging community.

An approach that has become increasingly popular is heterogeneous integration, which combines semiconductor technologies with complementary properties to improve overall performance [3], [4]. An attractive combination is gallium nitride (GaN) that supports high power levels and silicon (Si) that enables high integration density and technical maturity. To allow for more heat transfer from the GaN devices, they are typically grown on a silicon carbide (SiC) carrier with high thermal conductivity.

As a technology, heterogeneous integration can be applied to various radio frequency (RF), integrated circuit (IC) and System-in-Package (SiP) applications [5]-[7]. For proper functionality and reliability, it is important to understand the multi-physical (e.g. electrothermal) properties of the integrated systems to avoid design bottlenecks [8]-[10].

Figure 1 presents a conceptual drawing of a building practice suitable for compact millimetre-wave communications and sensing systems operating at, e.g., 20-50 GHz. In this concept, which utilises the heterogeneous integration of GaN and Si, the low-power and high-density baseband/low-frequency components can be manufactured in a Si process, and power amplifiers (PAs) and other high-power devices can be implemented on the GaN/SiC layer. In a practical application, the Si chip would be fed from the backside with multiple inputs/outputs (I/Os), and a smaller number of I/Os is applied to the GaN/SiC chip. This kind of stacked structure (where an antenna layer is located above the GaN/SiC chip, see Figure 1) helps to reduce both the number of signal interconnects and the overall losses between the different chips. Such a vertical assembly also enables a compact footprint for the entire system.

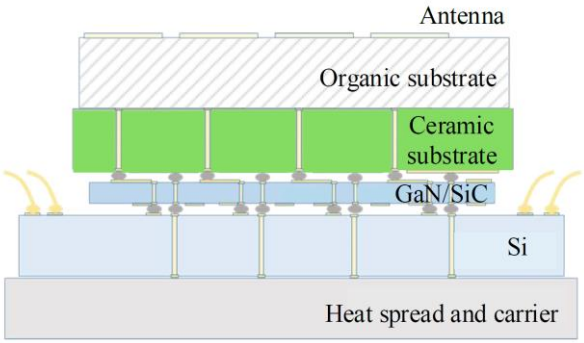


Figure 1. Conceptual drawing of a building practice for wireless communications and sensing applications at mm-wave frequencies. The drawing is not entirely to scale.

This simulation-based study looks at differences in the heat spreading and thermal characteristics of a stacked GaN/SiC-on-Si assembly when the thickness of the SiC carrier and pitch of the thermal interconnects are changed. Numerical and experimental studies on thermal effects in flip-chip based assemblies and GaN devices have been reported in [11] and [12], respectively. For IC applications, effects of the thickness and distribution of through-silicon vias (TSVs) have been investigated in, e.g., [13], [14]. Recently, the thermal properties of different thermal interconnect types

were studied in [15] for a more complicated geometry, but the effect of SiC carrier thickness was not considered.

2 Investigated Stacked Assembly and Research Methodology

The basic design investigated in this work consists of a GaN/SiC chip mounted onto a Si chip using gold (Au) bumps. Thermal simulations are carried out using the ANSYS Icepak software (v. 19.1), and the simulations assume the material properties shown in Table 1.

Table 1: Properties of the materials used in the study.

Material	Density ρ (kg/m^3)	Thermal cond. k (W/m·K)	Specific heat C_p (J/kg·K)
Au	1930	310	125
Si	2330	180	770
SiC	3210	450	1200
GaN	6500	130	490

2.1 Chip Dimensions and Heat Sources

Figure 2 illustrates the principal geometry of the study. The area of the Si chip is assumed to be 7×7 mm^2, and the size of the GaN/SiC chip is 3×3 mm^2 (see Figure 3). A constant thickness of 400 µm is used for the Si substrate. On top of the SiC carrier is a layer of GaN whose thickness is 3 µm. The thermal boundary resistance (TBR) in the GaN/SiC interface is assumed to be $3.3 \cdot 10^{-8}$ m^2·K/W. The TBR is caused by a thin aluminium nitride (AlN) layer needed to grow the GaN layer on the SiC carrier. In a GaN/SiC structure, the bulk SiC material acts as the main thermal carrier [16].

For the SiC carrier, its thickness is varied from 100 to 500 µm with 100-µm steps. The thickest substrate represents a standard thickness for typical commercially available 4H-SiC wafers. In many practical applications, thinned-down substrates are desirable, which motivates the choice of the thinnest case. To complement the analysis, and to see more of how the heat spreading depends on the thickness, additional intermediate thickness values (200, 300, and 400 µm) are investigated. It should be noted that most of the reported results are for the 100, 300, and 500-µm cases.

In the interface between the two substrates, the bottom face of the GaN/SiC chip and the top face of the Si chip are metallised with a thin Au layer, the thickness of which is 2 µm. Considering practical assembly and manufacturing, such a thickness is suitable to connect the GaN/SiC and Si chips using, e.g., thermocompression bonding and stud bumps.

To represent the high-power GaN device, a 10×100 µm^2 heat source is located at the centre of the GaN/SiC chip. The source dissipates a power of 5 W, and the resulting power density causes a very concentrated local hotspot and impractically high temperatures exactly at the source. Outside of the source and in the different layers, the temperature remains at a technologically tolerable level. To represent the connection of the assembly to its thermal surroundings, a fixed heat transfer coefficient of 6000 W/m^2·K is applied to the bottom interface of the Si substrate. This approach gives more accurate results than assuming a fixed temperature [17].

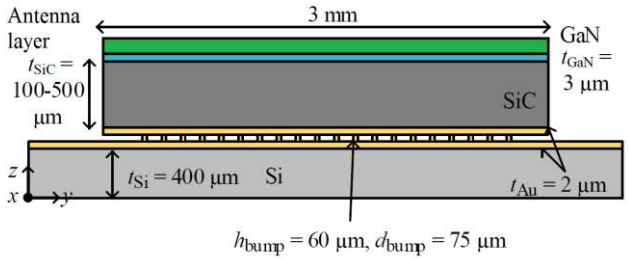


Figure 2. Side view of the investigated stacked assembly. The drawing is not entirely to scale, and the properties of the antenna layer are not considered in this study.

2.2 Distribution of Au Bump Interconnects

Figure 3 presents four different variants of Au bump arrays used to connect the two chips together. The height and diameter of the bumps are set to 60 and 75 µm, respectively, and these values are kept constant throughout the study. These bump dimensions showed good thermal properties in an earlier study [15], and they can also be considered feasible from a practical fabrication point of view. In all cases, the bumps are organised in a regular and symmetric array.

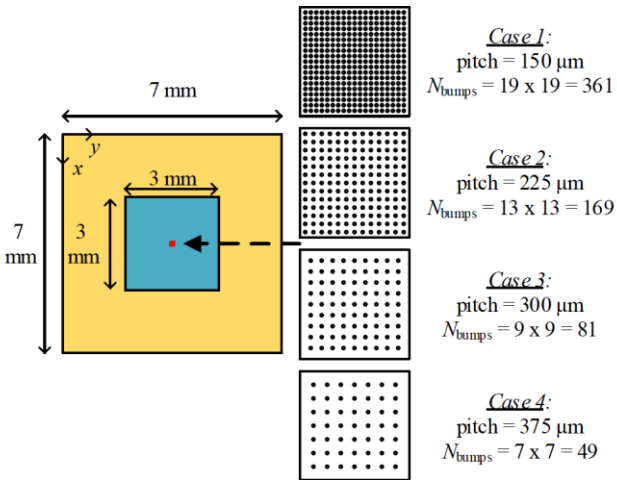


Figure 3. Top view of the assembly and the distribution of the Au bumps at the interface between the GaN/SiC and Si chips. The bump array is fully symmetric. Red square represents the heat source (not to scale).

The configuration of the Au bumps is varied by modifying their pitch as integer multiples of the bump diameter, and the pitch values used are 150, 225, 300, and 375 µm. With these values, the arrays have 19×19 = 361, 13×13 = 169, 9×9 = 81, and 7×7 = 49 bumps, respectively, between the GaN/SiC and Si chips. In all cases, the bump array is symmetric with respect to the centre of the chip, and the centremost bump is always located directly below the heat source.

3 Simulated Thermal Characteristics

For analysing the thermal properties of the investigated assembly, the lateral and vertical thermal characteristics of the structure are studied. This is done by observing temperature profiles and differences at various locations in the assembly. Geometric symmetry in the structure helps to reduce the number of cases to be considered. All dimensions and properties are kept constant throughout the study except for the bump pitch and SiC carrier thickness, which means that the observed thermal effects are mainly caused by these parameters.

3.1 Lateral Thermal Characteristics

The first step in the analysis is to investigate the heat spreading from the source in the lateral direction. Structural symmetry, in terms of the location of the heat source and bumps, allows limiting this study to one lateral path (parallel to the edges of the chips). Figure 4 presents the temperature profile at different layers of the assembly with different substrate thicknesses. These profiles are along a direction that crosses the centre of the GaN/SiC chip and the heat source.

As the substrate gets thinner, the temperature at the bottom layer of the SiC carrier increases in the vicinity of the heat source, and a periodic pattern caused by the bump pitch can be seen in the temperature profile. With the thinnest substrate, the difference in the SiC bottom temperature is approximately 12 °C between the sparsest (pitch = 375 µm) and densest (pitch = 150 µm) bump grids. The symmetry of the bump array is evident from the curves of Figure 4. Having the centremost bump beneath the heat source causes the local minima seen at zero location in all the cases in Figure 4.

Figure 5 compares the temperature behaviour in the top surface of the GaN layer and the bottom surface of the SiC carrier as a function of the bump pitch. As the curves of Figure 5 show, the two thickest substrates have rather similar temperature characteristics. The temperature falls quite rapidly when moving away from the centre, and the largest temperature drop at the top face occurs within 250 µm from the centre. With all substrates, the temperature profile of the bottom face begins to show periodic local minima corresponding to the pitch between adjacent bumps. This effect is most pronounced when the pitch is 300 and 375 µm.

When the SiC carrier is thinned down to 100 µm, the thermal behaviour in the vicinity of the source is different. Temperature drops comparable to those with the thicker chips (e.g. top side temperature) take place across a longer distance, and beyond approximately 100 µm from the source, both sides of the GaN/SiC chip have very similar temperature profiles. Adjacent to the source, the bottom face of the chip experiences more significant heating compared to the thicker substrates. The resulting temperature increase is up to 20 °C both locally (bottom surface of the SiC carrier) and globally (GaN layer; see the curves of Figure 7).

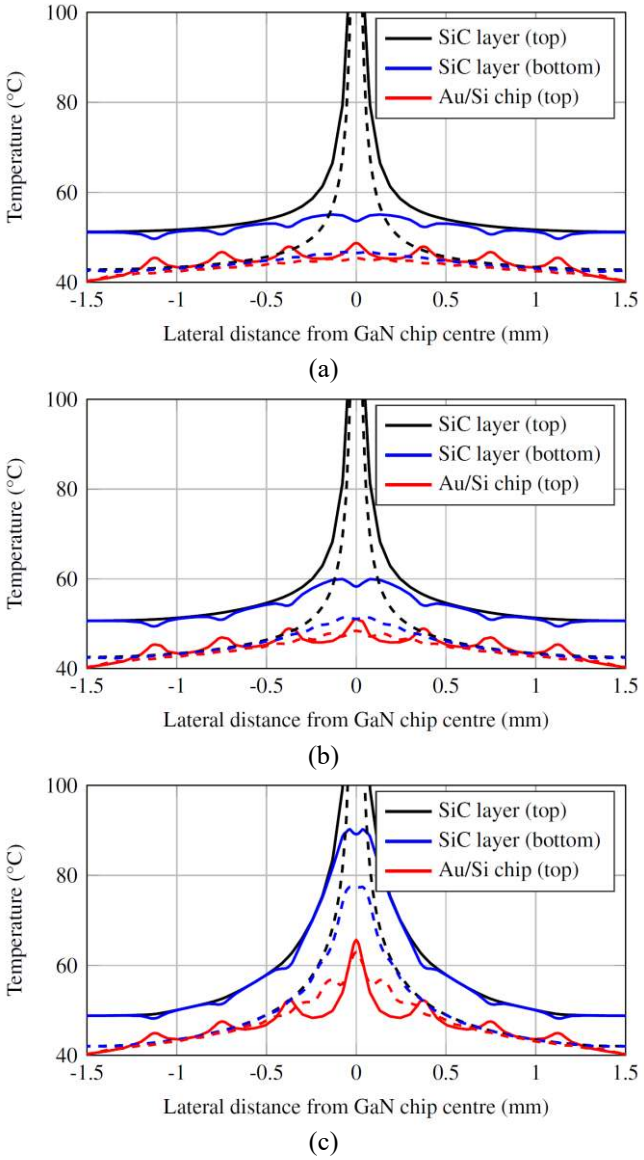


Figure 4. Comparison of temperature profiles at different layers in the assembly when the SiC carrier thickness is (a) 500 µm, (b) 300 µm, and (c) 100 µm. Bump pitch is 375 µm (solid line) and 150 µm (dashed line).

3.2 Vertical Thermal Characteristics

Figure 6 shows the vertical temperature profile through the centre of the GaN/SiC chip (temperature drop from the top surface of the GaN layer to the bottom surface of the SiC carrier). The curves of Figure 6 illustrate that in the vertical direction, the temperature drop between the top and bottom surfaces of the chip is steeper with a thicker carrier. For example, the temperature at the bottom face of the 500-µm carrier is approximately 20 °C lower than in the 100-µm case in the vicinity of the heat source.

Figure 7 presents a close-up of the thermal characteristics in the immediate vicinity of the top layer and GaN/SiC interface within the first 20 µm below the surface. As an example, the case of a 500-µm thick SiC carrier is shown in Figure 7(a). Additionally, the thickness dependence is illustrated for the

150-µm and 375-µm bump pitch in Figures 7(b) and (c), respectively. Apart from slight variations in the absolute temperature levels, the general trend is similar also with thinner carriers. When the SiC carrier is 100 µm thick, the shape of the T_{vert} curves is different, and it displays up to three different slopes across the thickness.

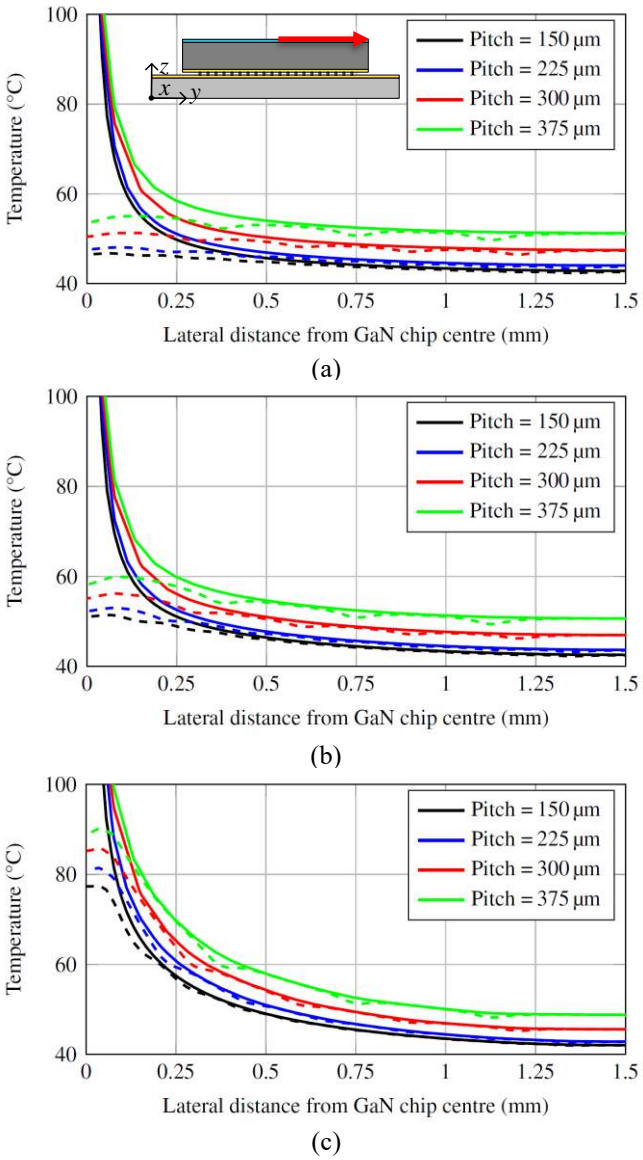


Figure 5. Lateral temperature profiles with different bump pitch values when the SiC carrier thickness is (a) 500 µm, (b) 300 µm, and (c) 100 µm. Solid line: top surface of the GaN layer. Dashed line: bottom surface of the SiC layer. The red line in the inset shows the direction of the temperature profile.

At the geometric centre of the source, the local peak temperature exceeds 400 °C (with the currently assumed value of P_{diss} = 5 W), but the temperature gradient is extremely steep when moving away from this point. The GaN layer is 3 µm thick, and the thermal boundary resistance at the interface affects the thermal properties (seen as a large discontinuity or change of slope in the temperature profile).

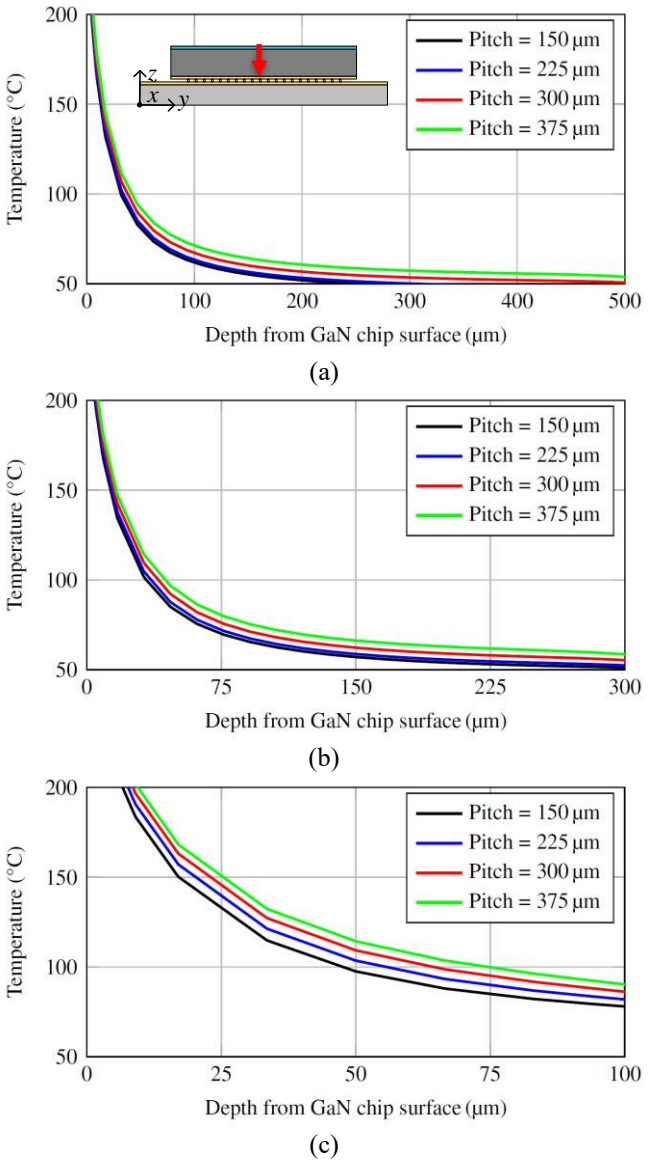


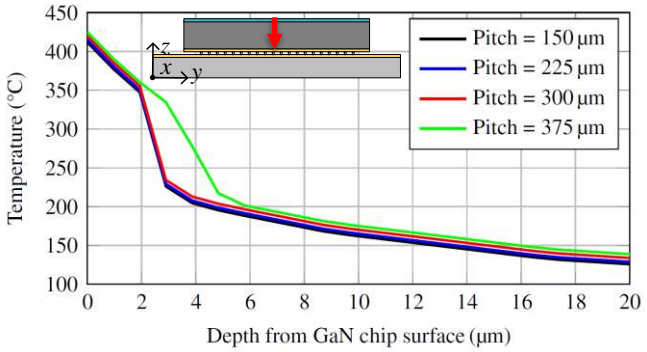
Figure 6. Vertical temperature profiles at the centre of the GaN/SiC chip with different bump pitch values when the SiC carrier thickness is (a) 500 µm, (b) 300 µm, and (c) 100 µm. The red line in the inset shows the direction of the temperature profile.

With all the studied SiC thicknesses, the sparsest bump pitch results in a slightly anomalous behaviour at the GaN/SiC interface. This could be resulting from a locally reduced heat transfer caused by increased distance to the adjacent bump.

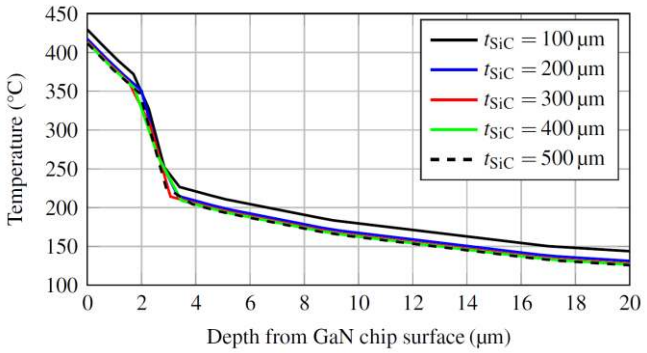
To illustrate the vertical temperature drop at different locations on the chip, Figure 8 represents the vertical temperature difference ($\Delta T_{vert} = T_{GaN,top} - T_{SiC,bottom}$) as a function of lateral distance from the heat source. The curves show that the vertical temperature difference reduces when moving away from the source, as expected, and that the profile is smoother with a denser bump grid.

When reducing the number of the bumps, their individual locations gradually become visible in the temperature profile

as local dips, whose positions correlate well with those of the bumps. With all the investigated substrate thickness and pitch values, the vertical temperature difference is within 2 °C beyond 0.5 mm from the chip centre.



(a)



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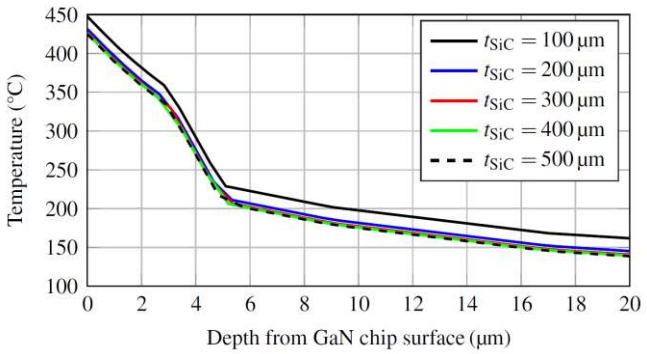
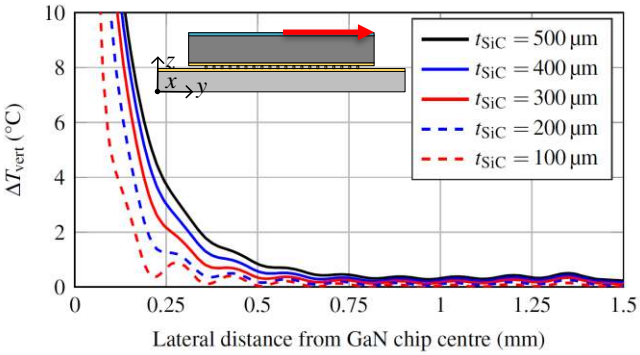


(c)

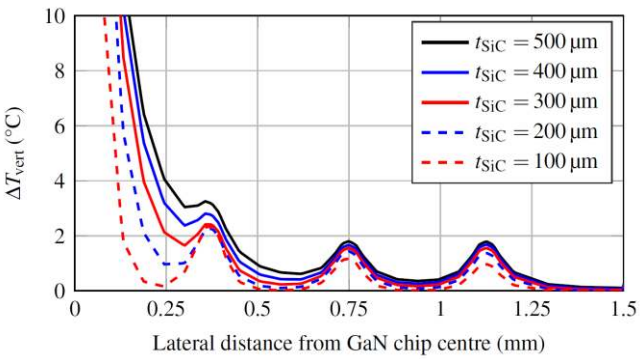
Figure 7. Close-up of the vertical temperature drop in the vicinity of the GaN layer when (a) t_{SiC} = 500 μm, (b) pitch = 150 μm, and (c) pitch = 375 μm. The red line in the inset shows the direction of the temperature profile.

4 Discussion

The observed lateral and vertical thermal effects raise a question of how the thermal characteristics of the studied assembly approach would change if the bump array outside the 0.5-mm radius were sparsened further. From a practical point of view, this is an important aspect as the currently used "ideal", fully populated bump arrays take up a considerable part of the overall chip area and increase the manufacturing costs for commercial implementations.



(a)



(b)

Figure 8. Vertical temperature difference ($\Delta T_{vert} = T_{GaN,top} - T_{SiC,bottom}$) as a function of SiC carrier thickness when the bump pitch is (a) 150 μm and (b) 375 μm. The red line in the inset shows the direction of the temperature profile.

In the present study, the array is only utilised for vertical heat transfer and, to some extent, structural and thermomechanical rigidity (which are outside the scope of this work). A more practical structure would require transferring both heat and RF signals in the vertical direction, meaning that a careful consideration is needed to suitably distribute the available area to incorporate all the required functionalities.

Additionally, the heterogeneous nature of the materials (e.g., different thermal expansion coefficients) used in the assembly can be a problem for the reliability. The structure experiences repetitive heating and cooling cycles during its operation, which causes thermomechanical stress. These aspects should be investigated in a separate study.

It should be noted that some of the assumptions made in the present study, e.g., on the dissipated power and dimensions of the heat source, represent something of a thermal worst-case scenario as the high P_{diss} is constantly on (steady-state result). In practice, the time-dependent properties of the used signals (power level, pulse duration, duty cycle etc.) can alleviate some of the worst problems, but the resulting possible transient thermal challenges also need to be properly considered.

5 Conclusion

This work has investigated how the heat spreading characteristics of a stacked heterogeneously integrated GaN/SiC-on-Si assembly are affected by the thickness of the SiC carrier and the bump pitch. The results show that as the SiC carrier is thinned down to 100 μm, its bottom surface heats up more in the vicinity of a highly localised heat source. With the current bump arrays, none of the studied pitches provides major thermal bottlenecks, but the used arrays can be too ideal for practical purposes.

The outcome of this study provides useful insights for designing compact, integrated, and high-power devices whose operation will not be restricted by thermal constraints. Studies on additional parameters and quantities are still needed for obtaining a more detailed understanding of the investigated lateral and vertical heat transfer problem. Future work also includes implementation of test structures for experimental studies on the thermal properties of the proposed assembly and integration approach.

Acknowledgements

This work was supported by the strategic innovation programme “Smarter Electronic Systems”, a joint effort by the Swedish Government Agency for Innovation Systems (VINNOVA), Formas, and the Swedish Energy Agency, through decision number 2017-01898. The authors would like to thank Mr. P. Ingelhag and Dr. P. Melin from Ericsson AB, Sweden, for providing suitable bump dimensions.

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