

Thermal Characterization of SiC Modules for Variable Frequency Drives

MARZIEH KARAMI¹ (Student Member, IEEE), TIANCHEN LI¹ (Student Member, IEEE),
RANGARANJAN TALLAM² (Member, IEEE), AND ROBERT CUZNER¹ (Member, IEEE)

¹ Electrical Engineering Department, College of Engineering and Applied Science, University of Wisconsin Milwaukee, Milwaukee, WI 53211 USA

² Low Voltage Drives Group of Rockwell Automation, Milwaukee, WI 53204 USA

CORRESPONDING AUTHOR: MARZIEH KARAMI (e-mail: karami.marzieh@gmail.com)

This work supported was supported in part by the Office of Naval Research, under Grant N00014-20-1-2667 and in part by the Midwest Energy Research Consortium.

ABSTRACT Silicon carbide (SiC) devices can exhibit simultaneously high electro-thermal conductivity and extremely fast switching. To perform optimal designs showing the benefits of SiC in achieving efficiency, size, weight, and cost objectives for electric converters design, it is necessary to establish better models for calculating device losses and an efficient thermal model that can be calibrated to consider the nuances of measurement based thermal equivalent circuits. This work's outputs can be used in a power converter multi-objective optimization process or real-time temperature prediction of drives to improve reliability and maximize performance. The proposed modified loss calculation and thermal model demonstrate the SiC power module's advantages to reduce peak junction temperature and power cycling effects. A detailed power loss calculation and thermal model is developed and tested on a 480 V, 186 A, 150 HP variable frequency drive (VFD) with SiC modules. A comparison between the SiC module and an equivalent rated Si module demonstrates the reduction in power cycling effects, particularly at low-speed operation. Infrared (IR) imaging results and analytical explanations of the phenomenon is provided. Power cycle tests show that higher thermal conductivity is not the only reason contributing to the lower temperature ripple in low-speed operation.

INDEX TERMS SiC, variable frequency drive (VFD), power cycling, reverse conduction, low speed operation and thermal model.

I. INTRODUCTION

With SiC based power modules that inherently exhibit low switching losses, high PWM switching frequencies can be obtained. Promising applications include high fundamental frequency motor drives (high-speed turbo-compressors and permanent magnet motor drives), filter size reduction (LCL filter for active rectifier), and audible noise reduction.

Various aspects of SiC-MOSFETs have been discussed comparing with IGBT, such as reducing the converter size and improving power density [1] through increased switching frequency and efficiency. However, the full benefits of SiC MOSFETs to motor drives have not, to date, been adequately identified in the literature. Understanding these benefits in the design phase, particularly when a manufacturer of Si IGBT

based drives is considering making a shift to SiC MOSFET, need to be explored through the increased capability of predicting losses, taking into account the practical impact of third quadrant operation.

Some SiC multi-chip module manufacturers are now eliminating the external parallel SiC junction barrier Schottky diode and using the intrinsic body diode. This change will make it necessary to consider accurate loss calculations.

The method presented in this paper can be applied in the early stages of converter design to improve behavioral models of the loss characteristics over what is provided in datasheets. Future designers can use the models provided in this work and apply them to their SiC converter prototypes. The presented algorithms are efficient and will run well on low-cost

processors, allowing the converter controller to change the switching frequency in real-time based on the predicted temperature.

The simplicity of the provided model will be advantageous when applied in design processes or multi-objective optimizations such as [2] intended to maximize the power density and efficiency benefits of SiC MOSFETs. The loss calculation and thermal model are used to predict the temperature swing of a SiC converter in low fundamental frequency conditions, and it has been shown that because of the reverse current conduction of the MOSFET channel, SiC converters show less temperature fluctuation. The first step to compare the thermal performance of SiC and Si power modules is to calculate switching and conduction losses. MOSFET channels can conduct reverse current, although, in applications with Si MOSFET, a series diode is usually used in combination with the MOSFET to mitigate the noise associated with MOSFET intrinsic body diode reverse recovery [3]. However, SiC MOSFET channels do not have reverse recovery losses, and therefore the intrinsic body diode can share the current with the external parallel diode.

In order to calculate the losses in a SiC MOSFET switch accurately, it is necessary to consider the conduction in the intrinsic body diode of MOSFET. This paper provides a method for calculating SiC MOSFETs' losses, considering the third-quadrant i-v curve characteristics of SiC MOSFETs.

Simplified thermal equivalent circuits that model each layer of a power module as a thermal resistor and capacitor pair are widely used [4] and are usually provided by the vendor datasheets. However, these models oversimplify the thermal capacitance associated with the insulating substrate layers of SiC MOSFET multi-chip modules [5] and often result in a less accurate temperature estimation during transients.

Higher order models are proposed in the literature to estimate the junction temperature rise with a higher degree of accuracy. For example, the finite element method is used in [6] to solve the temperature distribution across a discrete power module model. A third-order model provided in this paper [7] focused on including the effect of electrical properties on the transient responses of SiC MOSFETs. They have connected transient power losses, instantaneous values of current and temperature-dependent electrical resistance, and heat generation. Pulse currents are applied to a power MOSFET, and the junction temperature is measured to find the relation between the value of the electric current, cooling method, and the junction temperature. Curve fitting is used to match the third-order thermal model with the measurements. This model effectively considers the effect of on-resistance change with temperature; however, it only includes the effect of current pulses and does not adequately account for the realistic conditions associated with switching losses and the impacts of DC-link voltage level.

This paper is continued work from [8] that modifies the datasheet thermal model to match the temperature prediction with measurements with minimum possible error. The thermal model is developed for a 1200 V, 300 A SiC MOSFET with

an external diode (CAS300M12BM2) in a VFD and includes switching and conduction losses. Results are compared with a 1200 V, 300 A Si IGBT module (FF300R12KT4).

Low speed operation can cause high peak junction temperature and also high temperature oscillations. Thermomechanical effects of power cycling and temperature ripple concern the layer assembly under the chips and the connections. They lead to fracture initiation and propagation in solders and in the different interface layers of substrates and also wire bonds [9]. Therefore, reduction in temperature swing can increase the lifetime of the modules [10]. Using the developed thermal model, the SiC module has been characterized in low speed operation and it is shown that the temperature swing in the SiC module is reduced because of channel conduction in the reverse current. These results are promising because it shows that SiC converters can be a solution to low speed operation temperature oscillations.

The organization of the paper is as follows. Modifications required for calculating losses in SiC MOSFET converters are provided in Section II. A thermal model, an optimization algorithm for tuning model parameters and validation of the method in a test setup, is presented in Section III. Validation of the thermal model in DC operating conditions is discussed in Section IV. The benefits of using SiC converters in operations with high switching frequencies, low modulating frequency, and full rated current, along with practical issues of running converters with low output frequency and high switching frequency, are examined in Section V. Finally, the conclusion is made in Section VI.

II. LOSS CALCULATIONS IN SiC MODULES

Closed-form expressions are available for calculating losses in two-level converters, and usually, the same expressions of Si converters are used for SiC converters [11]. However, these expressions must be modified for SiC two-level converters because the MOSFET channel can also conduct the current in the reverse direction [12]. The third quadrant i-v characteristics for SiC modules are a combination of the diode and the MOSFET characteristics. The 3rd quadrant i-v characteristics can be found by numerically paralleling the channel i-v characteristics (similar to the first quadrant characteristics) and diode characteristics. The i-v characteristics for CAS300M12BM2 module it is shown in Fig. 1.

A time-based simulation is used to find the conduction losses in the third quadrant. The i-v characteristics of an IGBT module in linear mode can be modeled by a resistance (R_{CE}) and a voltage drop ($V_{CE,0}$), and a similar method can be used for diodes and MOSFET first quadrant. However, at any instant that the reverse current is flowing through the switch, the amount of current flowing through the diode and MOSFET channel must be determined, and based on that, the losses can be calculated. In a half-bridge with Si IGBT modules operating with unity power factor, the upper IGBT switch only conducts current in the positive direction. However, in a half-bridge with SiC modules, the MOSFETs conduct current

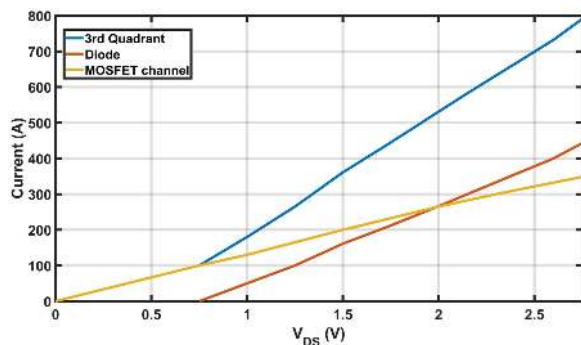


FIGURE 1. i-v characteristics of SiC Schottky Diode and MOSFET of CAS300M12BM2 from the datasheet at gate voltage of 20 V and junction temperature of 150 °C. The 3rd quadrant characteristics can be found by adding diode currents characteristics and MOSFET first quadrant characteristics.

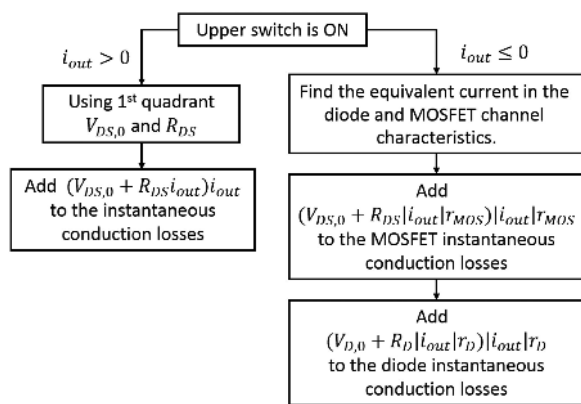


FIGURE 2. The algorithm for finding instantaneous conduction losses in the SiC MOSFET channel.

in both directions, therefore despite common methods of loss calculations, both directions of current must be considered.

The algorithm used for SiC MOSFET conduction loss calculation is shown in Fig. 2. In this algorithm, in positive output current direction, first quadrant i-v characteristics are used to find the instantaneous losses. In this graph, the output current is assumed to be i_{out} . The MOSFET channel in the first quadrant is modeled by a resistance (R_{DS}) and a voltage drop ($V_{DS,0}$). These two values depend on the current value and temperature. For loss calculation during reverse currents, the current is split into the channel current and the diode current. The ratio of the channel current and the diode current can be found from the 3rd quadrant i-v characteristics and diode i-v characteristics. Assuming the total current of i_{out} , the channel current ratio to total current is r_{MOS} and the external diode current to total current is r_D . The external diode is modeled using a voltage drop ($V_{D,0}$) and a resistance (R_D) as well.

Fig. 3 shows the losses with and without considering the third quadrant i-v characteristics in a three-phase inverter with the operating conditions of 650 V DC voltage, an output current of 186 A, and power factor of 0.63. Standard space vector modulation is used. The converter with SiC MOSFET is operated at the PWM frequency of 12 kHz, whereas the

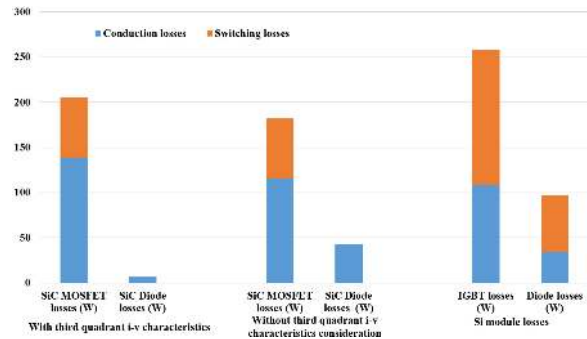


FIGURE 3. Loss calculations for SiC module for operating conditions of Fig. 4 and output frequency of 45 Hz.

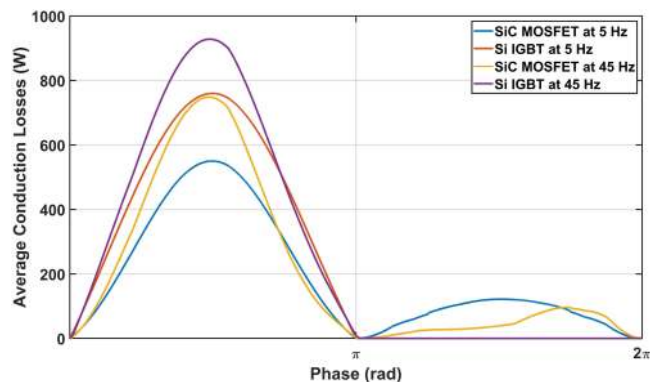


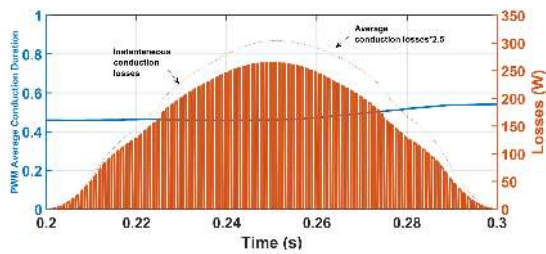
FIGURE 4. PWM cycle averaged loss over a line cycle for different fundamental frequencies. The asymmetry in negative half cycle of current of SiC converter in 45 Hz (yellow trace) is explained in Fig. 5.

Si IGBT converter is run at 8 kHz due to the IGBT junction temperature limit being exceeded at 186 A output current and 12 kHz PWM frequency.

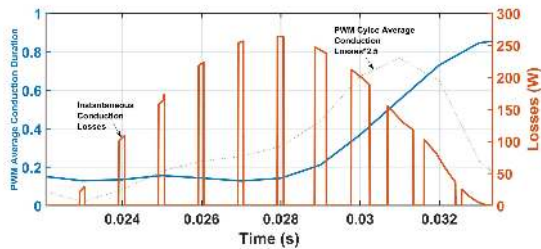
These results show that the external diode in parallel with SiC MOSFET does not significantly contribute to the module losses as it mainly conducts only during the dead-time, and therefore this external diode can be neglected in calculations of losses.

Fig. 4 shows the losses in upper switch of the converter mentioned above. The upper MOSFET has conduction losses during the reverse currents, as it shares the current with the parallel diode. The conduction losses are higher for higher fundamental frequency during positive currents, whereas it is lower for the reverse current direction (comparing yellow and blue trace in Fig. 4). In V/Hz operation, the modulating output voltage has a small value in lower operating frequencies. Therefore, conduction duration or the duty cycle of the upper switch is around 0.5 in low operating frequencies as it is presented in Fig. 5(a) whereas it changes over time with the operating frequency of 45 Hz (Fig. 5(b)). The asymmetry between SiC MOSFET losses in 45 Hz fundamental frequency and 5 Hz as shown in Fig. 3, can also be explained by the duty ratio changes of switches over time for 45 Hz fundamental frequency.

The difference between the average losses in a PWM cycle in the upper switch in reverse current condition for different



(a) Average conduction duration with switching frequency of 1 kHz and fundamental frequency of 5 Hz



(b) Average conduction duration with switching frequency of 1 kHz and fundamental frequency of 45 Hz

FIGURE 5. Losses and conduction duration for different fundamental frequencies, operating conditions of 4 and 1 kHz switching frequency. A lower value of switching frequency is selected to add clarity to instantaneous losses plot. (a) Average conduction duration with switching frequency of 1 kHz and fundamental frequency of 5 Hz. (b) Average conduction duration with switching frequency of 1 kHz and fundamental frequency of 45 Hz.

fundamental frequencies can be explained by the change of conduction duration over time.

The losses associated with the diode stored charge was calculated as $0.5 Q_c V_{DC} f_{sw}$ with Q_c as the total charge of the freewheeling diode. The COSS discharge across the MOSFET was included in the switching loss calculation as well [13].

Switching losses can be calculated similar to Si switches where the time-based simulation decides if switching is happening or not and scales the switching losses with current and voltage value.

III. DERIVATION OF THERMAL MODEL

Required modifications in conventional formulas of calculating losses in two-level converters were discussed in Section II for SiC MOSFET converters. In this section, a method is proposed to modify the thermal equivalent circuits of power modules to match the predictions with measurements in a converter test setup. These modifications are based on an RC thermal network proposed in [14] that account for the thermal interaction between MOSFET and diode chips.

The focus here is on tuning a thermal model that can account for the thermal impedance between diodes and MOSFET [15], is efficient in numerical calculations to enable prediction of temperature in real-time, and can be tuned to match with measurements. Temperature estimation is used for protection and it is very important to have an accurate estimation. To operate the inverter reliably, it is important to make

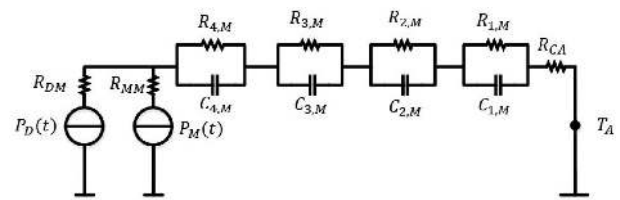


FIGURE 6. Thermal R and C network between MOSFET junction and case layer used to predict MOSFET junction temperature. A similar model is used for the SiC Schottky diode.

sure that the maximum junction temperature is within the allowed temperature.

A simple thermal model has two advantages. One is that in a converter and based on the current and voltage measurements it will enable prediction of the junction temperatures in real time with less numerical calculations burden on the converter's processor. The other advantage is that the inner structure of available commercial power modules limit the ability to measure the temperature oscillations and therefore, it is difficult to derive the parameters of complicated thermal models.

Compact and simple thermal models expressed as thermal RC networks are widely employed to predict junction temperatures rapidly [16]. Individual power devices are considered for more simplicity, and 1-D heat conduction is assumed to predict the junction temperatures. The models are usually constructed using either Cauer cells or Foster cells [17], [18]. Mathematical methods have been developed and well known to transform Cauer cells or Foster cells models from each other. The Foster networks are used as behavior models to calculate the transient junction temperatures, while the R and C parameters in the Cauer networks have true physical meanings [19]. Some of the manufacturers provide RC thermal models that are based on Foster cells. Some other manufacturers only provide the transient thermal impedance values of the junction to the case over time and not the details of the RC model. It should be noted that in either case (RC thermal model or impedance values over time) datasheet models just provide a simplified model that only consider the self-heating of modules and not the thermal cross-coupling between different modules and diodes.

The thermal model used in this paper is shown in Fig. 6, which is based on Foster cells and the thermal model presented in [14] and the coupling between the diode and MOSFET is considered. This coupling is modeled only as a thermal resistance, which does not model the transients.

The thermal resistance between case to ambient (R_{CA}) is measured for the specific inverter used. This resistance is calculated by using known IGBT modules (in which the total losses for specified operation conditions are known) with the specific inverter (Same fans and heatsink) and measuring case temperature (T_{case}). Case to ambient thermal resistance can be calculated as $P_{total} / (T_{case} - T_{amb})$ where P_{total} is the total losses of all the power modules on the same heat sink which can include the three-phase IGBT and diode losses.

The instantaneous junction temperatures T_D and T_M can be found from (1). Equation (1) is based on Fig. 6.

$$\begin{aligned}
 T_M(t) &= T_{net}(t) + R_{MM}P_M(t) + R_{DM}P_D(t) + R_{CA}P_{total} \\
 T_{net}(t) &= T_1 + T_2 + T_3 + T_4 \\
 C_{1,M} \frac{dT_1}{dt} + \frac{T_1}{R_{1,M}} &= P_M(t) \\
 C_{2,M} \frac{dT_2}{dt} + \frac{T_2}{R_{2,M}} &= P_M(t) \\
 C_{3,M} \frac{dT_3}{dt} + \frac{T_3}{R_{3,M}} &= P_M(t) \\
 C_{4,M} \frac{dT_4}{dt} + \frac{T_4}{R_{4,M}} &= P_M(t)
 \end{aligned} \tag{1}$$

The thermal characteristics of a module for average losses and temperature can be modeled as (2) where the thermal interaction between the diode and IGBT has been considered.

In this equation, $T_{D,av}$ and $T_{M,av}$ are diode and MOSFET average junction temperatures, $P_D(t)$ and $P_M(t)$ are the instantaneous losses in diode and MOSFET accordingly with average values of $P_{D,av}$ and $P_{M,av}$ and R_{DC} and R_{MC} are the thermal resistance between diode and case layer and MOSFET and case layer.

The resistance of R_{MC} is equal to sum of thermal resistances of R_{MM} , $R_{1,M}$, $R_{2,M}$, $R_{3,M}$ and $R_{4,M}$ of Fig. 6. A similar circuit can be considered for the diode with R_{DC} as the sum of the total thermal resistance. The losses of $P_D(t)$ and $P_M(t)$ can be calculated based on the time based simulation explained in Section II. P_{total} is the total average losses of all switches mounted on the converter heat sink. This can include all the six power modules of an inverter and the six diodes of the rectifier in an electric drive.

The average junction temperatures of $T_{D,av}$ and $T_{M,av}$ can be measured by an IR camera.

$$\begin{bmatrix} T_{D,av} \\ T_{M,av} \end{bmatrix} = \begin{bmatrix} R_{DC} & R_{DM} \\ R_{DM} & R_{MC} \end{bmatrix} \begin{bmatrix} P_{D,av} \\ P_{M,av} \end{bmatrix} + T_A + R_{CA}P_{total} \tag{2}$$

To match the thermal model of Fig. 6 with datasheet information and measurements, an optimization algorithm is used, which is presented in Fig. 7. The design variables are the thermal resistances and capacitors. The objective is to 1) minimize the error between measured and predicted average junction temperature and 2) minimize the error between maximum junction temperature found from the thermal model of the datasheet and predicted maximum junction temperature. The average junction temperature is measured in a test setup with an open module and an IR camera.

The optimization algorithm receives a series of input parameters such as the switching frequency in which the converter is going to perform at (f_{sw}), total losses of all the power modules on the same heat sink (P_{total}) in (2), and measurements from Open Module Thermal Test (OMTT) and

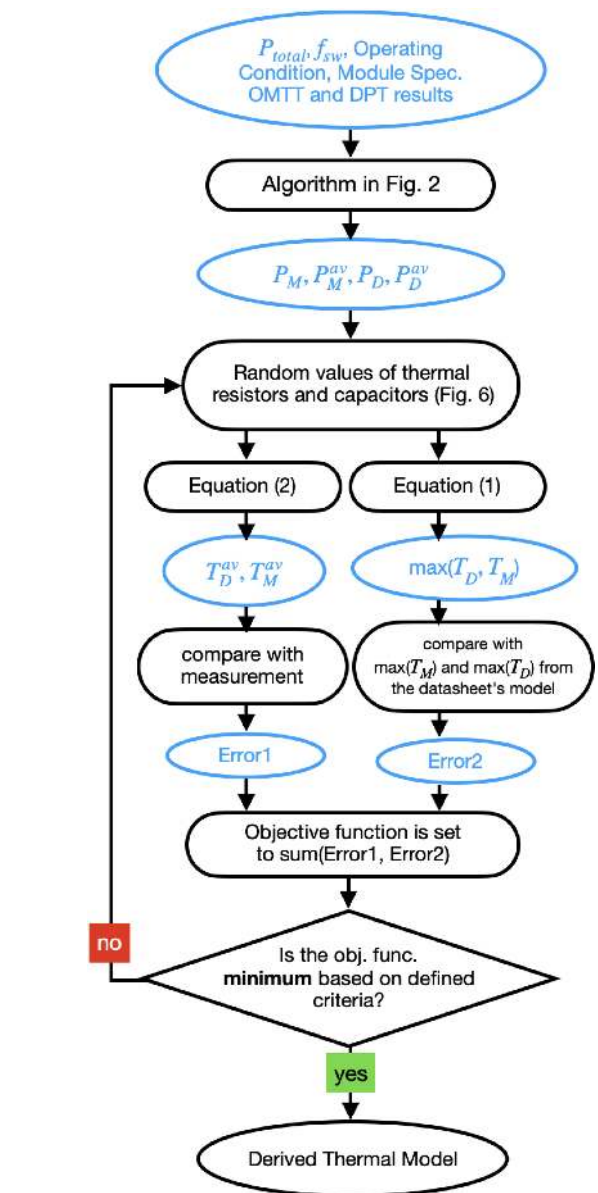


FIGURE 7. Optimization algorithm used for finding the thermal model parameters.

Double Pulse Test (DPT). A set of fundamental frequencies (\vec{f}) are selected to run the optimization algorithm at. These could be sample points within the range of output frequencies that the converter can work at. For all these output frequencies, the average and instantaneous losses of the MOSFET and diode (P_M , P_M^{av} , P_D , and P_D^{av}) are calculated using the algorithm presented Fig. 2. Then for random values of thermal resistors and capacitors with the constraint of $R_{DC} = R_{MM} + R_{4,M} + R_{3,M} + R_{2,M} + R_{1,M}$ average and maximum junction temperature values are found. The maximum junction temperature values are equal to the maximum of the instantaneous temperature values found in (1). The average junction temperature values also can be found either from averaging the instantaneous temperature values found in (1) or directly

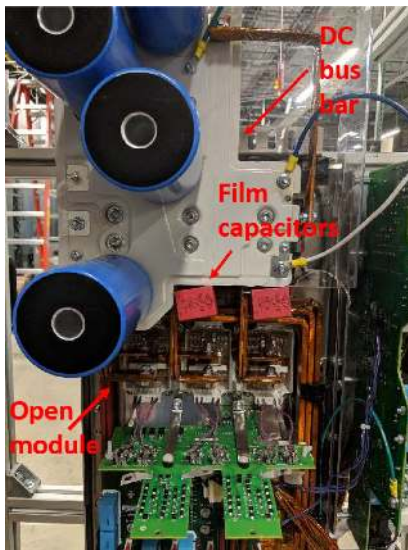


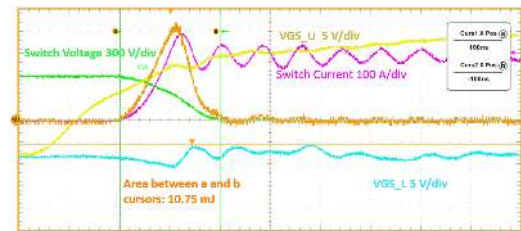
FIGURE 8. Test setup for deriving thermal models of the SiC module.

from (2). The average temperature values are compared with the thermal test measurements $\overrightarrow{Error1}$ and the peak junction temperature values are compared with the maximum junction temperature values found from the datasheet thermal model $\overrightarrow{Error2}$. The objective function is equal to sum of two vectors of $\overrightarrow{Error1}$ and $\overrightarrow{Error2}$. Each point in these vectors correspond to a specific operating frequency. The algorithm will stop when the objective function is minimized.

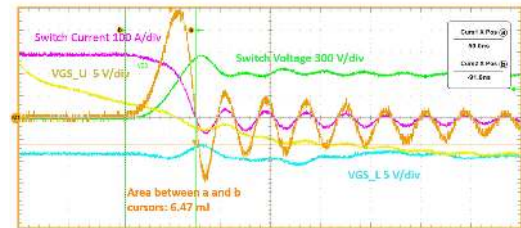
As it was stated earlier, the optimization algorithm is dependent on measuring the average junction temperature. There are different methods used for measuring chip junction temperature. Installing thermocouples on the junction chips can damage the insulation and cause module failure in high voltage applications. Therefore, it is safer to use thermocouples for measuring case temperature and IR cameras for junction temperature measurement. One can use the power modules without the insulation and only apply the low voltage DC, but in that case, the switching losses will be low, and the thermal measurements would not be useful. As the sample module is rated at 1200 V, open module switches need gels to insulate the chips. The gel will add time delay to the measurements, and therefore the measured temperature will be averaged over time. As a result, the measurement of instantaneous peak temperature is impossible for AC operation using an IR camera.

The accuracy of the thermal camera was tested by thermocouples. Thermocouples were placed on a test heat sink and the temperature was measured. Then thermal camera was used to measure the heat sink temperature at the same environment. The camera settings was changed to match the measurements of the thermal camera and thermometer.

The test setup used in this work is shown in Fig. 8. The first step to finding the thermal characteristics of modules is to run the double pulse test at the test setup to find switching losses. The results for this test is different from the datasheet, which can be explained by the fact that the stray inductances



(a) Turn on



(b) Turn off

FIGURE 9. Switching losses in SiC MOSFET. (a) Turn on. (b) Turn off.

TABLE 1. Measured and Estimated Junction Temperature At Different Fundamental Output Frequencies, Output Current of 186 A, DC Bus Voltage of 650 V and Power Factor of 0.63. Normal Space Vector Modulation is Used

f (Hz)	f_{sw} (kHz)	P_M (W)	Measured °C		Estimated °C	
			$T_{D,av}$	$T_{M,av}$	$T_{D,av}$	$T_{M,av}$
45	12	198	62.0	73.0	62.8	73.1
30	12	151	59.7	70.0	61	70.7
15	12	142	58.1	68.1	59.2	68.7
10	12	138	59.2	70.0	59.6	71.0
5	4	86	46.7	54.4	48.0	55.2

are higher in this setup due to the long distance between the open modules and the laminated DC bus bar.

Although film capacitors have been used to lower the DC bus bar inductance to the modules, the stray inductance still can be noticeable. Fig. 9 shows double pulse turn on and off losses measurements, which is different with the datasheet numbers because of the specific bus bar design and the distance between the modules and the bus bar. The double pulse test is done in a closed setup as well, and for the final thermal model of the inverter, the closed setup losses are incorporated.

For modeling the thermal behavior of the module, the inverter was run in different operating frequencies, and the average junction temperature was measured.

The results from running these tests are presented in Table 1 where f is output frequency, and f_{sw} is switching frequency. Fig. 10 shows an example of one of these measurements with the SiC module. Based on the diode and MOSFET average losses in Fig. 3, the temperature inside the diode must be very low. However, MOSFET and diode junction temperatures are measured as 71 °C and 61 °C. This high temperature inside the diode shows that because of the thermal impedance between the MOSFET die and the diode, the diode temperature is comparably high and this shows the importance of using a thermal resistance between MOSFET and diode junction.

The measurement results along with the information about the transient impedance of the power module from the

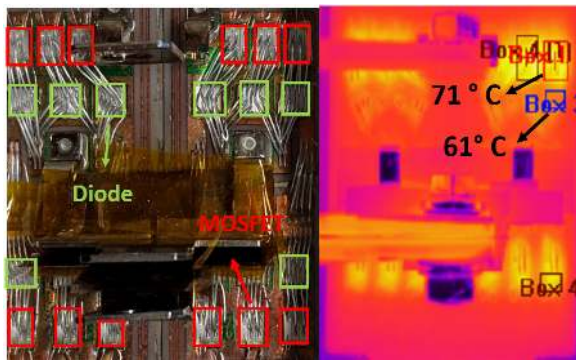


FIGURE 10. Junction temperature for fundamental frequency of 45 Hz, 650 V DC voltage, output current of 186 A, PWM frequency of 12 kHz and power factor of 0.63.

TABLE 2. Transient Thermal Information Provided in the Datasheet for the SiC Module

Time (s)	Transient thermal impedance °C/W
10^{-6}	80×10^{-6}
10^{-5}	550×10^{-6}
10^{-3}	8×10^{-3}
10^{-2}	27×10^{-3}
0.1	53×10^{-3}
0.6	68×10^{-3}
1	75×10^{-3}

TABLE 3. Transient Thermal Impedance of Si IGBT and SiC MOSFET

Si IGBT		
Impedance number	Thermal resistance (K/W)	Time constant (s)
1	0.02418	0.01
2	0.02697	0.02
3	0.03022	0.05
4	0.01163	0.1

SiC MOSFET		
Impedance	Thermal resistance (K/W)	Time constant (s)
$R_{1,M}$ and $C_{1,M}$	1.0513×10^{-5}	1.7765×10^{-5}
$R_{2,M}$ and $C_{2,M}$	0.0041	7.3043×10^{-5}
$R_{3,M}$ and $C_{3,M}$	0.0439	0.0218
$R_{4,M}$ and $C_{4,M}$	0.0504	0.3563
R_{MM}	0.0089	-
R_{MD}	0.0596	-

datasheet can give the input parameters to the optimization algorithm. The optimization algorithm will find the coefficients of (1) and (2).

The information provided in the datasheet about the SiC module used in this paper is summarized in Table 2. Genetic algorithm is used to run the optimization algorithm presented in Fig. 7 and minimize the error between the predicted and measured temperature using the RC circuit presented in Fig. 6. The calculated RC model is presented in Table 3 and the estimated average junction temperature values found from this model are given in Table 1. It can be seen that the thermal model can be adjusted to the measurements with small errors. This model will be verified in DC condition in section IV.

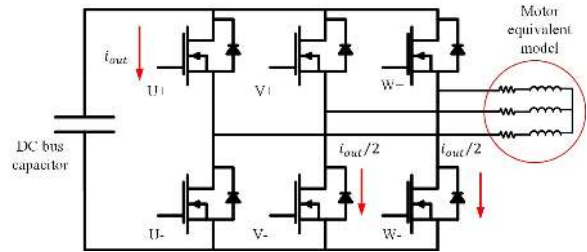
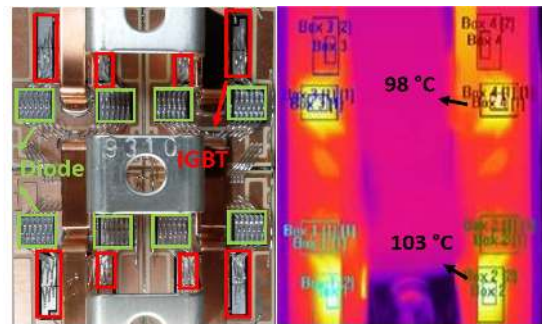
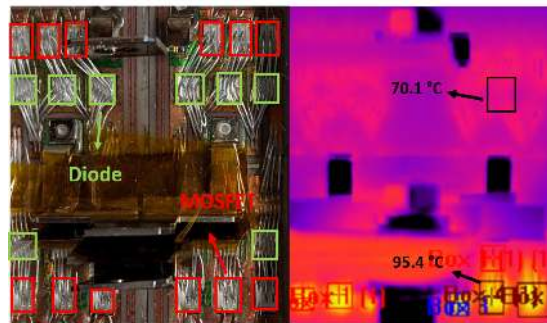


FIGURE 11. Running the converter at DC condition



(a) IGBT module with 2 kHz output frequency at DC operation



(b) SiC module with 12 kHz output frequency at DC operation

FIGURE 12. IR camera measurements for DC operation. (a) IGBT module with 2 kHz output frequency at DC operation. (b) SiC module with 12 kHz output frequency at DC operation.

IV. CHARACTERIZATION OF THE THERMAL MODEL IN DC CONDITION

The average and maximum junction temperature are equal in DC operation. Therefore, the model presented in (2) can be verified by DC operation.

A small DC voltage on the inverter output will result in a high unidirectional current in the inverter as Fig. 11 shows. Different DC voltages can be applied as the reference voltage of the inverter for different combinations of current direction and magnitude in the DC circuit.

Using α, β transformation, if v_α is equal to unity and v_β is set to zero, the current will be in the direction shown in Fig. 11.

Fig. 12(a) and 12(b) shows the IR camera measurements for the IGBT and the SiC module run at 650 DC bus voltage. The current going through the upper module in phase U is 240 A, and it can be seen that the lower diode junction temperature in the IGBT half-bridge is close to the upper switch junction

TABLE 4. MOSEFT Junction Temperature Rise Over Heat Sink for Different DC Conditions

DC test No.	Switch with I_{DC}	Switches with $0.5I_{DC}$	$T_M - T_{case}$ (°C)
1	U+	V- and W-	52
2	W-	U+ and V+	58
3	V+	U- and W-	48
4	U-	V+ and W+	54
5	W+	U- and V-	49
6	V-	U+ and W+	48

temperature. However, only the upper MOSFET junction temperature is high in SiC MOSFET half-bridge, and the diode temperature is 25 °C lower than the MOSFET die. When the upper switch turns off, the current conducts through the lower diode during the dead-time.

After the lower switch is turned on, the current is shared between the diode and the MOSFET channel. The lower MOSFET does not experience any turn-on losses because when the lower MOSFET turns on, there is zero voltage across it as the external diode was already conducting during the dead-time.

The corresponding point to this DC current can be found in the third quadrant of module i-v characteristics to find the conduction losses. It can be calculated that the losses through the lower MOSFET channel and the external diode are equal to 102 W and 57 W, whereas the losses in the upper MOSFET is 462 W.

Table 4 shows the junction temperature measurements for the different current direction of DC current. The value of current (I_{DC}) was 240 A in all the DC tests.

The junction measurements are done for the switch that has the highest current. The junction temperature is different between different switches, although the current in all tests is constant. The reason behind this difference is the placement of the switches on the heat sink and fan direction.

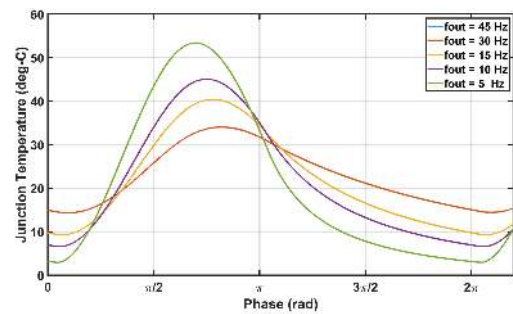
The switch placement can be seen at Fig. 8, and it can be inferred that the lower switch in phase W has the highest thermal resistance between the heat sink and junction.

In order to take this asymmetry into account, a thermal impedance matrix between different switches can be used. However, this model will be too complicated, and this asymmetry is only noticeable at DC conditions. Here, the junction temperature rise over heat sink is averaged, and the impedance matrix of (2) is verified. The average measured temperature is 51.5 °C and the estimated average temperature is 52.5 °C which proves the accuracy of the thermal model.

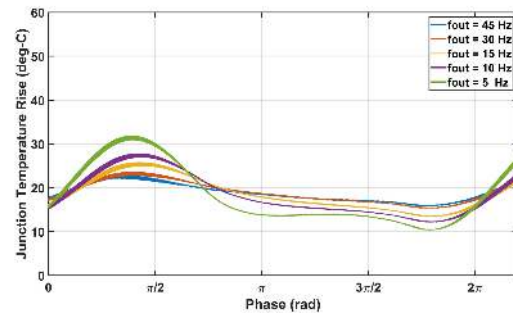
V. LOW-SPEED OPERATION

Voltage-source inverters for AC motor drives have an inherent short-coming for generating full torque at low output frequencies. Low output frequency means low modulation index and low motor speed in V/Hz operation.

If the output waveform fundamental period is comparable to the time constants of power modules, there will be a considerable swing in the junction temperature, and the peak temperature will correspond to the peak power dissipation rather than the average.



(a) IGBT junction temperature rise over heat sink with switching frequency of 8 kHz



(b) SiC MOSBET junction temperature rise over heat sink with switching frequency of 12 kHz

FIGURE 13. Junction temperature oscillations at different fundamental frequencies without considering the cross thermal coupling between the modules and the diode. (a) IGBT junction temperature rise over heat sink with switching frequency of 8 kHz. (b) SiC MOSBET junction temperature rise over heat sink with switching frequency of 12 kHz.

Peak junction temperature will limit the maximum output current, whereas the swing in junction temperature (power cycling) will reduce the life of the power module [20].

Various solutions have been proposed to decrease the high junction temperature of low operation frequency. Many of these solutions are based on alternatively clamping the output to the negative and the positive rails of the DC bus [21] depending on the current direction. Considering the V/Hz operation, the fundamental voltage magnitude is relatively small in low-speed operation conditions. Therefore, clamping the output to the negative and positive rail of DC voltage will result in voltage pulses with low dwell time.

Two issues can arise from these modulation methods with low pulse duration voltages. One is the difficulty of implementation, and the other one is long cable applications. The controller and also the driver circuits have inherent propagation delays that make the implementation of the short duration pulses impossible. For long cable applications, narrow pulses could result in high peak motor voltage due to the reflected wave phenomenon [22].

SiC modules can provide the opportunity to lower junction temperature peak values and ripple. Fig. 13 shows the temperature oscillations for different output frequencies for the SiC MOSFET and IGBT module at the operating conditions of Fig. 10. It can be seen that the temperature swing is less in SiC module.

TABLE 5. The Ratio of Maximum Temperature to Average Temperature for the Si IGBT and SiC MOSFET

f (Hz)	IGBT $T_{M,max}/T_{M,av}$	MOSFET $T_{I,max}/T_{I,av}$
45	1.32	1.22
30	1.45	1.25
15	1.79	1.39
10	2.03	1.52
5	2.44	1.76

From the detailed information of the transient thermal model in Table 3, it can be seen that the longest time constant of the SiC thermal model is 0.3563 s, which is longer than Si IGBT. Therefore, the temperature swing must be higher in SiC MOSFET. However, because of channel conduction in the reverse direction, this swing is smaller.

Table 5 shows the ratio between maximum junction temperature and average junction temperature found for the SiC MOSFET and Si IGBT. $T_{I,max}$ is the maximum IGBT junction temperature and $T_{I,av}$ is the average IGBT junction temperature. These results show that the temperature swing is smaller in SiC MOSFET modules for lower operating frequencies compared to Si IGBT modules. This will allow the operation of SiC modules at full torque low speed operations. However, using SiC power modules and consequently high switching frequency can cause an issue in low speed operation. Current-based dead-time compensation methods result in distortion in low fundamental outputs and high switching frequencies.

Fig. 14 shows the output current at different fundamental and switching frequencies and operating conditions of 45 Hz, 650 V DC voltage, the output current of 186 A, and power factor of 0.63. It can be seen that the output current is distorted, especially at higher switching frequencies.

In higher switching frequencies, the dead-time duration can be comparable to the switch duty cycle. Dead-time Compensation (DTC) is supposed to tackle this effect.

The dead-time compensation used in this inverter control is based on [23]. As this method and a lot of other similar dead-time compensation algorithms [24] are based on current polarization, measurement errors, current ripples, and discontinuous current conduction can disrupt the current spectrum.

Assuming the current direction cannot be accurately detected for $-10 < i_{out} < 10$, for an output frequency of 5 Hz and output current of 186 A, that means that the dead-time compensation algorithm will result in arbitrary results for 2.4 ms although in the output frequency of 45 Hz that is reduced to 0.26 ms which is almost negligible.

The dead-time can be reduced in order to decrease the effect of dead-time on the output spectrum. However, it is necessary to check the switch turn off time for different current conditions for this adjustment.

Fig. 15 shows measurements of gate turn off time for different output currents. These measurements need to be done for both upper and lower switches in the half-bridge converter as they have different turn off times. The propagation delay between the gate and the control circuit needs to be counted in too. Based on the maximum measured turn off time of 905 ns

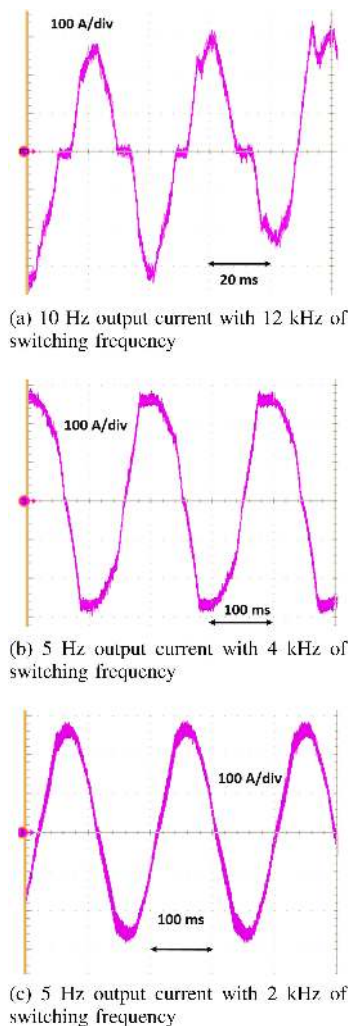
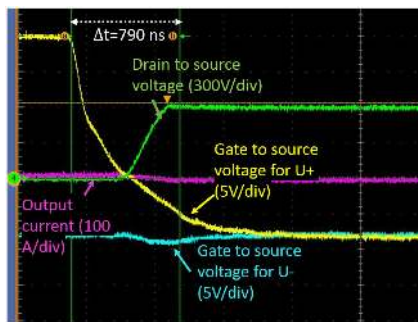


FIGURE 14. Current distortion in low fundamental frequency and high switching frequency. High dead-time values Current based dead-time compensation methods are the reason behind the distortion. (a) 10 Hz output current with 12 kHz of switching frequency. (b) 5 Hz output current with 4 kHz of switching frequency. (c) 5 Hz output current with 2 kHz of switching frequency.

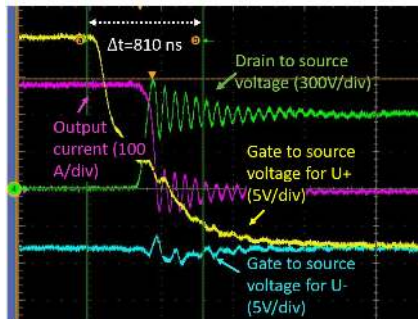
and considering gate driver delay, dead-time was reduced from $2\mu\text{s}$ to $1.5\mu\text{s}$.

VI. CONCLUSION

Junction temperature prediction is essential for determining the maximum possible current rating of a converter. It requires the correct calculation of losses inside the switches and developing an accurate thermal model. This paper includes an algorithm for calculating conduction losses of a SiC MOSFET. Furthermore, a simple RC based thermal model and an algorithm to adjust it to measurements and datasheet parameters are proposed. Finally, based on the tuned thermal model, third quadrant characteristics on the temperature swing of a module are analyzed. It has been shown that SiC temperature swing is less than IGBT modules, and it can be used as a solution to low-speed operation temperature oscillations. These results prove that SiC inverters can be used for high torque and



(a) Turn off time for 20 A output current in U+



(b) Turn off time for 300 A output current in U+

FIGURE 15. Turn off time for different output currents and lower and upper switches. These measurements do not show the gate circuit and communication delays. (a) Turn off time for 20 A output current in U+. (b) Turn off time for 300 A output current in U+.

low-speed applications because of high thermal conductivity and reverse current conduction capability. dead-time issues of low-speed operating drives with high switching frequency and the accurate setting for using voltage-based dead-time compensation algorithms are discussed. The proposed thermal characterization method can guide heat sink and cold plate designs and enables power converter optimization efforts.

ACKNOWLEDGMENT

Any opinions, findings, and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of these institutions.

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