Thermal Component Models for Electro Thermal Analysis of Multichip Power Modules

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***Abstract*— Thermal component models are developed for multi-chip of insulated gate bipolar transistor (IGBT) power electronic modules (PEM) and associated high-power converter heat sinks. The models are implemented in SABER†† and are combined with the electro-thermal IGBT and diode models to simulate the electro-thermal performance of high power converter systems. The thermal component models are parameterized in terms of structural and material parameters so that they can be readily used to develop a library of component models for the various commercially available power modules. The paper presents model development and implementation in SABER††, simulation results, and validation using experimental data.**

Keywords—electrothermal model; electrothermal simulation, multichip; component models, direct-bonded-copper, heat sink.

I. Introduction

Integrated virtual prototyping tools for power electronic systems will allow industry to bring schedules, performance, tests, support, production, life-cycle costs, reliability prediction, and quality control into the earliest stages of the product creation process. This will result in faster time-to-market and better quality for new power electronic products.

The electrical characteristics and reliability of integrated power electronic modules (IPEM) can be greatly influenced by the temperature distribution inside the module. Therefore, to evaluate IPEM performance, it is important to have accurate models to predict its electro-thermal behavior.

An electro-thermal simulation methodology using the Saber†† simulator has previously been introduced for discrete power devices and packages [1,2]. In this methodology, the simulator solves for the temperature distribution within the semiconductor devices, packages and heat sinks (thermal network) as well as current and voltages within the electrical network. The interface between the thermal and electrical networks is through the temperature dependent device models [3]. The device model has terminals that are connected to the electrical network and a terminal connected to the thermal network. The thermal network is the interconnection of compact thermal component models where each model represents an indivisible building block used by the designer to form the thermal network. The modular structure of the models allows the designer to interchange different thermal components and examine different configurations of the thermal network easily and allows development of standard component libraries for simulation software such as Saber††. Furthermore, the output of the thermal model can be used to predict thermal stresses, evaluate operation within maximum ratings, and analyze IPEM long-term reliability.

The previously developed thermal network component models [2] are not applicable to high power modules because the high power devices contain multiple chips within the same package, require heat conduction through the electrical isolation layers, and are typically used with large multi-module heat sinks that have a highly non-uniform surface temperature. The purpose of this work is to develop the models required to extend the Saber†† electro-thermal simulation methodology to power electronic systems that utilize multi-chip power modules. Methods used to develop temperature dependent models for power semiconductor devices are described in the literature, see for example [3].

In this paper, we present the development, implementation, calibration, and validation of a compact electro-thermal model for an IPEM and cooling system. Detailed modeling of IPEM thermal interactions is achieved by application of the heat

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transfer equation to model heat flow through complex geometries. The numerical solution of the heat flow equation is achieved by finite difference methods (FDM) implemented through Saber†† system variables. The implemented thermal component models are parameterized in terms of structural and material parameters to facilitate parametric generation of thermal component libraries for commercially available IPEMs and Center for Power Electronic Systems (CPES) Generation I and II IPEMs.

The thermal component models for IPEM packages and cooling systems developed in this paper are combined with electrical models of the power electronic system to self consistently simulate the electrical, thermal and time dependence aspects of a high-power three-phase inverter. The thermal network component models for the package and heat sink use the power losses computed from the electro-thermal models for the IGBT and diode chips as input to compute the temperature distribution within the thermal network. The IGBT and diode models use the instantaneous chip surface temperatures computed from the thermal network to compute the temperature dependent electrical characteristics. This is illustrated in Fig. 1.

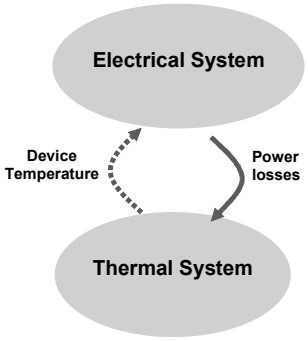

Figure 1. Electro-thermal modeling.

II. IPEM Electro-thermal Model Development

In this section, the techniques used to develop and to implement the thermal network component models in Saber†† for the IPEM paralleled silicon chips, electrical insulating layer structure, and base-plate are briefly described.

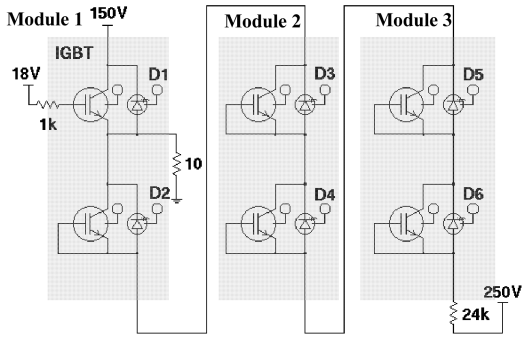

Figure 2. Saber electrical model of the experimental system.

Figs. 2 and 3 show the three-phase inverter electro-thermal model developed in this work to demonstrate and validate the multi-chip power module package and multi-module heat sink thermal models. Fig. 2 shows the electrical model for the three-phase inverter as implemented in Saber††. The inverter uses three half-bridge IGBT modules mounted on a common heat sink. In this test, only one of the IGBTs is operated in a power-dissipating mode and the diodes of the remaining switches are used to monitor the local device temperatures within the modules. Power dissipation in the active IGBT is achieved by operating the IGBT in the active region, and a high power 10 Ω resistor is used for feedback stabilization. The diodes are biased with constant currents as shown, and all voltage points are monitored by an automated data-collection system. The additional terminal shown in the diodes and IGBT correspond to the thermal terminal.

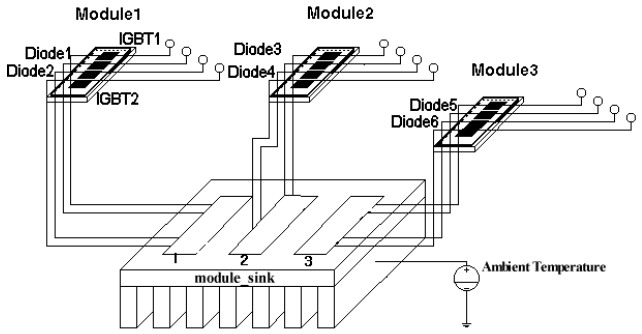

Figure 3. Saber thermal network of Experiment.

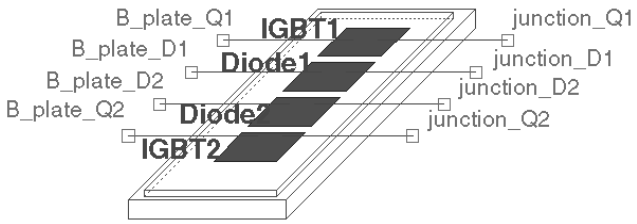

Figure 4. Symbol of the Power Electronic Module in Saber.

The thermal terminals indicated in the electrical circuit Fig. 2 are connected to the chip surface temperature points in the thermal network shown in Figs. 3 and 4. In each electro-thermal semiconductor model, a portion of the electrical power delivered to the device electrical terminals is dissipated as heat. The dissipated power calculated by each electrical model supplies heat to the surface of the respective silicon chip thermal models through the thermal terminals. The connection "junction_XX" shown in Fig. 4 are connected to the corresponded device (Q1, Q2, D1, D2) specified by the "XX" and the "B_plate_XX" are the connections from the baseplate to the module to the heat sink to complete the thermal network.

The instantaneous temperature at the surface of each silicon chip, calculated by the thermal network, is used by the electro-thermal semiconductor model to calculate the

electrical and power dissipation characteristics. In this way, the thermal network response is directly related to the power dissipation, and the electrical characteristics of the system are temperature dependent.

As indicated in Fig. 3, the thermal component network for the three-phase inverter consists of three IPEMs that are placed at specific locations on the heat sink. Each half-bridge IPEM module consists of four sets of paralleled chips comprising the upper and lower IGBTs and freewheeling diodes as shown in Fig. 5. The chips are arranged on insulating direct-bonded-copper (DBC) layers within the module. Each set of paralleled IGBT chips shares a DBC layer structure with its free wheeling diode paralleled chip set. The two DBC layers with their associated chips are mounted on the module baseplate. Fig. 6 shows the thermal path between a chip and the baseplate through the different materials layers of the DBC. Each layer has different thermal properties that must be included in the thermal model.

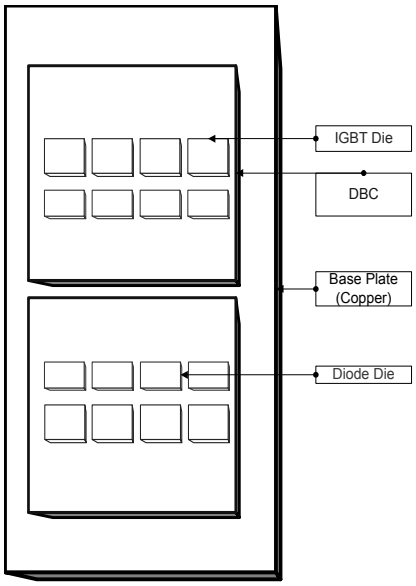

Figure 5. Internal Layout of a commercial IPEM.

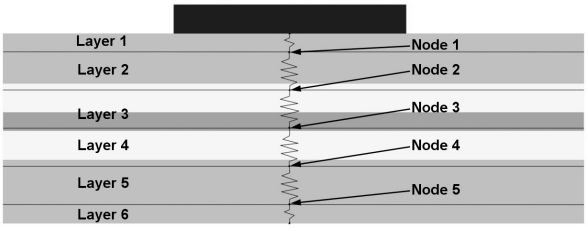

Figure 6. Direct Bonded Copper (DBC) layer structure.

In the development of the compact model for the power module, the module is divided into different regions that form thermal component building blocks. The thermal component building blocks approach aids in reusing blocks for common elements in the structures and for reconfiguring the blocks to model different classes of modules. These thermal component building blocks are transparent to the user of a module thermal component model as only the external connections and internal dimensions need to be specified for the thermal network. For the half bridge module structure of Fig. 5, the vertical heat flow is divided into four basic paths; one for each set of paralleled chips. Each of the heat flow paths contains a building block for the chip, DBC, and baseplate.

This formulation is possible in the case of power devices because the thickness is small compared to other dimensions and heat is generally dissipated uniformly across the surface of the paralleled chips and flows vertically toward the heat sink. We take advantage of this to model the heat transfer process as a quasi-one-dimensional process with lateral coupling using the rectangular-coordinates heat equation:

$$K\frac{\partial^2 T}{\partial x^2} = \rho c\frac{\partial T}{\partial t}. \qquad (1)$$

with boundary conditions,

$$SK\left.\frac{\partial T}{\partial x}\right|_{X=0} = -P_{in}(t) \;\; \alpha\nu\delta \;\; T(t, x = L_o) = T_{in}(t).$$

where K is the thermal conductivity, ρ is the mass density, c is the specific heat, P_{in} is the power dissipation input, S surface area, L_o vertical length and T_{in} outside temperature [4].

Using the components geometry, the nonlinear thermal properties of the material and other non-linear heat transport mechanisms such as convection, the thermal network component models are derived from finite element discretization of (1). The three-dimensional heat flow is accounted for using the appropriate symmetry in the discretization in each region of the component using the effective heat flow area approach. This is used to derive expressions for the two-dimensional network of thermal resistances, thermal capacitance, and the heat energies. The grid spacing is made to increase logarithmically with distance from the heat source to minimize the number of thermal elements required to accurately represent the heat flow for the full range of application conditions.

III. Implementation in Saber

A. Silicon Chip thermal model

The silicon chip thermal model is a standard library component in the Saber†† software and it is based upon the rectangular coordinate heat diffusion equation and includes the nonlinear thermal conductivity of silicon. The details of the model are given in [2].

B. Package Thermal Model

The discretized heat equation of the package thermal model is formulated similarly to the silicon chip thermal model except that the expressions used to calculate the

thermal resistances, thermal capacitances, and the heat energies are different. The package model describes the two-dimensional lateral heat spreading, the die attachment thermal resistance, and the heat capacity of the package periphery. In accordance with the logarithmic grid spacing principle, the DBC model of the package includes five thermal nodes in the heat conduction path from the package header toward the base plate, also exists two more nodes in the base plate toward the heat sink. The package periphery is modeled as an additional thermal node that is not in the direct heat conduction path and accounts for the remainder of the heat capacitance outside of the main heat conduction path. The parameters for the generic package thermal model include the chip area, the location of the chip on the package header, the width of the header, the length of the header, and the thickness of the header. Based upon these parameters, the discretization coefficients are calculated in the parameters section of the template and can be listed when the templates are loaded by setting appropriate options in the program.

Thus, various package component models can be generated from the generic package template by specifying structural and material parameters, and the user does not need to calculate the internal thermal resistances and thermal capacitances.

The lateral heat spreading in the package results in an effective heat flow area that increases with depth into the package. In the model, the effective heat flow area at each depth into the package is obtained by combining the components of heat flow area due to the cylindrical heat spreading along the edges of the chip, the spherical heat spreading at the corners of the chip, and the rectangular coordinate component of heat flow directly beneath the chip.

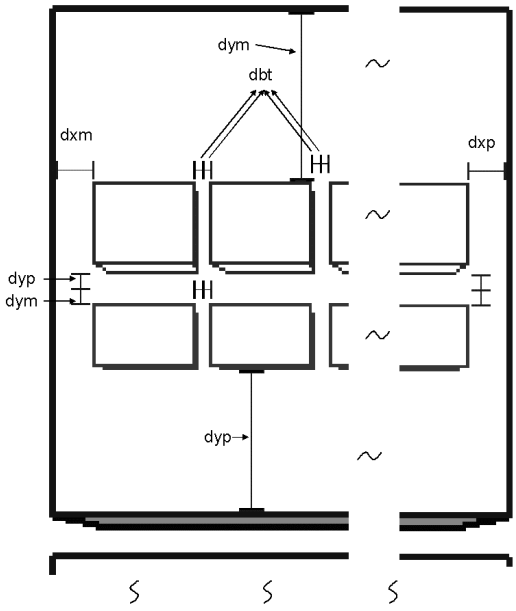

Figure 7. Definition of boundary variables.

Because the heat does not spread laterally beyond the edges of the package, the radius that the heat spreads beyond each edge of the chip (rxp_i, rxm_i, ryp_i, rym_i, rbt) is limited in the model for each node at depth z_i by the distance from each edge of the chip to the edges of the package (2). The boundary between the parallel chips (*dbt*) exists because each one generates the same amount of heat, and is located right in the middle between chips. The boundaries to the adjacent bodies and the edge of the package are represented by *dxp, dxm, dyp, dym, dbt*. Fig. 7 shows the location of the boundaries in a section of the multi-chip package module, the location of the radius that the heat spreads (rxp_i, rxm_i, ryp_i, rym_i, rbt) are in the same direction of the corresponding boundary, for example rxp_i is in the same direction as *dxp*.

$$rxp_i = \begin{cases} z_i & \text{for } z_i \le dxp \\ dxp & \text{for } z_i > dxp \end{cases}. \quad (2)$$

We consider cylindrical and spherical components when quantifying the heat flow area. The cylindrical component of the heat flow area is given by the areas of the one-quarter cylinders at each edge of the chip:

$$Acyl_i = \frac{\pi}{4} W_{ch}(rym_i + ryp_i) + n\frac{\pi}{4} L_{ch}(rxm_i + rxp_i) + (n-1)\frac{\pi}{4} W_{ch}(rbt_i^2). \quad (3)$$

where one-half of the lateral heat spreading has been assumed to be towards the package periphery and the other half towards the package case. The spherical component of heat flow area is then given by the area of the one-eighth spheres at each corner of the chip:

$$Asph_i = \frac{\pi}{4} W_{ch}(rym_i + ryp_i)\cdot(rxm_i + rxp_i) + R (n-1)\frac{\pi}{4} W_{ch}(2\cdot rbt_i)\cdot(rxm_i + rxp_i). \quad (4)$$

These expressions for the cylindrical and spherical components of heat flow area at the i-th node are a modified version of those developed in [2] to be able to characterize the geometry of a power module as presented in Fig. 2.

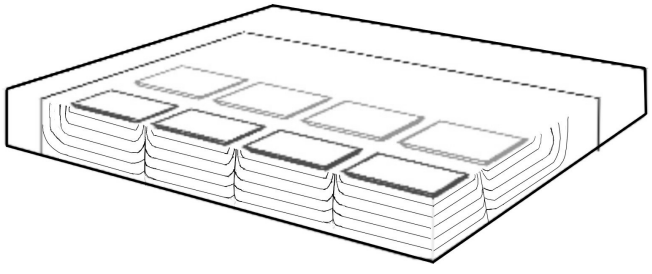

Figure 8. IPEM cross section showing the heat spreading.

The value of the effective heat flow area used to calculate the thermal resistance and capacitance at each node is then

given by $A_{effi} = A_{cyli} + A_{sphi} + A_{chip}$. The value of the effective heat flow area at the package case is also used as a parameter for the heat sink thermal model *area_heat*. Fig. 8 presents the contours formed using the rectangular, spherical, and cylindrical components. The total volume inside these contours became the volume used to calculate the thermal capacitances.

The effective areas for each of the nodes are calculated in the parameter section of the Saber†† model and take into consideration the boundaries of the package. The area changes with depth, also temperature conductivity changes with the materials involved between each pair of nodes. These values are used to calculate the thermal resistance between nodes using:

$$R_{th} = \frac{thick}{K \cdot A}. \quad (5)$$

where R_{th} is the thermal resistance, K is the thermal conductivity, A is the area and *thick* is the thickness of the material. Also the average of the effective area between nodes is used to calculate the volume that store heat between nodes. The thermal capacitance is given by:

$$C_{th} = v \cdot \rho \cdot c. \quad (1)$$

where C_{th} is the thermal capacitance, v is the volume, ρ is the material density and c is the specific heat and implemented in template *module_10.sin*. The template was developed using a hierarchical programming in MAST and the organization of the program is shown in Fig. 9. A representation of the values and equation section of the template is presented in Fig. 10.

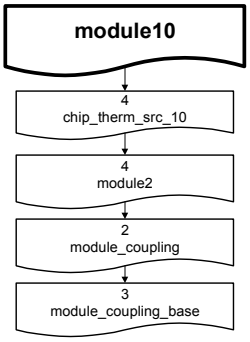

Figure 9. IPEM Template Organization.

C. Heat Sink Thermal Model

The heat sink thermal component model includes a discretized heat equation similar to the chip and package thermal models where the discretization coefficients are determined by the structural and material parameters of the heat sink as well as the value of *area_heat* determined by the package models. The heat sink model describes: (i) the lateral thermal coupling between IPEM over the heat sink, (ii) the semi-cylindrical heat diffusion from the area beneath the package toward the heat sink fins, and (iii) the nonlinear forced and natural convection heat transfer from the heat sink fins to the ambient terminal. The parameters for the heat sink template include the package heat source area for each of the regions of each device, the thickness of the heat sink base, and the location of the package on the heat sink. It also needs the fin area, the fin height, and the air velocity for forced convection.

```
#-------------------------------- Template Header --------------------------------#

                                ###Template Body###

                                ### Parameters###
values  {
          th = tc(header)+math_ctok
          t1 = tc(node1)+math_ctok
          etc…

          h1 = t1*c1
          h2 = t2*c2
          etc…

        }
equations {
          p(header -> node1)+= (th-t1)/rh1
          p(node1  -> node2)+= (t1-t2)/r12
          p(node2  -> node3)+= (t2-t3)/r23
          p(node3  -> node4)+= (t3-t4)/r34
          p(node4  -> node5)+= (t4-t5)/r45
          p(node5  -> case) += (t5-tc)/r5c
          p(case -> nodep)  += (tc-tp)/rp

          p(node1)+= d_by_dt(h1)
          p(node2)+= d_by_dt(h2)
          p(node3)+= d_by_dt(h3)
          p(node4)+= d_by_dt(h4)
          p(node5)+= d_by_dt(h5)
          p(nodep)+= d_by_dt(hp)

           }}
```

Figure 10. Values and Equation sections for discretized form of heat diffusion equation.

In the vicinity of the heat source (location of package), the heat diffuses vertically toward the back of the heat sink body and also spreads laterally, as described for the package models. After the heat has diffused to the back of the heat sink body beneath the heat source, the heat flow continues diffusing vertically and also spreads laterally beyond the location of the heat source. The same happens in each of the four connections of each module. After that, the heat is transferred laterally around the heat sink by thermal resistance between adjacent nodes in the x and y direction.

In accordance with the logarithmic grid spacing principle, three thermal nodes are required to describe the vertical heat flow through the base region. At the heat sink fins, the heat is transferred to the ambient terminal by forced and natural convection. The natural convection thermal resistance is given by [5], where R_{nat} is the thermal resistance due to natural convection, T_f is the fin temperature, T_a is the ambient temperature, h'_{nat} is the natural convection, and A_{fin} is the fin area.

$$h'_{nat} = 4.84 \cdot 10^{-4} \frac{A_{fin}}{P_{fin}^{0.35}}. \quad (7)$$

$$R_{nat} = \frac{1}{h'_{nat} \cdot (T_f - T_a)^{0.35}}. \quad (8)$$

The forced convection thermal resistance is given by [6], where R_{for} is the thermal resistance due by forced convection, h'_{for} is the forced convection and v_{air} is the air velocity.

$$f = \begin{cases} 1.7 + 0.148 \cdot \ln(v_{air}/508) & \text{for } v_{air} \le 508\,cm/s \\ 1.7 + 0.433 \cdot \ln(v_{air}/508) & \text{for } v_{air} \le 508\,cm/s \end{cases}. \quad (9)$$

$$h'_{for} = f \cdot 4.88 \cdot 10^{-4} \frac{A_{fin}}{\sqrt{Z_{fin}}}. \quad (10)$$

$$R_{for} = \frac{1}{h'_{for} \cdot \sqrt{v_{air}}}. \quad (11)$$

Where the fin-to-ambient thermal resistance is the parallel combination of the forced convection thermal resistance, the natural convection thermal resistance, and the shunt chases mounting thermal resistance. Because h'_{nat} and h'_{for} do not depend upon the simulator system variables, they are calculated in the parameters section of the Saber[††] template and can be listed when the templates are loaded. Also, the template for the heat sink *heat_sink.sin* was developed using an hierarchical programming in MAST and the organization of the program is shown in Fig. 11. A section of the *heat_sink.sin* template is developed is shown in Fig. 12.

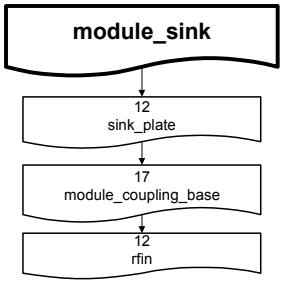

Figure 11. Heat Sink Template Organization.

```
#-------------------------------- Template Header-------------------------------------------
template module_sink module connections ambient = Parameters
thermal_c  module connections

#default model parameters
{
###Template Body ###
# local declarations

sink_plate.module1q1 case1q1 fin1q1                =        Parameters
# SAME FOR EACH NODE

# Coupling between components in each module

module_coupling_base.1 fin1q1 fin1d1               =        Parameters

module_coupling_base.6 fin2d2 fin2q2               =        Parameters

module_coupling_base.8 fin3d1 fin3d2               =        Parameters

# Coupling between components in each module

module_coupling_base.10 fin1q1 fin2q1              =        Parameters
module_coupling_base.14 fin2q1 fin3q1              =        Parameters

rfin.1q1     fin1q1 ambient                        =        Parameters
rfin.1d1
# SAME FOR EACH TERMINAL
}
```

Figure 12. Overview of the heat sink implemented in MAST.

IV. Experimental Work

A. Data Acquisition System

An experimental system to validate the electrothermal models for the IPEM and for the three-phase inverter was built at NIST and reproduced at UPRM to calibrate and validate the developed models. The system consists of a computer-based data acquisition system based on Lab Windows-CVI[†††] from National Instrument with digital multimeters and recorders as shown in Fig. 13. The system acquires temperature at different points in the three-phase inverter and voltages at the module inputs. Communication between instruments and the computer is based on the GPIB protocol. Two programs were developed: one for calibration and one for data acquisition and junction temperature estimation.

The calibration program panel is shown in Fig. 14. This program is used to get calibration curves to relate junction temperature and voltage at the terminals of the device using the temperature-sensitive electrical parameter method TSEP [6]. Pressing "LOOP" initiates the calibration cycle where temperature is changing and voltage is measured until the final temperature is reached. During that time, the measured data is displayed graphically for the diodes and the IGBT. The text boxes in the right of the LOOP bottom are for setting the temperature controller.

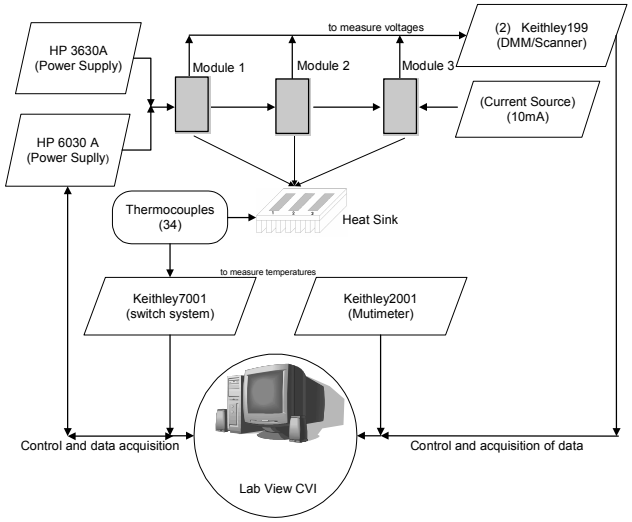

Figure 13. Data Acquisition System.

The transient program panel is shown in Fig. 15. Using this panel, measured thermocouple temperatures and estimated junction temperatures are recorded and displayed during thermal transients. This is the data that will be used to validate and calibrate the model.

B. Model Validation Results

Fig. 2 shows the test circuit built for the model validation experiment indicating the interconnection of the top IGBT of the first module, and the interconnection of the free wheeling diodes of the remaining IGBT in the first module and the other two modules of the inverter. The IGBT is biased to act as a

150 W constant-power source, and the diodes are biased for use as temperature indicators. The diodes are calibrated for their temperature-forward voltage characteristics and the IGBT is calibrated for the temperature-threshold voltage characteristics, using a temperature-controlled heat sink. This enables the semiconductor devices to be used as monitors of the chip temperatures using the TSEP [6]. The experimental data collection commences when power is applied to the IGBT. The temperature of the heat sink and heat sink fins are measured at thirty different points using thermocouples, and all voltage nodes are monitored as the heating progresses.

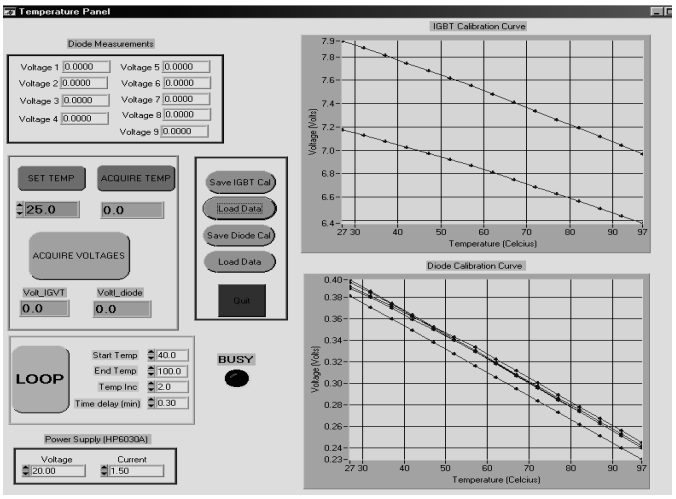

Figure 14. Lab Windows CVI Calibration Panel.

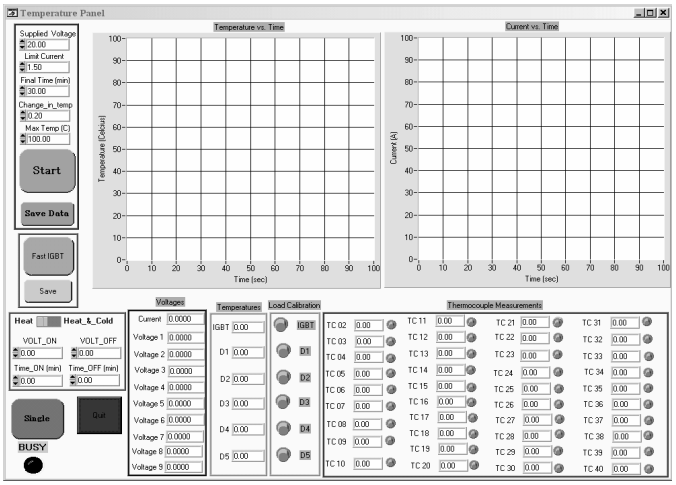

Figure 15. Lab Windows CVI Transient Panel.

Fig. 16 shows a comparison between the experimental and simulated results for the junction temperature of the IGBT and the diodes. The experimental results show good fitting of the junction temperature response of the devices by the model. Fig. 17 shows a comparison between the experimental and simulated results for the temperatures at different positions in the heat sink under the IGBT. The modeled heat sink surface temperature is about 5°C higher than the measured temperature. This is due to the fact that the modeled temperature was on the top of the heat sink next to the baseplate, while the measured heat sink temperature is in a hole drilled slightly below the surface. The fin temperatures are predicted to within approximately 2°C of the measured temperature. These results show good agreement considering that the model represents a local spatial average compared to the single point of the measurements

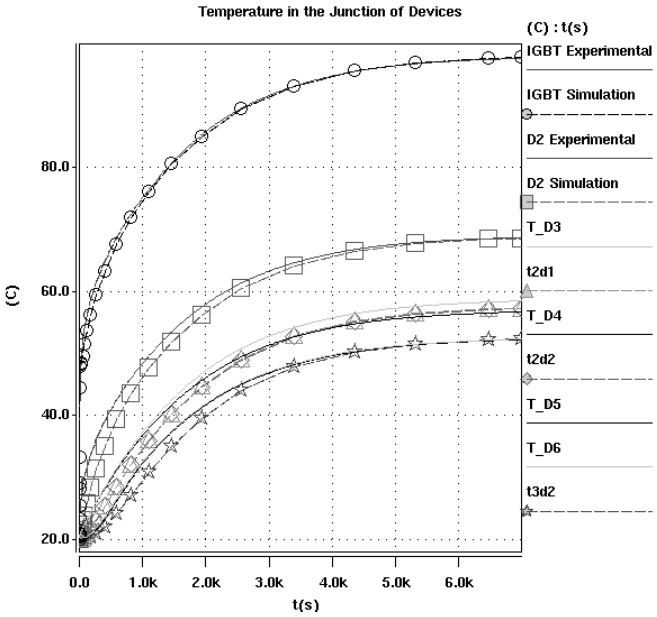

Figure 16. Comparison of temperature at the junction of the devices.

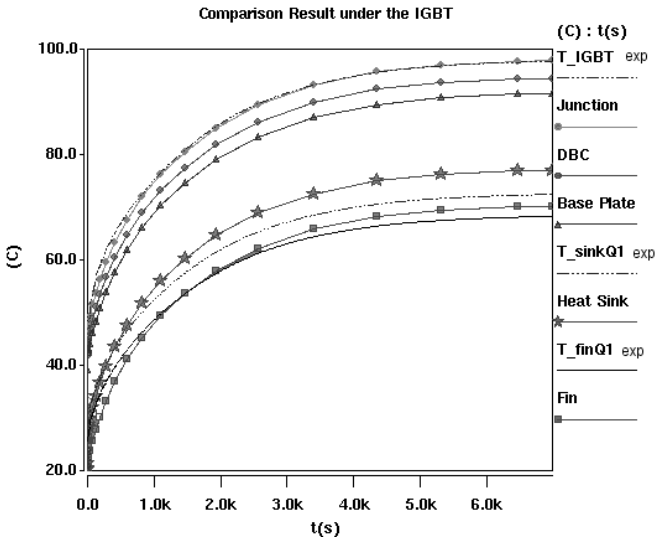

Figure 17. Temperature at different positions under the IGBT.

CONCLUSIONS AND FINAL REMARKS

A reduced-order electro-thermal model of an IPEM and heat sink cooling system is developed and used to develop an electro-thermal model for a three-phase inverter system. The

models are developed from a finite difference discretization of the heat transfer equation using the thermal network component modeling methodology. The resulting models are implemented in Saber†† and allow parametric analysis for the IPEM electro-thermal performance within the inverter. Calibration results show good agreement between experimental data and model output.

We are working on developing experiments to validate the model under different operating modes including switching operation and using multiple IGBTs as heat sources.

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