Thermal-Driven Multilevel Routing for 3-D ICs *

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Abstract

3-D IC has a great potential for improving circuit performance and degree of integration. It is also an attractive platform for system-on-chip or system-in-package solutions. A critical issue in 3-D circuit design is heat dissipation. In this paper we propose an efficient 3-D multilevel routing approach that includes a novel through-the-silicon via (TS-via) planning algorithm. The proposed approach features an adaptive lumped resistive thermal model and a two-step multilevel TS-via planning scheme. Experimental results show that with multilevel TS-via planning, the thermal-driven approach can reduce the maximum temperature to the required temperature with reasonable wirelength increase. Compared to a post processing approach for dummy TS-via insertion, to achieve the same required temperature, our approach uses 80% fewer TS-vias. To our knowledge, this proposed approach is the first thermal-driven 3-D routing algorithm.

I. Introduction

3-D ICs have recently attracted great interest from researchers and IC designers. Studies [1] demonstrate a potential performance improvement of up to 65% by transferring a placement from 2-D to 3-D and eliminating long interconnects. Furthermore, the multiple device layer structure of 3-D ICs provides a platform to integrate different components, such as digital ICs, analog ICs, memory, RF modules, and different technologies such as SOI, SiGe HBTs, GaAs, etc., into one single circuit stack. Thus, it is a more flexible vehicle for system-on-chip (SoC) and system-in-package (SiP) designs compared to planar 2-D IC technologies.

Fig. 1 shows a typical schematic for a 3-D IC. There are mainly three kinds of fabrication technologies to realize circuit designs with multiple Si layers: (1) chip-level 3-D integration, also called 3-D MCM [2][3], under which multiple fabricated chips are packaged into one 3-D multi-chip module; (2) block-level 3-D integration, such as the wafer bonding technology [1]; and (3) cell-level 3-D integration [1, 4]. In this paper we are going to assume the block-level integration technology, under which the basic units are macro blocks with different sizes and aspect ratios.

Although 3-D integration shows promise, significant challenges associated with efficient circuit design and operation have hampered its adoption and further development. The

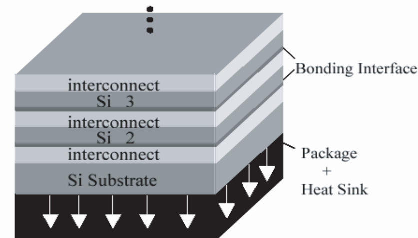

Fig. 1. 3-D IC Scheme

most important issue in 3-D IC is heat dissipation. The thermal problem has already had an impact on the reliability and performance of high-performance 2-D ICs [5][6]. The problem is aggravated in 3-D ICs, principally for two reasons: the devices are more packed, which results in higher power density; and the insulating dielectric layers between the device layers have much lower thermal conductivities than silicon. Also, a 3-D IC physical design problem is usually of higher complexity, with a much enlarged solution space due to the multiple device layer structure. Efficient 3-D physical designs tools, including 3-D routing algorithms, that are specifically designed to take the thermal problem into consideration, are essential to 3-D IC circuit design.

A fast and accurate temperature profiling model is critical to an efficient thermal-driven routing algorithm. The most popular thermal models in circuit design can be divided into three groups: (1) numeric computing methods, such as the finite element (FEM) method [7] and the finite difference (FDM) method [8][9], (2) compact resistive networks [10][11], and (3) simplified closed-form formula models [12][13]. The FEM- and FDM-based methods are the most accurate and time-consuming, and the closed-form formulae are the fastest, but inaccurate.

There are several existing works on 3-D routing. In the early nineties, Enbody and Tan proposed a 3-D channel routing algorithm [14]. Later, Tong and Liu proposed another 3-D channel routing algorithm [15] that decomposes the 3-D routing problem into a set of 2-D routing problems. Das, et al., used a 3-D extension of the hierarchical routing algorithm in their 3-D circuit design flow that treats the 3-D routing as a 2-D routing problem with more routing layers and large obstacles [16]. Minz and Lim proposed a 3-D global area routing algorithm for package-level 3-D IC [17] that assigns the vias one-by-one according to the assignment cost. As far as we know, there is no existing work that considers the thermal problem in routing.

In this paper we propose a multilevel 3-D routing system

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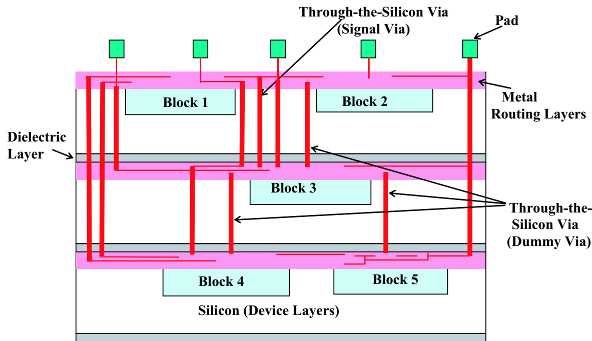

Fig. 2. Cross Section of a 3-D IC Stack

with a novel thermal-driven via planning algorithm. With a more global view and the planning power of a multilevel planning scheme, the via planning step can effectively optimize temperature and wirelength through direct planning of the vias instead of indirect planning through path searching for wires. The rest of the paper is organized as follows. Section II will further discuss the specific thermal problem in routing and formulate the problem that we are aiming to solve. Section III will briefly introduce the resistive thermal model used in our system. Section IV presents the complete 3-D routing algorithm with thermal-driven via planning. We will show the experimental results in Section V and conclude the paper in Section VI.

II. Problem Formulation and New Challenges

A. 3-D Routing Problem

The multiple device layer structure of 3-D ICs not only brings great potential for eliminating long interconnects, but also brings changes to the routing problem formulation. Fig. 2 shows a cross-section of a routed 3-D IC stack. A device layer is covered by several metal routing layers. In this paper we assume that only the top two routing layers are available for inter-block connection. Besides the metal routing layers, interconnect wires can also go through the silicon device layers using vias located at the white space between the macro blocks. Unlike normal routing layers, only vertical vias but no x- or y-direction wires are allowed at the device layers.

The number of routing layers grows as the device layers increase; routing the whole circuit without pruning the search space will be time-consuming. Also, the existence of large obstacles in device layers will cause a long detour of the nets that span multiple device layers and make fast wirelength prediction, such as the half-perimeter metric in 2-D routing, no longer accurate.

B. Through-the-Silicon Via

A via that goes through a device layer is called a *through-the-silicon via*. Through-the-silicon vias are a new kind of physical object in 3-D IC, which are usually fabricated using costly special technologies. Under the current technology, through-the-silicon vias ($pitch \approx 5\mu m \times 5\mu m$) [18] are usually much larger than a regular via ($pitch \leq 0.5\mu m \times 0.5\mu m$), and the routing resource for through-the-silicon via is limited since there will always be big obstacles on device layers.

More importantly, through-the-silicon vias are very effective for heat dissipation and can decrease the maximum temperature over 50% [13]. So through-the-silicon vias are also referred to as *thermal vias*. Further experiments show that the regular metal wires and vias have little effect on the temperature of a circuit due to their neglectable small sizes [19].

The number of through-the-silicon vias in a circuit is determined by circuit connection and placement. Although the through-the-silicon via number can be increased by detouring the routing wires, it is not preferred due to possible wirelength and delay increase. An alternative is to add *dummy through-the-silicon vias* when the *signal through-the-silicon via* number is not sufficient enough to bring down the chip temperature to a satisfactory point. So there are two kinds of through-the-silicon vias in a 3-D circuit: *signal through-the-silicon vias* which are used to connect the signal nets, and *dummy through-the-silicon vias* which exist only for temperature reduction purposes and have no wire connection. However, since the through-the-silicon vias are expensive to fabricate, the total number of through-the-silicon vias in a circuit should be minimized with the temperature as a constraint.

The number and positions of the through-the-silicon vias will determine the final maximum temperature of the circuit and the positions of the signal through-the-silicon vias will affect the final wirelength. One possible approach is to insert dummy through-the-silicon vias after routing. However, since the routing process is not aware of the temperature information, signal through-the-silicon vias are placed to minimize wirelength only, which will probably result in inserting more dummy through-the-silicon vias than necessary. A simultaneous through-the-silicon via planning with routing approach will consider wirelength and temperature at the same time. For conciseness reasons, we are going to refer to "through-the-silicon via" as "TS-via" in the remaining part of the paper.

C. Thermal-Driven 3-D Routing Problem Formulation

The thermal-driven 3-D routing with TS-via planning problem can be described as follows, given the following input:

1. the target 3-D IC technology, including design rule, height and thermal conductivity of each material layer,
2. a 3-D circuit placement or floorplan result with white space reserved between blocks for interlayer interconnects,
3. a given maximum temperature T_0, e.g. 80^oC,

route the circuit according to the connecting rule and design rule, so that the weighted cost of wirelength and the total TS-via number is minimized.

In this paper we assume a wafer bonding technology [1] and TS-vias of size $5\mu m \times 5\mu m$ [18]. A set of floorplan benchmarks is used to demonstrate our approach. However, the proposed routing algorithm can work for all three kinds of technologies if the routing layers and the device layer obstacles are properly modeled in the routing graph.

III. Compact Resistive Thermal Model

A. Basic Thermal Calculation and Assumption

The time constant for on-chip heat conduction is in the range of milliseconds and is several orders of magnitude larger

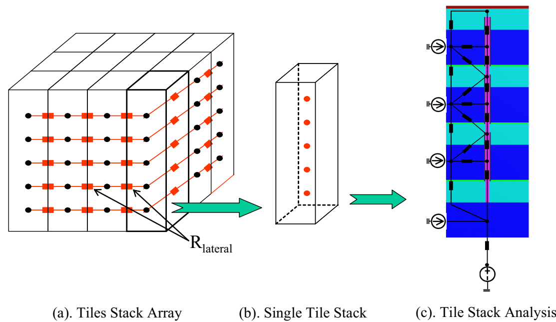

Fig. 3. Resistive Thermal Model for a 3-D IC

than the clock cycles of modern chips. Therefore, only the steady-state status is considered. Also, we only consider the heat generated by transistor switches, since the Joule heating effect of wires is small compared to device heating, and also hard to estimate. We assume all heat sources (blocks) are of constant power density. The steady-state on-chip temperature satisfies the following equation [9],

$$k(x, y, z)\nabla^2 T(x, y, z) + g(x, y, z) \;=\; 0, \qquad (1)$$

subject to the general thermal boundary condition, where $k(x, y, z)$ is the thermal conductivity, $T(x, y, z)$ is the temperature, and $g(x, y, z)$ is the power density. Since a heat sink is usually attached to the substrate, the bottom side of the tile stack in Fig. 1 is isothermal of constant room temperature, 27^oC. The four side walls and top of the chip are treated as ambient, since the chip is usually packaged in thermally insulated materials.

B. Compact Thermal Resistive Model for 3-D IC

Considering both accuracy and runtime, we chose to make use of a compact thermal resistive model proposed by Wilkerson, et al. [11], which explicitly models the thermal effects of the vias. In their thermal resistive model, a tile structure is imposed on the circuit stack with each tile the size of a via pitch, as shown in Fig. 3(a). Each tile stack contains an array of tiles, one tile for each device layer, as shown in Fig. 3(b). A tile either contains one via at the center, or no via at all. A tile stack is modeled as a resistive network, as shown in Fig. 3(c). A voltage source is utilized for the isothermal base, and current sources are present in each silicon layer to represent heat sources. The tile stacks are connected by lateral resistances, $R_{lateral}$. The values of the resistances in the network are determined by a commercial FEM-based thermal simulation tool [20][21]. If there is no via existing in a tile, unnecessary nodes can be deleted to speed up the computing time.

IV. Multilevel routing with Thermal-Driven TS-via Planning

The scalable computation ability and the powerful planning capability of a multilevel routing scheme [22][23] make it a suitable framework for thermal-driven 3-D routing, which faces the challenges of higher complexity and thermal constraint.

A multilevel routing scheme is composed of a recursive coarsening, an initial routing and a recursive refinement process. The scheme features a "V-shaped" work flow, as shown in Fig. 4, which is the typical multilevel optimization scheme. The "downward pass" of recursive coarsening builds up the representations of routing regions and reserves routing resources for local nets, while the "upward pass" of iterative refinement allows a gradual convergence to a globally optimal solution. An in-depth discussion of the method is available in [23].

In order to efficiently handle the new challenges discussed in Section II, we propose a novel thermal-driven routing system for 3-D IC whose multilevel framework is shown in Fig. 4. We introduce several new techniques, including a multilevel thermal-driven TS-via planning and an adaptive lumped resistive thermal model that shares the same underlying tile structure with the multilevel routing scheme. In the remainder of this section, we will introduce the lumped resistive thermal model, give an overview of the multilevel routing system with thermal-driven TS-via planning, then present the detailed TS-via planning algorithm.

A. TS-via Modeling

The thermal-driven TS-via planning starts from the coarsest level and continues at all refinement levels, which correspond to the right half of the "V" cycle in Fig. 4. Routing tiles, which are the uniform-sized constituting cubes of the whole circuit stack, are the basic planning unit for each level. Most thermal activities happen on device layers, where heat sources are located and TS-vias are inserted. So only the nodes corresponding to the device layers are modeled in the thermal profiling process. Temperature differences between routing tiles, rather than within a routing tile, determine the thermal-related cost for planning.

The original thermal resistive model in [11] assumes that each tile is the size of a TS-via pitch. Strictly following such a setting would lead to a huge tile number, which is unrealistic for computation. We coarsen the thermal resistive model so that the thermal model shares the same underlying tile structure with routing. All TS-vias in each tile are lumped together at the center of that tile, as shown in Fig. 5. A thermal model of certain granularity will be generated at each refinement level. The thermal model at the coarsest level has the largest tile size, smallest tile number and lowest accuracy. The thermal model is gradually refined along with refinement of the routing results. In this way, the set of adaptive thermal models provides the accuracy that the planning engine requires without introducing unnecessary computing complexity.

B. Overview of Thermal-Driven Multilevel 3-D Routing

TS-vias are generated by drilling through the silicon device layers, which leads to their large sizes. Also, the TS-vias act as "heat pipes" for power dissipation, while regular vias and wires have little effect on circuit temperature. The size and thermal conductivity disparity between TS-vias and the regular signal wires and vias makes it difficult to handle them together. An individual step of TS-via planning also gives us more control over the temperature of the circuit, since the TS-vias are planned directly instead of being planned through shortest-path searching.

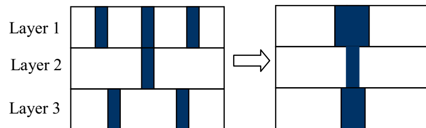

Fig. 5. Lumped Resistive Thermal Model for Multilevel Routing

The multilevel framework has a powerful planning capability. To fully utilize the existing framework, we integrate the TS-via planning and the wire planning into one multilevel planning framework.

The new thermal-driven 3-D routing system, shown in Fig. 4 has a the similar "downward pass" as the scheme in [23], where the routing resources are estimated using a weighted area sum model, and the routing resources for local nets are reserved at each level. Moreover, the thermal-related information, such as the average power density of each tile is also computed during the coarsening process.

During the initial routing stage, an initial 3-D Steiner tree is generated for each multipin net. The Steiner tree heuristic starts from a minimum spanning tree (MST), and a point-to-path maze-searching engine is applied to each edge of the initial MST. Steiner edges are generated when the searching algorithm touches the existing edges of the tree before the target point. Since the maze-searching algorithm can find the shortest path around obstacles, the problem of the existence of many huge obstacles on the device layers can be solved. Then, the number of dummy TS-vias that need to be inserted is estimated through binary search. The upper bound of dummy TS-via numbers that can be inserted into each device layer is estimated by the amount of white space between the blocks. From our experience, the dummy TS-via number can be determined in fewer than ten iterations. After that, a *TS-via number distribution* step is carried out to assign the dummy TS-vias to the tiles.

During each refinement stage, the TS-vias are refined first to minimize wirelength and maximum temperature. The TS-via refinement has two steps, *TS-via number distribution* and *signal TS-via assignment*, which try to optimize temperature and wirelength respectively. After TS-via refinement, the wires are also refined according to the refined TS-vias.

The multilevel routing system communicates with the thermal model throughout the whole planning process. Before TS-via planning, a latest thermal profile will be provided by the thermal model. The thermal model reads in the tile structure and the TS-via number at each tile and returns a temperature map with one temperature value assigned to each tile.

C. TS-Via Planning

Each device layer of the circuit is divided into planning windows PW for TS-via planning. TS-via planning is carried out for each planning window. The problem of TS-via planning then can be described as: given a planning window PW, for TS-vias $\{v_i\}$, $i = 1, \ldots, m$, in PW, and tiles $\{T_j\}$, $j = 1, \ldots, n$, covered by PW, with position $(x_j,\, y_j)$ and capacity c_j, assign each TS-via to one of the tiles, so that the total TS-via number assigned to each tile T_j does not exceed its capacity c_j, and the wirelength and the maximum temperature is minimized.

Our proposed approach optimizes the temperature and the wirelength in two separate steps. In the first step, the number of the TS-vias assigned to each tile is estimated for congestion and temperature minimization. During the second step, a min-cost max-flow formulation is applied for wirelength optimization.

C.1 TS-via number distribution

At this stage, we assign a TS-via number $nv(j)$ to each tile T_j in PW, so that the resulting maximum tile temperature $max(T(j))$ in PW is minimized. The number of TS-vias that we assign to tile j, $nv(j)$ is proportional to $\triangle T(j)$, which is the temperature difference of T_j and the device layer tile immediately below T_j, and is calculated as

$$nv(j) = min(m \cdot \triangle T(j) / \sum_{k:T_k \in PW} \triangle T(k), c_j) \qquad (2)$$

When c_j is smaller than $m \cdot \triangle T(j)/\sum_{k:T_k \in PW} \triangle T(k)$, which means that the empty space of T_j is not sufficient for the planned dummy TS-vias, the rest TS-vias will be inserted into the neighboring tiles with empty spaces.

C.2 Signal TS-via and dummy TS-via assignment

With a TS-via number assigned to each tile, signal TS-vias are first assigned to each tile according to the wirelength cost. The problem can be formulated as a min-cost flow problem, as illustrated in Fig. 6. Let each signal TS-via v_i and tile T_j be a node in graph $G(V, E)$. A source node s and a sink node t are added, with respective supply and demand of m. Each edge will be assigned with a $(capacity, cost_{wl})$ pair, where $cost_{wl}(i, j)$ is the normalized cost of the estimated wirelength after assigning v_i to T_j. There is an edge from S to every TS-via node, with capacity 1 and cost 0; an edge is assigned to every $(v_i,\, T_j)$ pair, with capacity ∞ and cost $cost_{wl}(i, j)$; tile nodes are connected to T by edges of capacity $nv(j)$ and cost 0. Fig. 6 shows the min-cost max-flow problem formulation of assigning six TS-vias, v_1, ..., v_6 to four tiles, T_1, ..., T_4. After the signal TS-vias are assigned to each tile, the remaining number of TS-vias assigned to the tile is then the number of dummy TS-vias that are inserted to that tile.

Since the min-cost flow problem can be solved optimally within polynomial time, the signal TS-via assignment can generate an optimal wirelength solution for one PW. Since all nets passing the same tile are considered at the same time, min-cost flow based TS-via planning approach does not suffer the net ordering problem in net-by-net routing.

A TS-via planning example at level $k-1$ is shown in Fig. 7, where the planning window is chosen as a level k tile. There are three TS-vias a, b and c. a and c are signal TS-vias, which have an estimated connection to other level $k-1$ tiles, while b is a dummy TS-via, which has no connection to wires. The first step of TS-via number distribution assigns one TS-via to each of the three hotter tiles, shown as the dark areas in level $k-1$. In the second step, $cost_{wl}$ will drive c to the higher right corner, and a to the left lower corner.

Such procedures are repeated for all planning windows at all device layers, until all TS-vias are positioned in level $k-1$.

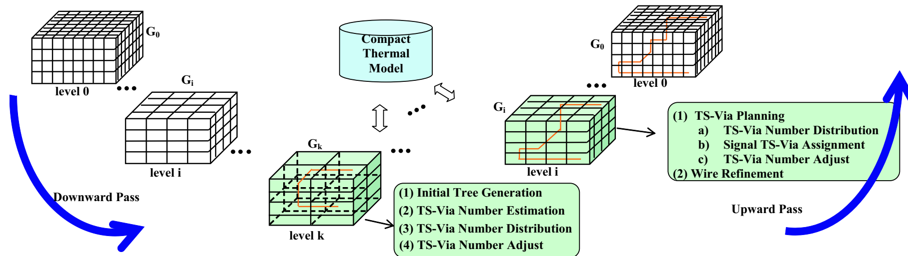

Fig. 4. Thermal-Driven 3-D Multilevel Routing with TS-via Planning

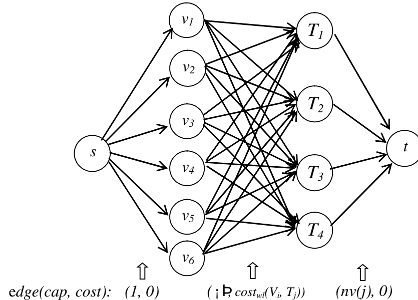

Fig. 6. Transformation to a Min-Cost Max-Flow Problem

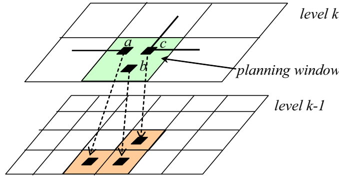

Fig. 7. TS-via Planning

The temperature profile is updated after the planning of one device layer is finished, so that the later planning can be based on a more accurate temperature map. TS-via planning can also be iterated to generate better results. In our implementation, a planning window simply corresponds to one coarse level tile at the refinement level.

Since the dummy TS-via number is estimated by a very simple heuristic, the required temperature may not be achieved after the TS-via planning. Therefore, the TS-via number will be adjusted after TS-via planning. The TS-via number at all tiles will be multiplied by a uniform ratio α. If the current temperature is lower than required temperature, α will be smaller than 1, otherwise, larger than 1. The value of α is determined by binary search. The rationale behind this proportional TS-via number adjustment is that we trust the TS-via planning process, so we hope that the TS-via distribution does not change after the adjustment.

V. Experimental Results

We implemented the thermal-driven 3-D multilevel routing system with TS-via planning using C++, and tested it on Sun Blade 750. The system has been tested on MCNC and GSRC floorplan benchmarks, including two MCNC circuits, ami33 and ami49, and three GSRC circuits, n100, n200 and n300. A 4-device layer configuration is assumed for all circuits. Each block is randomly assigned with a power density value between $10^5(w/m^2)$ and $10^7(w/m^2)$ [9]. The 3-D floorplan layout is generated by a 3-D thermal-driven floorplanning tool [24] with white space reserved between blocks for interlayer connections. Table I shows the total multipin net number and initial temperature of the circuits, which is calculated from the floorplanning result without TS-vias.

TABLE I
3-D Routing Examples

circuits	#nets	init T (^oC)
ami33	133	298.8
ami49	407	210.7
n100	884	275.3
n200	1584	311.2
n300	1892	290.2

We compared our approach of thermal-driven 3-D routing with simultaneous TS-via planning ("$3DR+spr.$") with 3-D routing with a dummy TS-via insertion scheme through a post processing after regular 3-D wirelength-driven routing in Table II. "$3DR+pp.t$" scheme inserts TS-vias according to the temperature of each tile. Both schemes are required to bring the temperature down to 77^oC(350 in absolute temperature). The result of a regular wirelength-driven routing,"$3DR$", is also listed for comparison. The final temperatures are calculated by the compact resistive thermal model at the finest level of the multilevel routing, where each tile contains very few TS-vias. Compared to the post processing of dummy TS-via insertion, our simultaneous TS-via planning can reduce the required dummy TS-via number by 80%. The reason that multilevel TS-via planning is more effective in reducing the temperature is because temperature distribution of different granularity is considered during the multilevel planning process and the hot spots of different sizes can be eliminated through TS-via insertion.

The detailed routing of the 3-D thermal-driven routing system is completed by a grid-based detailed routing algorithm. The final results of the three different routing algorithms, wirelength-driven routing ("$3DR$"), thermal-driven routing with TS-via planning ("$3DR+spr.$") and post processing dummy TS-via insertion after routing ("$3DR+pp.t$"), are also listed in Table II. For the set of the benchmarks that we use, all three schemes can complete all the circuits. "$3DR+spr.$" generates 2% more wirelength because the thermal TS-via positions will restrain the signal TS-via positions. When wirelength is given higher priority than TS-via number, signal TS-vias should be assigned before the TS-via number distribution step. The "$3DR+spr.$" and the "$3DR+pp.t$" will require longer runtime, most of which is due to the extra thermal

TABLE II
COMPARISON OF DIFFERENT TS-VIA INSERTION APPROACHES

	3DR				*3DR + spr.*				*3DR + pp.t*			
circuits	T(^oC)	TS-via #	*wl*	*r.t(s)*	T(^oC)	TS-via #	*wl*	*r.t(s)*	T(^oC)	TS-via #	*wl*	*r.t(s)*
ami33	142.8	227	1.42e5	18.7	79.4	1521	1.41e5	36.5	78.4	2162	1.42e5	37.8
ami49	202.7	185	1.41e6	415.2	77.4	43528	1.43e6	701.6	78.3	138737	1.41e6	758.9
n100	189	1222	2.06e6	138.1	76.8	21564	2.10e6	222.9	78.4	30144	2.06e6	233.4
n200	174.4	2129	3.77e6	239.7	77.2	19724	3.87e6	380.7	77.5	28073	3.77e6	424.2
n300	187.8	2456	6.87e6	394.2	78.1	27215	7.20e6	761.8	76.6	42044	6.87e6	964.2
Avg.			1	1		1	1.02	1.76		1.79	1.00	1.95

profiling. The post processing of dummy TS-via insertion is even slower than the "$3DR + spr.$" because more iterations take place in the finest level, where the thermal profiling is the most expensive.

VI. Conclusions

We propose the first thermal-driven 3-D multilevel routing algorithm which features an integrated adaptive lumped resistive thermal model and a simultaneous multilevel TS-via planning. Experimental results show that our approaches are effective in reducing the dummy TS-vias to bring down the circuit temperature to a required level with similar wirelength and with a reasonable increase in runtime.

There are many interesting topics in thermal-driven 3-D routing. In our current approach, thermal-driven planning is carried out in the refinement stages of the multilevel routing scheme. A thermal need estimation and planning during the coarsening process would probably help to further improve the results. Also, because of the importance of TS-vias in heat dissipation, early thermal planning, such as during 3-D floorplanning or placement, can also improve results in both temperature and wirelength.

VII. Acknowledgement

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