Thermal modelling of Silicon Photonic Ring Modulator with Substrate Undercut

David Coenen[1,2], Herman Oprins[2], Yoojin Ban[2], Filippo Ferraro[2], Marianna Pantouvaki[2], Joris Van Campenhout[2], Ingrid De Wolf[1,2]
[1]Dept. Materials. Eng. KU Leuven, Leuven, Belgium, [2]imec, Kapeldreef 75, Leuven, Belgium
David.Coenen@imec.be

***Abstract*—Ring modulators for silicon photonic (SiPho) optical transceivers are extremely thermally sensitive and require thermal tuning for stable operation. This tuning is achieved with integrated heaters and in this work two aspects of the heaters are investigated: firstly, how to thermally model the heater-waveguide system in a SiPho ring modulator. Secondly, how to improve the energy efficiency by adapting the design in order to minimize the thermal tuning power consumed by the heater. Silicon substrate undercut (UCUT) is done in order to achieve out-of-plane thermal isolation and prevent heat flow directly into the Si substrate below the device. Introducing the UCUT increases the heater efficiency (η_h) with a factor X3.08. It is shown that the influence of the UCUT cross section on the heater efficiency can be neglected, only the total area and metals significantly influence the thermal behaviour. Comparison between electro-thermal and pure thermal simulation shows very similar behaviour. Finally, the UCUT causes an increase in thermal time constant with factor X3.68.**

***Index Terms*—Silicon Photonics, thermal modelling, ring modulator**

I. Introduction

SILICON photonic transceivers require compact and energy efficient electro-optic modulators for the next generation of optical interconnects. Ring modulators (RM) are a popular choice because of their small footprint and low power consumption [1]. One inherent problem with these devices, is that due to their resonant nature, they are very sensitive to variations in operating conditions. Dimensional tolerances from processing are very strict and process variation can cause significant operating errors. Furthermore, due to the large thermo-optic coefficient of silicon ($1.8 \cdot 10^{-4}$ 1/K) [2], the resonant wavelength shift due to temperature variation can be up to 70 pm/K, which can degrade the data transmission transmission quality of the optical link for temperature shifts of only ~ 0.1 K. This is the main motivation for thermally tuning the RM, which is achieved by integrating a metal heater close to the Si waveguide (WG). By monitoring the coupled optical power in the RM, a closed-loop control of the heater current can be achieved in order to lock the resonant wavelength to the wavelength of the communication channel. A mismatch between both wavelengths is compensated by increasing the heater current (red-shift) or decreasing the current (blue-shift) [3]. A significant fraction of total power consumption is required for this thermal tuning, and for this reason an accurate model of the thermal behaviour of a ring modulator is necessary. In addition, such a model allows to optimize the design with respect to thermal performance.

Recently, alternative methods to deal with the temperature sensitivity have been proposed [4], [5]. For example, athermalisation of the waveguide by means of a cladding with negative thermo-optic coefficient which partly compensates the positive coefficient of the waveguide core. However, the limitation here is that the materials used (polymers or TiO_2) are not mature in a CMOS process flow and can be unstable over time. For this reason, heaters are still the most popular solution. A metal heater (typically tungsten [6]) is not the only viable option with respect to heater solutions, e.g. a doped Si heater or even a doped Si waveguide have been studied in literature [7]. The efficiency of the different heater topologies is very similar and the choice typically depends on which type is the easiest to integrate in the process flow. There have been efforts recently to improve the efficiency of the heater by introducing vertical isolation [8] or even lateral isolation by etching air trenches close to the heater [9]. However, full design-space optimisation is lacking [10] and practical guidelines for device designers are not available. For example: How large should the isolation cavity be? How do metal interconnects influence the performance? What should be the metal tiling clearance for optimal performance? These questions are aswered in this paper. In Section II a review of the methodology is shown and the models are validated with experimental data. In Section III the validated models are used to explore factors which influence modelling accuracy. In Section IV possible measures for further heater efficiency optimisation are discussed.

II. Methodology

The ring modulator under investigation (Fig.1) has a diameter of 15 μm and has four electrical I/Os: two RF modulator connects to the bond pads for high speed electro-optical modulation and two heater connects for DC current. Fig.2 shows the typical schematic cross section, highlighting the material stack. The modulator contacts are made of tungsten (W) and are connected to the back-end-of-line (BEOL) interconnect layers with copper (Cu) connects. The metal heater (MHD) generates heat through Joule heating and increases the temperature of the Si waveguide (WG) below. An overview of the different material properties used in the simulations is shown in Table I. Three main cases are investigated in detail: a device without

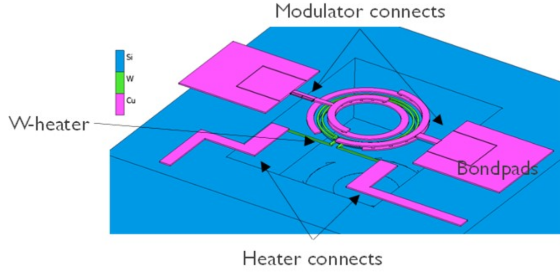

Fig. 1. Ring modulator geometry. Filler material (SiO_2) hidden in order to make device visible. Si (blue), Cu (pink) and W (green)

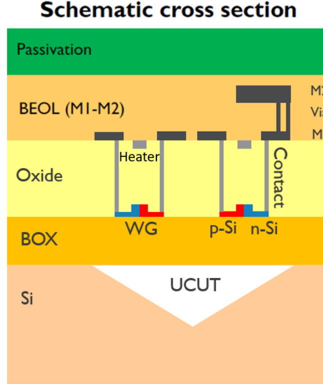

Fig. 2. Device cross section, Si WG (silicon waveguide), BOX (buried oxide) BEOL (back-end-of-line)

substrate undercut (UCUT), with incomplete UCUT and with full UCUT.

A. Simulation setup

A finite element thermal model is made for a single ring modulator, as shown in Fig.1. The software package Msc.Marc [12] is used for modelling and simulation. The depletetion-mode modulator has a pn-junction as waveguide. Silicon thermal conductivity is very insensitive to a change in doping concentration [11], consequently the waveguide can be modelled as an undoped Si rectangle. The domain surrounding the ring modulator included in the model is taken sufficiently large (16 times ring diameter) to account heat spreading and heating of the die in the dynamical analysis. On the top face of the SiPho die a convective heat transfer boundary condition is applied with value 10 W/m^2K, equivalent to natural convection cooling. On the bottom face a convective heat transfer boundary condition is applied with value $10^{11}W/m^2K$, equivalent to an almost isothermal face connected to an ideal heat sink. The side faces of the die are adiabatic. These boundary conditions represent wafer level conditions for probe station testing, allowing comparison of modelling results with experimental data. The mesh size of the model is chosen according to the method of the grid convergence index (GCI) [13]. The model consists of $2.2 \cdot 10^5$ elements, at this size the relative error with the Richardson extrapolation is 2.122%. As this is a sufficiently small error, the mesh resolution is deemed adequate.

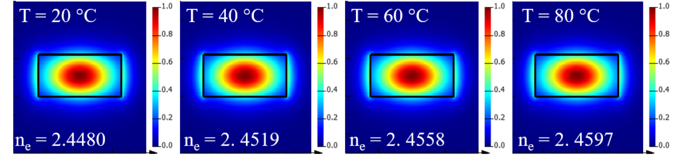

Fig. 3. Optical simulation of Si waveguide in Lumerical Mode solver, intensity of E-field for fundamental mode (TE polarized) and effective refractive index at different temperatures

The objective of the thermal design is to minimize the power consumption of the heater. The heater efficiency η_h, which should be maximized, is calculated as the volumetric average waveguide temperature per unit power applied to the heater, in units of °C/mW. This efficiency η_h can be coupled to the optical characteristic of the ring modulator by converting it to the resonant wavelength shift normalized by heater power $d\lambda/dP$, expressed in pm/mW. This can be done according to Eq.1 [14], [15], [19]:

$$\eta_h = \frac{dT}{dP} = \frac{d\lambda}{dP} \frac{\lambda}{FSR \cdot 2\pi r \cdot \frac{dn_{eff}}{dT}}, \tag{1}$$

where FSR is the free spectral range, λ is the wavelength, r the RM radius and dn_{eff}/dT the thermo-optic coefficient of the effective refractive index for C-band wavelength for this modulator. The latter can be extracted from optical simulation of the fundamental mode propagating through the waveguide (Fig.3). The thermo-optic coefficient at a wavelength of $\lambda = 1.55\ \mu m$ is $1.95 \cdot 10^{-4}\ K^{-1}$ (Fig.4). The FSR can be calculated as follows [20]:

$$FSR = \frac{\lambda^2}{n_g 2\pi r}, \tag{2}$$

where n_g is the group index which takes into account the dispersion in the waveguide and is calculated:

$$n_g = n_{eff} - \lambda \cdot \frac{dn_{eff}}{d\lambda} \tag{3}$$

The dispersion $dn_{eff}/d\lambda = -1.0461\ \mu m^{-1}$ can be calculated by doing a frequency sweep in the C-band range and the simulation result is shown in Fig.4.

All temperatures reported will be normalized with respect to input power, meaning the simulations are carried out for 1 mW of thermal power dissipation in the heater. As discussed above, the normalized waveguide temperature is defined as the heater efficiency η_h. The normalized heater temperature is defined as the heater thermal resistance R_h, both in units of °C/mW.

B. Experimental model validation

The simulation results are compared to experimental measurement data in order to validate the model. In Fig.5 the measured wavelength shift is shown in function of increasing heater power. This is done for three cases: without UCUT, with incomplete UCUT etch and full UCUT. In Fig.5 (B) an incomplete UCUT is shown, which occurs when there still

TABLE I
OVERVIEW OF MATERIAL PROPERTIES USED FOR SIMULATION. REFRACTIVE INDEX AT 1550 NM WAVELENGTH AND 20°C.

	Si	BOX	SiO_2	W	Cu	Passivation
Thermal conductivity $[W/m \cdot K]$	150	1	1	100	400	10
Electrical resistivity $[\Omega \cdot m]$	$2.3 \cdot 10^3$	$1 \cdot 10^{15}$	$1 \cdot 10^{15}$	$5.6 \cdot 10^{-8}$	$1.68 \cdot 10^{-8}$	$1 \cdot 10^{15}$
Density $[kg/m^3]$	2320	2200	2200	10930	8960	2200
Heat capacity $[J/kg \cdot K]$	700	635	635	134	390	2300
Refractive index $[-]$	3.478	1.444	1.444	/	/	/

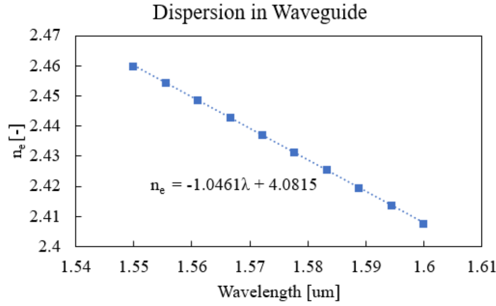

Fig. 4. Optical simulation of Si waveguide in Lumerical Mode solver, effective refractive index in function of wavelength

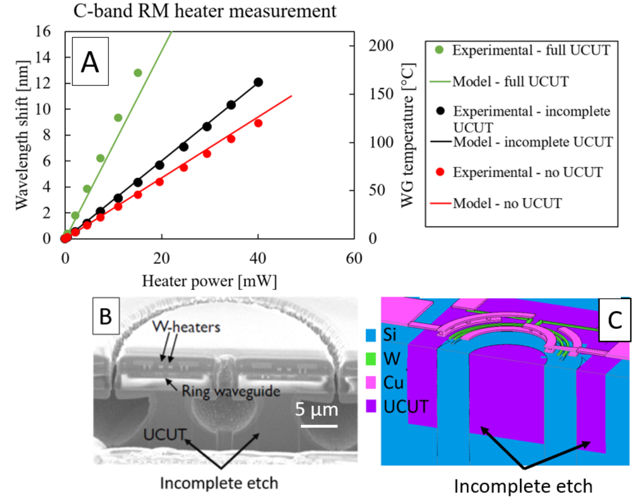

Fig. 5. (A) Measurement results for resonance wavelength shift by increasing heater power, (B) RM cross section with incomplete UCUT and (C) adapted model geometry (cross section) for incomplete UCUT

TABLE II
COMPARISON BETWEEN EXPERIMENTAL MEASUREMENT DATA AND SIMULATION RESULTS OF HEATER EFFICIENCY. STANDARD DEVIATION GIVEN FOR MEASUREMENT DATA WITH AVAILABLE STATISTICS

	Experimental		Simulation	
	pm/mW	°C/mW	°C/mW	error [%]
No UCUT	222±10	2.99±0.14	3.160	5.68
Incomplete UCUT	300	4.04	4.036	0.07
Full UCUT	843±55	11.35±0.74	9.730	14.38

is a fraction of Si below the RM. This produces a heater efficiency expressed in pm/mW, which can be converted to °C/mW with Eq.1. The results are compared with the simulation results in Table II. The case without UCUT shows a relative modelling error of 5.68%. Linear regression in Fig.5 (A) through the experimental data has R^2 value of 0.9991. This signifies that approximation of constant material properties is sufficiently accurate in the chosen temperature range. The incomplete UCUT geometry is modelled in a way that good agreement between simulation and experiment is obtained (0.07% error). The full UCUT shows a relative error of 14.38%. This error is larger compared to the two other cases, and this can be explained by the additional variability introduced in the structure by adding the UCUT. The measured value of 843 pm/mW has a standard deviation of 55 pm/mW over the measured lot, while the standard deviation of the case without UCUT only is 10 pm/mW. The model is now calibrated and in Section IV.A&B a full UCUT etch is further compared with no UCUT and incomplete UCUT.

Transient thermal simulations and measurements are performed with the main purpose of extracting the thermal time constant of the heater and waveguide, which is defined as the time required to reach a temperature change of $1 - 1/e \approx 0.63$ times the steady state temperature change. This assumption holds under the condition that the thermal response can be approximated as a first-order exponential function [16], which is the case. At $t = 0$ s a step function of heater power is applied and the evolution of the temperature is extracted from the model and compared with measurements. The time-dependent measurements on the heater temperature R_h are done by applying a current to the heater and measuring the time evolution of the resistance, which is an indicator of average temperature [17]. The time-dependent waveguide temperature η_h is measured by applying current to the heater and light to the input waveguide, and monitoring the output optical power over time [18]. In Fig.6 the modelled thermal response of the heater (black) and waveguide (red) is shown on a logarithmic time scale. After calibrating the model with experimental data, a time constant τ of 4.92 μs for the heater and 10.38 μs for the waveguide are obtained, for the case without UCUT. The time constants are indicated in Fig.6, along with the corresponding temperature. The calibration is done by adapting the heat capacity of the SiO_2 and BOX layer (see Table I). A full overview of time constants is

TABLE III
OVERVIEW OF NUMERICAL RESULTS OF TRANSIENT SIMULATIONS

	No UCUT	
	Model	Experimental
τ heater [μs]	4.92	5
τ WG [μs]	10.38	10

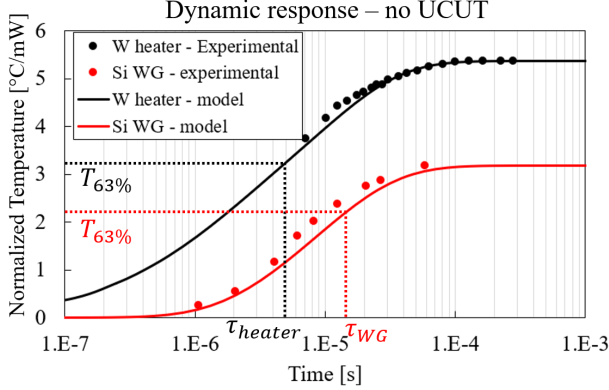

Fig. 6. Transient simulation of dynamic response to a heater power step function at $t = 0s$, heater temperature (R_h, black) and waveguide temperature (η_h, red). Results are for the case without UCUT and calibrated to closely match experimental data.

shown in Table III. It can be concluded that the model is well calibrated with experimental measurements.

III. Analysis of Ring Modulator Model

A. UCUT cross section shape

The UCUT is made by an isotropic wet etch of the Si below the device. The etch shape follows the crystal lattice orientation, resulting in a specific angle which is independent of the cavity size. In Fig.7 two SEM cross sections of the UCUT are shown, the top image shows a typical triangular shape and the bottom image shows a W-shape. This can occur if the etch is incomplete. On the right side, the model implementation of the UCUT geometry is shown. The triangle can be approximated as a rectangular cavity with the same width (dashed lines). It should be noted that the cross sections shown in Fig.7 are of a simplified geometry, with a single heater in the centre. The simulation results are summarized in Fig.8. The temperature distribution for the different UCUT shapes is shown, and the heater efficiency is highlighted. The

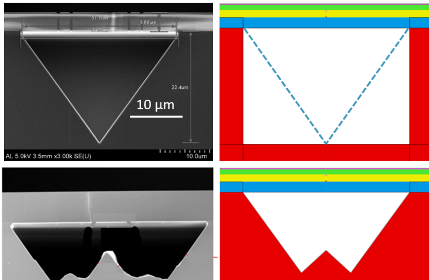

Fig. 7. Different SEM UCUT cross sections, triangular shape can be approximated as rectangle (top) and W-shape after incomplete etch (bottom).

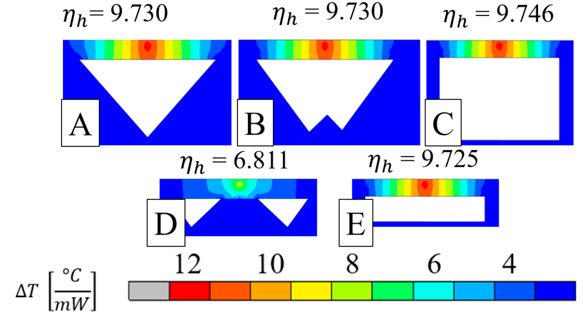

Fig. 8. Simulation result for different UCUT cross sections. Triangular (A), W-shape (B), rectangular (C), W-shape with touching tip (D) and rectangular with decreased height.

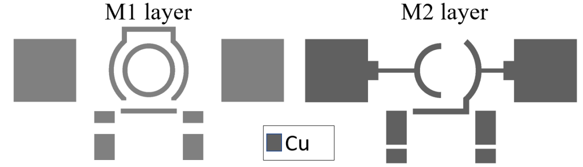

Fig. 9. Layout of metal M1 and M2 layer, including Cu connects and Cu electrodes inside device

results show that within the accuracy of the finite element model all cross section shapes have the same heater efficiency, as long as they have the same UCUT width and as long as no Si touches the suspended oxide membrane right below the heater (Fig.8 D). This simplifies the thermal modelling, as the cavity can be approximated as a rectangular shape. This also means that having an incomplete etch will not affect the thermal performance, as long as some clearance below the oxide membrane is maintained.

B. Significance of metal interconnects

The ring modulator design contains a significant amount of metal interconnects in the BEOL, which potentially influences the thermal performance. This is investigated by including Cu from the M1 and M2 layers in the thermal model. The device layout is shown in Fig.9. On one hand, there are metals located inside the RM, which are required for contacting the electro-optical junctions, and on the other hand there are metals outside the RM required for interconnecting the device for high speed RF signal (bond pads) and DC connections for the heater power supply. The simulations are done for four cases: including and excluding all BEOL metals, each time for the case with UCUT and without. The results are shown in Fig.10, if no metals are included, an overestimation of heater efficiency of 52% is obtained for the case with UCUT, compared with correctly including the BEOL metals in the model. This overestimation is only 18% for the case without UCUT. The first conclusion that can be made based on these observations, is that BEOL metals should be included in device-level thermal simulations for the RM. These metals have a large thermal conductivity and spread the heat which is generated by the integrated heater. This heat spreading is an unwanted effect, but can not be avoided as the device needs electrical I/O. The large thermal impact of the BEOL

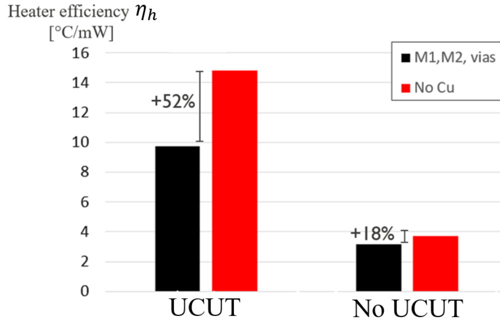

Fig. 10. Simulation result for including Cu in thermal models

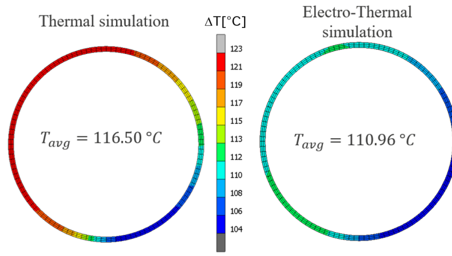

Fig. 11. Waveguide temperature comparison for thermal simulation (left) and electro-thermal simulation (right).

interconnect opens up possibilities for electro-thermal co-optimization. In literature, the inclusion of the metal I/O is most often forgotten [21]–[23]. The second conclusion is that the heat spreading effect is lower for the case without UCUT. The reason for this is that the heat is much less contained close to the device, thus limiting the impact of the metals.

C. Electro-thermal vs. thermal simulation

The simulation results shown in previous sections are obtained by pure thermal simulation. All heat is uniformly generated in the W heater, which is an approximation of the real case where the heat is generated by Joule heating and consequently also in the Cu connects to the heater. In order to investigate how important this effect is and if this needs to be modelled, two cases are simulated. First an electro-thermal simulation is carried out. The total amount of Joule heat generated is used as input in a pure thermal simulation where this power is only dissipated within the heater element itself. The two cases thus dissipate the same value of power, but the spatial distribution is different. The temperature distribution in the waveguide for both cases is shown in Fig.11. The heater efficiency shown up to this point is based on the volumetric average waveguide temperature. However, due to the asymmetric design of the device, the temperature profile along the circumference of the waveguide will not be uniform. The difference between the pure thermal and electro-thermal simulation is small. The cause for this small difference is 2.04% power that is generated in the Cu connects. In conclusion, the pure thermal simulation is sufficiently accurate for the calculation of the heater efficiency.

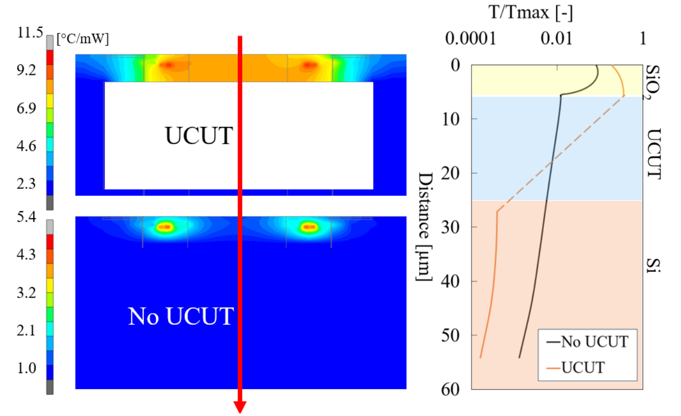

Fig. 12. Cross section of simulation result with UCUT (top) and without (bottom). Note that both contour plots have a different scale. Vertical temperature profile extracted for both cases, normalized with respect to the maximum temperature.

TABLE IV
RESULTS FOR UCUT VS. NO UCUT COMPARISON. HEATER THERMAL RESISTANCE R_h, HEATER EFFICIENCY η_h AND COUPLING η_h/R_h ARE SHOWN.

	UCUT	no UCUT	Increase
R_h [°C/mW]	11.51	5.40	X2.13
η_h [°C/mW]	9.73	3.16	X3.08
η_h [pm/mW]	946	307	X3.08
Coupling [%]	84.5	58.4	X1.47

IV. IMPROVING HEATER EFFICIENCY

The obtained thermal modelling results allow to further explore different measures for increasing the heater efficiency. No drastic changes are introduced in the design and all changes are standard processing compatible.

A. UCUT vs. no UCUT

First the effect of introducing UCUT is investigated. Two different geometries are simulated: with and without UCUT. The UCUT geometry is 27 x 45 μm^2 and removes all Si directly below the RM. The simulation results are summarized in Table IV. The heater efficiency increases with a factor X3.08, which is caused by higher heater temperature and more effective thermal coupling between the heater and waveguide. The physical effect behind this large efficiency gain can be explained with Fig.12. A cross section through the middle of the RM is taken and the temperature is shown for the case with UCUT, and without. With UCUT, the heat is trapped and can not move vertically into the Si substrate: it is forced to spread laterally through the oxide with low thermal conductivity. This adds a significant increase in total thermal resistance. In contrary, the case without UCUT shows much less heat trapping close to the heaters. The main heat path is directly into the Si substrate. In Fig.12 (right) a vertical temperature profile is shown for both simulated cases. The temperature is normalized with respect to the maximum temperature and the temperature drop across the UCUT region is shown with the orange dashed line.

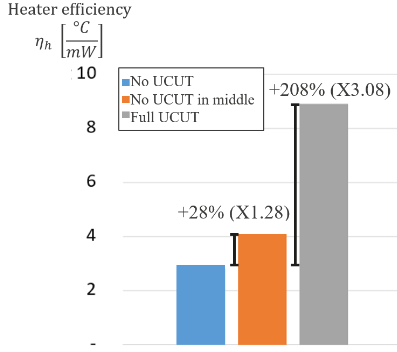

Fig. 13. Heater efficiency without UCUT (blue), incomplete etch (orange) and full UCUT (gray)

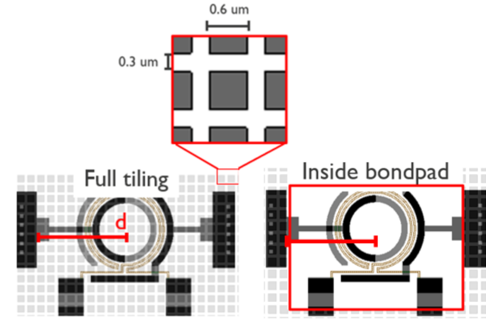

Fig. 14. Tiling no-fill zone expressed as distance from RM center. Detail shows tiles dimensions, actual tiles not to scale in the schematic

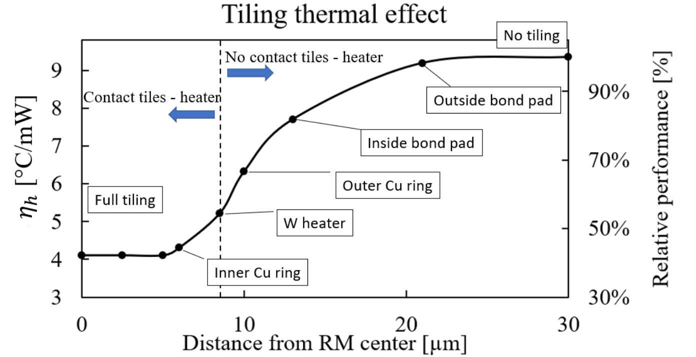

Fig. 15. Heater efficiency η_h in function of tiling no-fill dimension, relative performance is defined using the case without any tiling

B. UCUT geometry

The substrate undercut cavity is made by performing a wet etch of the Si through etch holes in the oxide layers above. If no etch hole is placed centrally in the RM, the Si directly below the device is not removed, resulting in an incomplete etch. A schematic cross section of this concept is shown in Fig.5.C. The incomplete etch has Si in the center of the cross section, while this is not the case for the full UCUT. The effect on the thermal behaviour is now further investigated. In Fig.13 the simulation results are shown. As previously reported, the heater efficiency without UCUT is 3.16 °C/mW, which is increased by 28% (X1.28) by introducing the incomplete etch. If this is expanded to the full UCUT case, an efficiency gain of 208% (X3.08) is obtained. From this can be concluded that an incomplete etch does not fully utilize the potential UCUT efficiency gain. Leaving Si right below will create a highly conductive thermal path into the substrate. This should be avoided by going for the full UCUT geometry.

C. Metal tiling

During processing of SiPho chip, dummy metal tiles are placed in the BEOL layers for structural stability and uniform metal deposition. However, from a thermal point of view this can influence the performance of the heater as the metals have a high thermal conductivity and can spread out the heat. Typical tiling geometry is shown in Fig.14, the tile dimensions are 600 x 600 nm^2 with 300 nm spacing. In some cases it can be acceptable to leave an area open without tiles, which is referred to as a no-fill zone. In order to investigate the thermal impact of such no-fill zone, different geometries are simulated where the size of the no-fill zone is gradually increased. The size of the zone is measured as the distance from the RM center and in Fig.14 two cases are highlighted: full tiling and no-fill zone inside the bond pads. The results are shown in Fig.15. The heater efficiency η_h and relative performance are plotted against the no-fill zone size. The largest no-fill zone size is the limit case where no tiles are placed at all, which is taken as the reference for relative performance. For the other extreme case, where full tiling is placed, a relative performance of 40% is obtained. Here it becomes immediately clear that the metal tiling will have a significant impact on the thermal performance. With a small no-fill zone there is direct contact between the tiles and heater. This causes significant heat spreading in the BEOL layers, which needs to be avoided in order to contain the heat close to the device. In Fig.15 the location of the heater is indicated with a dashed line. Tiling left of this line will cause direct contact between tiles and heater. Tiling to right of the line will have a clearance between both. The largest efficiency gain is obtained as soon as there is no contact between tiles and heater. Increasing the no-fill zone area with factor 4 beyond the inside of the bond pad results in an additional efficiency gain of 21%.

D. Dynamic characterisation

The final aspect discussed in this paper, is the impact on the thermal dynamics by the introduction of the UCUT below the ring modulator. The calibrated model is used to simulate the impact of introducing the UCUT, see Fig.16. The initial response of the heater and waveguide is independent of the UCUT, as the heat does not have sufficient time to reach the bottom of the device. However, after the initial response, the temperature of the device keeps rising and consequently takes a longer time before the steady state temperature is reached. This translates to an increase in thermal time constant of the waveguide from 10.38 μs to 38.1 μs (X3.68) when an UCUT is introduced, while the steady state heater efficiency increases with a factor 3.08. The increased thermal inertia of the RM due to the introduction of UCUT can be beneficial in certain applications, e.g. when a small thermal frequency response of the heater is required in AC-driven applications.

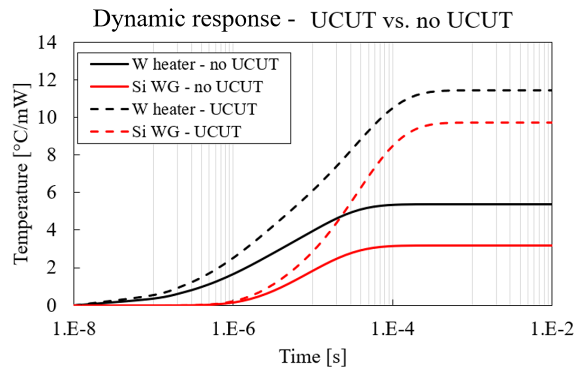

Fig. 16. Comparison of dynamic response for UCUT and no UCUT, τ heater is 18.1 μs and τ waveguide is 38.1 μs with UCUT.

V. Conclusion

Two main research questions are investigated in this paper: (1) How to thermally model a silicon photonic ring modulator and (2) what is the impact of introducing substrate undercut below the ring modulator and can the heater efficiency be improved any further. In the first part it is shown that out-of-plane UCUT geometry is trivial for thermal performance, as long as total UCUT width is kept constant. Secondly, device metals should be included in the model. If they are left out, modelling errors up to 50% can be made. Thirdly, electro-thermal simulation is compared to thermal simulation, which both yield very similar results ($\pm$2.04% relative difference). In the second part it is shown that the removal of all Si below the device can increase the heater efficiency with a factor X3.08 by effective thermal isolation. Furthermore, if the Si etch is incomplete, this factor is only X1.28. The metal tiling in the BEOL layer causes an efficiency penalty up to 60%. It is important to make a tiling no-fill zone above the device, and its size will depend on the trade-off between processing requirements. Lastly, the impact of the UCUT on the device dynamics is investigated, and an increase of thermal time constant of the waveguide from 10.38 μs to 38.1 μs is observed.

Acknowledgment

This work was carried out as part of imec's industry affiliation R&D program "Optical I/O".

References

[1] M. Rakowski et al., "Hybrid 14nm FinFET - Silicon Photonics Technology for Low-Power Tb/s/mm2 Optical I/O," *Symposium on VLSI Technology Digest of Technical Papers*, 2018.
[2] L. Pavesi, D.J. Lockwood, "Silicon Photonics III: Systems and Applications," Springer, 2016.
[3] S. Agarwal, "CMOS Circuitry for the Wavelength Locking of a Ring-based Silicon Photonics Transmitter," Ph.D. Thesis, KU Leuven, 2018.
[4] S. S. Djordjevic et al., "Athermal Silicon Ring Modulators Clad with Titanium Dioxide by RF Magnetron Sputtering," *Optical Interconnects Conference*, 2013.
[5] K. Padmaraju, K. Bergman, "Resolving the thermal challenges for silicon microring resonator devices," *Nanophotonics*, Vol.3, 269-281, 2014.
[6] A. Masood et al., "CMOS-compatible Tungsten Heaters for Silicon Photonic Waveguides," *9th International Conference on Group IV Photonics*, 2012.
[7] A. Masood et al., "Comparison of heater architectures for thermal control of silicon photonic circuits," *10th International Conference on Group IV Photonics*, 2013.
[8] I. Shubin et al., "Integration, processing and performance of low power thermally tunable CMOS-SOI WDM resonators," *Optical and Quantum Electronics*, Vol.38, Apr. 2012, doi: DOI 10.1007/s11082-012-9577-9.
[9] Q. Fang. et al., "Ultralow Power Silicon Photonics Thermo-Optic Switch With Suspended Phase Arms," *IEEE Photonics Technology Letters*, Vol. 23, No. 8, pp. 525-527, Apr. 2011.
[10] A.H. Atabaki, E. Shah Hosseini, A.A. Eftekhar, S. Yegnanarayanan and A. Adibi, "Optimization of metallic microheaters for high-speed reconfigurable silicon photonics," *Optics Express (OSA)*, Vol.18, No.17, Aug. 2010.
[11] M. Asheghi et al., "Thermal conduction in doped single-crystal silicon films," *Journal of Applied Physics*, Vol.91, No.8, 2002.
[12] MSC-Marc, http://www.mscsoftware.com/product/marc
[13] P.J. Roache, Perspective: "A method for Uniform Reporting of Grid Refinement Studies," *Journal of Fluids Engineering*, 1994.
[14] K. Pedmaraju, K. Bergman, "Resolving the thermal challenges for silicon microring resonator devices,"*Nanophotonics*, Vol.3, pp. 269-281, 2014.
[15] J. Teng et al., "Athermal silicon-on-insulator ring resonators by overlaying a polymer cladding on narrowed waveguides," *Opt. Express*, Vol.17, pp.14627-33, 2009.
[16] JEDEC Solid State Technology Association, "Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction to Case of Semiconductor Devices with Heat Flow Trough a Single Path," Standard JESD51-14, 2010.
[17] K. Croes et al., "Understanding EM-degradation mechanisms in metal heaters used for Si Photonics applications," *IEEE International Reliability Physics Symposium (IRPS)*, 2019.
[18] Po Dong et al., " Thermally tunable silicon racetrack resonators with ultralow tuning power," *Optics Express*, Vol.18, No. 19, 2010.
[19] Q. Fang, J. Song, X. Luo, L. Jia, M. Yu, G. Lo, Y. Liu, "High efficiency ring-resonator filter with NiSi heater," *IEEE Photonic Tech. L.*, Vol.24, pp.350-2, 2012.
[20] W. Bogaerts at al., "Silicon microring resonators," *Laser Photonics Rev.6*, No.1, pp. 47-73, 2012.
[21] A.H. Atabaki, E.S. Hosseini, A.A. Eftekhar, S. Yegnanarayanan and A. Adibi, "Optimization of metallic microheaters for high-speed reconfigurable silicon Photonics," *Optics Express*, Vol.18 (17), 2010.
[22] L. Cao et al., "CMOS compatible micro-oven heater for efficient thermal control of silicon photonic devices," *Optics Communications*, Vol.305, P.66-70, 2013.
[23] P. A.K. Yepez et al., "Novel Measures for Thermal Management of Silicon Photonic Optical Phased Arrays," *IEEE Photonics Journal*, Vol.11 (4), 2019.