IOSR Journal of Applied Physics (IOSR-JAP)
e-ISSN: 2278-4861.Volume 9, Issue 3 Ver. I (May. – Jun. 2017), PP 11-13
www.iosrjournals.org

Thermal Noise Analysis of Switched Capacitor Networks

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Abstract: *Thermal noise is one of the most important challenges in analogue intergrated circuits design. This problem is more critical in switched capacitor (Sc) filters due to the aliasing effect of wide band thermal noise. In these circuits, switching introduces a boost in the power spectral density of the thermal noise due to aliasing. Unfortunately, even though the theory of noise in Sc circuits is discussed in the literature, it is very tedious and requires highly sophisticated and not widely available software. The purpose of this paper is twofold. It provides a tutorial description of the physical phenomena taking place in anSc circuit while it processes noise. It also proposes some specialized but highly efficient algorithms for estimating the resulting sampled noise in Sc circuits, which need only simple calculations. A practical design procedure, which follows directly from the estimate, is also described. The accuracy of the proposed estimation algorithms is verified by simulation using spectre RF. As an example, it is applied to the estimation of the total thermal noise in a second order low-distortion delta sigma converter.*

I. Introduction

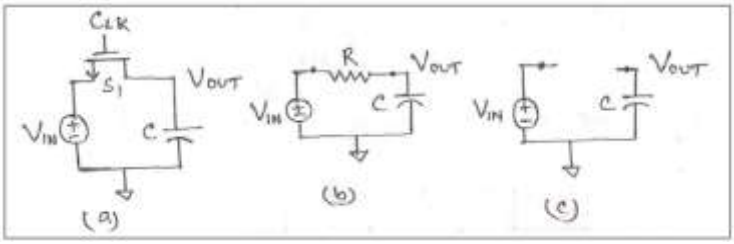
Now a day, sampled data circuits are widely used in integrated mixed singal system. Such functions include switched-capacitor filters, analog to digital converters and so on. The sampling of analog signals was discussed as early as the 1870's when James clark Maxwell developed the fundamental theory of sampled of sampled data circuits the equivalent resistance of a periodic switched capacitor is

$R = \frac{Tc}{KC}$

During the late 1950s and early 1960s, the theory of sampled the data circuits evolved. However, they were not used widely until semiconductor technology was developed so that switches could be embedded into integrated circuits. In particular, Hodges and Gray of Berkely and Brodessen/Copeland found switches can be practically realized with MOSFETS. Sampled data circuits or switched-capaciotor circuits by using MOSFETS as switches have been widely used in analog design.

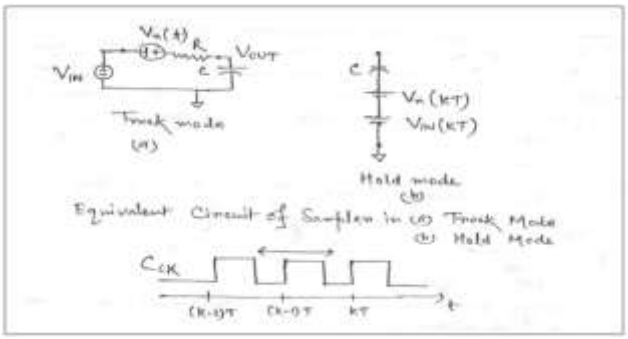
II. Thermal Noise

Thermal noise is one of the issues of Sc circuits and has become the bottleneck of using the Sc circuits to achieve high resolution and high speed. The effect of thermal noise will be reviewed in this section. Take a 1st order Sc circuit as an example as shown in figure. When the switch is turned on in the first phase, it can be modeled as a resistor R as shown in fig(b). This is termed the track mode as sample mode of the sampling circuit. When the CLK is off in phase 2, it can be modeled by an open circuit as shown in Fig(c). Tis is termed the hold mode of the sampling circuit.



Single-transistor sampler (a) transistor implementation of switch (b) track mode (c) hold mode

Consider again the track and hold amplifier in fig, during the track mode, the MOSFET is operating in the triode region and behaves as aresistor,. During the hold mode, it acts as an open circuit. Any resistor, including the MOSFET when acting as a resistor in the track mode, is noisy and the dominant noise is often the thermal noise that is due to the randam movement of electrons in the resistor. This can be modeled as a series noise voltage source as shown in below fig (a). When the switch opens, the capacitor voltage is ideally Vin (KT), where T is the clock period and where it is assumed that the phase of the clock is such that time KT is near the end of the hold interval of the K th clock period. The actual voltage on the capaiator will differ from the ideal value by a noise voltage Vn (KT) due to the thermal noise coming from the switch resistance that was present during the track mode. The clock phasing is shown in below fig.. The noise voltage Vn (KT) is a noise sequence.



Timing Diagram of sampling Clock

The noise power spectral density of a resistor R is equal to

$SR = 4KTR$ …….. ……(i)

The transfer function from input to output is

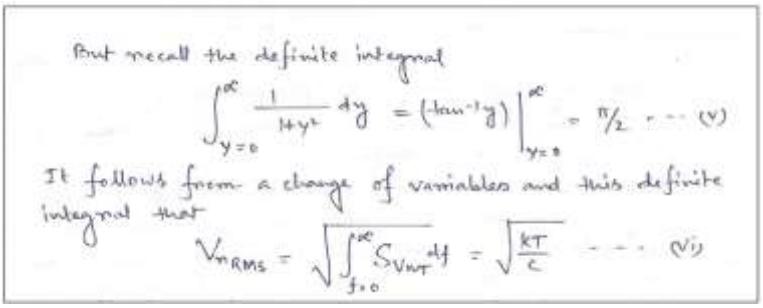
$H(jw) = \frac{1}{1+jwRC}$……..(ii)

The noise voltage on the capacitor during the track mode has noise spectral density

$Sv_{ovt} = 4KTR\left(\frac{1}{1+(RCW)2}\right)$ ……(iii)

Where, $W = 2\pi f$ The RMS noise voltage on the capacitor is given by

$Vr_{RMS} = \sqrt{\int_{f=0}^{\infty} Svovt} = \frac{4KTR}{1+W2R2C2} df$ …… (iv)



This is independent of the size of the resistor R. For switched-capacitor networks, people usually use $\sqrt{KT}/C$ to express the thermal noise voltage contributed by switched capacitors. This equation is valid under the assumption that the bandwaidth of thermal noise is much larger than the clock frequency, in other words, it is an oversampling circuit. The cut off frequency of the thermal noise in most cases exceed sampling rate by orders of maguitude. It will show that the RMS value as the power of the thermal noise calculated from the accurate spectrum analysis has the same order of magnitude of that from KT/C analysis.

Thermal Noise Effects in a Delta Sigma Loop:-

As an example of the use of described noise estimation algorithm, we shall next apply it to the design of a second order low distortion deta-sigma modulater. Its block diagram is shown in Fig1; the H(z) blocks represent Sc integrators using the circuit of Fig 2. The complete circuit is shown in fig-3. We shall assume an oversampling ration OSR=32, a maxium input signal power of 0.25 V_2 (- 6.0 dBV) and a desire 13 – bit performance (i.e, an SNR of 80.0 dB).

To find the minimum acceptable Values of the switched input capacitor Cs1and Cs_2 of the two integrators, and of the input capacitors of the quantizer Q, the following steps need to be performed.

(i) Identify the thermal noise sources (Sc branches, op-amps) in the circuit.
In this circuit, there are five Sc branches (fig 2); one at the input of the first integrator (note that Cs1 is shared between the input and feedback signal paths), one at the input of the second integrator, and three at the input of the quantizer. There are also two op-amps, one in each integrator. The corresponding noise sources are indicate in fig1.

(ii) Find the Voltage and power transfer functions from each noise source to the output.

This may be done numerically, using a dedicated Sc analysis program, or analytically. We shall illustrate the latter method. Using

$H(z) = Z^{-1}/1-Z^{-1}$ …… (a)

The noise voltage transfer function from the input of the first integrator to the output of the modulator is found to be

$NTF_{i1}(z) = \frac{H2+2H}{1+2H+H2} = 2Z^{-1} - Z^{-2}$ ……. (b)

(iii) Add the noise powers due the individual noise sources to obtain the total output thermal noise; equate it to the permissible noise, and use this to find the minimum valus of the Sc.

The minimum value of Cs1 can be obtained directly

$Cs1 \approx 7.24x10^{-2}KT/V^2 = 0.16pF$

The other Sc may be chosen to be much smaller than Cs_1

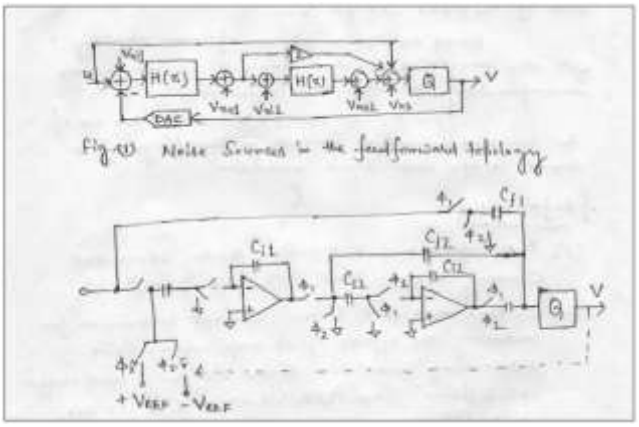


Fig – (2) Schematic of the feed forward topology

In general, a simple optimization can be performed to minimize the total capacitance for a desirable thermal wise level.

III. Conclusion

The effect of thermal noise generated by the switches and op-amp devices in an SC Circuit were analyzed. The analysis was simplified by assuming that the circuit contains only first order blocks (SC branches, feedback op-amps), all designed to settle within half a clock period. This very practical assumption allowed a simple noise estimation process, resulting in a noise model consisting of input and output referred equivalent noise sources. The model was verified by comparing the estimation result for a typical SC integrator with those given by a state of the art CAD program.

Based on the model, an optimum strategy was also suggested for the design of SC integrators incorporating thermal noise considerations. Finally, an example illustrated the use of the proposed estimation process in the design of a second order delta – sigma modulator.

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