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D. DeVoto, P. Paret, M. Mihalic,
and S. Narumanchi
National Renewable Energy Laboratory

A. Bar-Cohen and K. Matin
Defense Advanced Research Projects Agency

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Thermal Performance and Reliability Characterization of Bonded Interface Materials (BIMs)

Douglas DeVoto, Paul Paret, Mark Mihalic, and Sreekant Narumanchi
National Renewable Energy Laboratory
15013 Denver West Parkway
Golden, CO 80401
Email: sreekant.narumanchi@nrel.gov

Avram Bar-Cohen and Kaiser Matin
Defense Advanced Research Projects Agency
675 N. Randolph Street, Arlington, VA 22203

ABSTRACT

Thermal interface materials (TIMs) are an important enabler for low thermal resistance and reliable electronics packaging for a wide array of applications. There is a trend towards bonded interface materials (BIMs) because of their potential for low thermal resistance (<1 mm^2-K/W). However, due to coefficient of thermal expansion mismatches between various layers of a package, thermomechanical stresses are induced in BIMs and the package can be prone to failures and integrity risks. Deteriorated interfaces can result in high thermal resistance in the package and degradation and/or failure of the electronics. The Defense Advanced Research Projects Agency's (DARPA) Thermal Management Technologies (TMT) Program has addressed this challenge, supporting the development of mechanically compliant, low resistivity nano-thermal interface (NTI) materials. Prior development of these materials resulted in samples that met DARPA's initial thermal performance and synthesis metrics. In this present work, we describe the testing procedure and report the results of thermal performance and reliability characterization of an initial sample set of three different NTI-BIMs tested at the National Renewable Energy Laboratory.

KEY WORDS: thermal interface, bonded interface material, accelerated testing, temperature cycling, aging, thermal resistance, transient technique, steady-state technique

NOMENCLATURE

A	metering block cross-sectional area, m^2
BIM	bonded interface material
c_p	specific heat, J/g-K
DARPA	Defense Advanced Research Projects Agency
k	thermal conductivity of metering block, W/m-K
l	thickness of the test sample, cm
NREL	National Renewable Energy Laboratory
NTI	nano-thermal interface
R	thermal resistance, mm^2-K/W
t	time, s
T	temperature, °C
TIM	thermal interface material
TMT	Thermal Management Technologies
x	bondline thickness, mm
Δx_1	distance between T_1 and T_2 or T_3 and T_4, m
Δx_2	distance between T_2 or T_3 and sample interface, m

Greek

a	thermal diffusivity, cm^2/s
λ	thermal conductivity, W/m-K
ρ	bulk density, g/cm^3

Subscripts

avg	average
s top	top of the interface material
s bot	bottom of the interface material
top	top metering block
bot	bottom metering block
1,2,3,4	locations of temperature measurement in the metering blocks

INTRODUCTION

Modern electronic packages continue to increase in processing power by shrinking transistors in each subsequent generation of the silicon devices. With these advances, thermal management of the package becomes more challenging. A successful cooling solution must address the needs of a chip that operates at higher power levels and higher heat fluxes. Hot spots in the chip can result in localized heat fluxes that are several times greater than the chip's average heat flux. Package and die stacking designs will limit access to the back side of chips for cooling, thus creating higher heat density packages. Innovative thermal management solutions are needed to ensure that future chip package architectures can operate at their maximum performance potential.

DARPA's TMT Program aims to address these thermal design concerns through several focus areas: novel air-cooled heat sinks, two-phase heat spreaders, TIMs/BIMs, and thermoelectric coolers. In an electronic package, the TIM/BIM is a critical component that fills up the air gaps between various layers thereby providing a path for heat dissipation. Historically, polymeric interface materials such as greases, gels and phase change materials [1, 2] have been used in various packaging applications. However, the trend towards miniaturization and increasing power densities has resulted in the need for development of low-resistance packaging configurations with TIM/BIM layer resistances on the order of 1 mm^2-K/W or less. An additional and important requirement is also that the TIM/BIM should be reliable. For environmental reasons, non-lead-based solutions are being developed and include lead-free solders [3-7], high-pressure sintered silver [8, 9], low-pressure/temperature sintered silver [10, 11], as well as thermoplastic adhesives [12]. None of these materials though have yielded thermal resistances below 1 mm^2-K/W for large-area attachments (> 50 mm X 50 mm cross-sectional area footprint) while demonstrating reliability under harsh accelerated testing conditions. The goal of the DARPA NTI Program is to develop materials with thermal resistance on the order of 1 mm^2-K/W while demonstrating robustness and reliability. In this work, we report the

characterization of thermal performance and reliability of BIMs synthesized by several performers in DARPA's NTI Program. Standardized test samples were bonded by the performers for accelerated thermal testing. Their initial thermal performance was characterized by the xenon flash transient measurement technique. Xenon flash measurements were taken at periodic intervals during and after the completion of accelerated testing. Rigorous finite element analysis was used to revise a steady-state experimental setup for measuring the thermal resistance of the samples between standardized copper test blocks.

DESCRIPTION OF TEST SAMPLES

A variety of interface materials were evaluated to meet DARPA's thermal and reliability requirements. They include aligned carbon nanotubes, laminated graphite and solder, and copper nanosprings. GE has established an assembly technique that forms metal nanosprings by the glancing angle deposition process [13]. The number of springs, diameter of spring wire, radius of winding, number of windings, and overall spring length can be controlled by the glancing angle deposition process. This allows the process to engineer the desired shear and compressive compliance within the interface while also optimizing for minimal thermal resistance. Teledyne developed a bonding process that vertically aligns graphite platelets within the contact area between two surfaces [14]. The platelets are first aligned and compressed into thin layers before a solder binds the graphite layers to each other and to the surfaces. The Georgia Institute of Technology has led an effort to develop a low temperature process that grows and aligns carbon nanotubes as a thin interface material [15].

The thermal performance and reliability of the performers' interface materials were characterized by utilizing 10-mm X 10-mm cross-sectional footprint samples of silicon bonded to copper via the BIMs, shown in Fig. 1. The silicon diodes used for creating the bonded samples were 350 µm thick and were provided with a backside metallization of aluminum/titanium/nickel/silver. The copper coupons were 1 mm thick and were not provided with any metallization. Surface preparation and additional metallization processing were allowed for the teams to optimize the bond strength with their interface materials. After bonding, bondline thicknesses varied amongst the performers' samples from 70 to 325 µm.

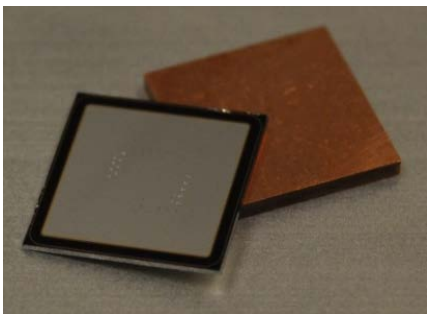

Fig. 1 Silicon and copper coupons

INITIAL THERMAL RESISTANCE MEASUREMENTS

Bonded samples were evaluated for thermal performance using a Netzsch LFA 447 Nanoflash instrument. The Nanoflash operates following the ASTM E-1461-13 test standard [16]. A xenon flash pulse directs energy towards the underside of a test sample. An infrared detector with a 7.8 mm aperture records the sample's top-side rise in temperature as a function of time. This technique is demonstrated in Fig. 2.

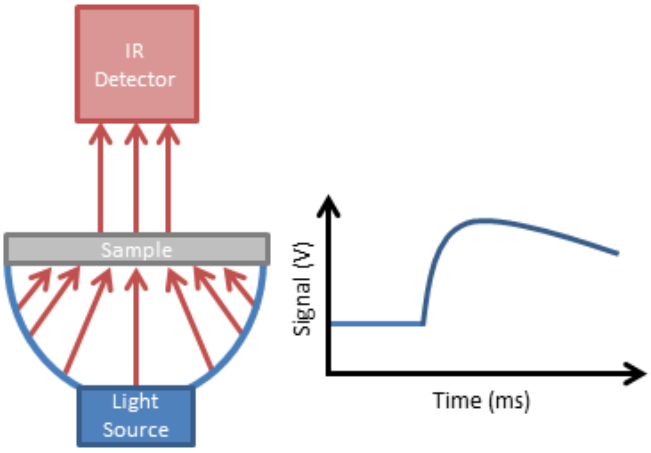

Fig. 2 Xenon flash measurement technique

Under adiabatic conditions, this allows for the thermal diffusivity of the sample to be calculated by the following equation:

$$a = 0.1388 \cdot \frac{l^2}{t_{50}} \quad (1)$$

where:

a = thermal diffusivity
l = thickness of the test sample
t_{50} = the time at which 50% of the temperature rise has occurred

Previous knowledge of a sample's bulk density and specific heat also allows calculation of its thermal conductivity, as shown in the following equation:

$$\lambda(T) = a(T) \cdot \rho(T) \cdot c_p(T) \quad (2)$$

where:

T = temperature
λ = thermal conductivity
ρ = bulk density
c_p = specific heat

With knowledge of the sample's bondline thickness, the thermal resistance of the interface layer can be calculated:

$$R = \frac{x}{\lambda} \quad (3)$$

where:

R = thermal resistance
x = bondline thickness
λ = thermal conductivity

Prior to testing, all samples were sprayed with DGF-123 Dry Graphite Film Spray. This uniform graphite coating allows for consistent absorptivity of the xenon flash pulse and emissivity to the infrared detector between test samples.

Initial thermal resistance measurements are summarized in Table 1. The performers will be designated as Performer A, B, or C for all discussions of results.

Table 1. Initial sample thermal resistance (mm^2-K/W)

Sample Number	Performer A	Performer B	Performer C
1	28.8	3.3	8.4
2	16.7	3.4	3.4
3	13.3	2.7	2.2
4	4.6	2.6	2.1
5	13.4	2.9	1.2
6	9.8	84.1	0.9
7	3.6	19.1	2.4
8	4.3	78.4	1.5
9	4.9	18.6	1.4
10	46.8	21.5	1.2
11	15.6	13.3	1.3
12	4.9	11.9	0.8
13	3.9	3.6	2
14	4.7	4.8	--
15	4.4	3.7	--

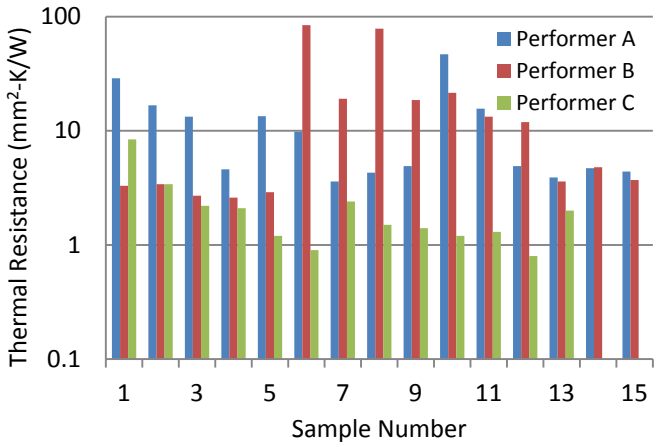

Fig. 3 Initial sample thermal resistance (mm^2-K/W)

Performer A synthesized a sample with a bondline thermal resistance of 3.6 mm^2-K/W, and approximately half of the samples were measured to have thermal resistances lower than 5 mm^2-K/W. However, a significant number of samples were measured with high resistances. This indicates the potential for a low thermal resistance material but also that synthesis variations are present in the production process. Performer B samples followed a similar pattern with one sample measuring 2.6 mm^2-K/W, and half of the samples measuring below 5 mm^2-K/W. Again, the remaining samples yielded high thermal resistances. Performer C produced samples that measured less than 1 mm^2-K/W and was the only team that produced samples with little deviation in thermal resistance measurements.

In addition to transient thermal measurements with the Nanoflash apparatus, acoustic microscopy images were taken of the bondlines for qualitative evaluations of the interfaces.

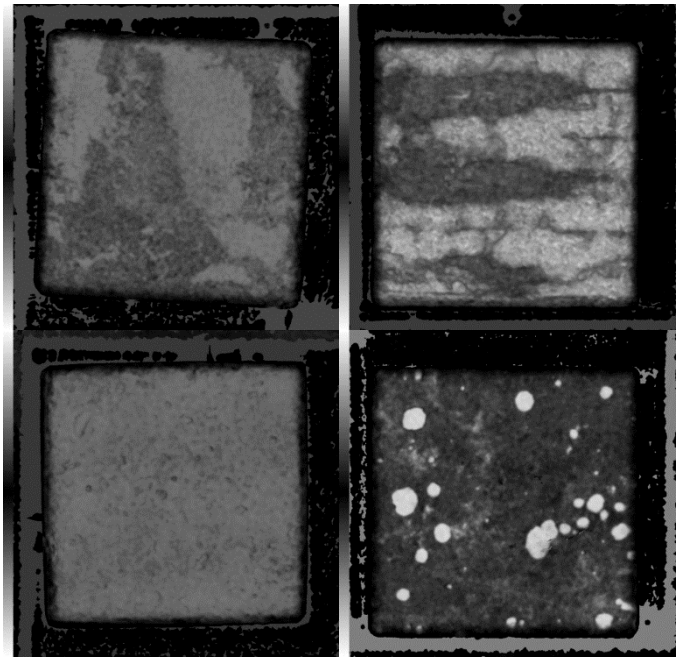

Fig. 4 Acoustic images of samples from Performer A (top left), Performer B (top right), Performer C (bottom left), and lead solder as a reference (bottom right)

In general, darker areas indicate a strong bond between the silicon and copper coupons while lighter areas denote the likely presence of voiding or delamination. Performer A and B samples typically had large areas of discontinuity while Performer C samples consistently showed minimal variation in bond quality (Fig. 4). The presence of lighter, poorer bond areas in samples correlated with higher thermal resistance measurements. For reference, a sample bonded with lead-solder is shown with a high percentage of voiding.

RELIABILITY TESTING AND CHARACTERIZATION

The bonded samples were subjected to accelerated tests in the form of temperature cycling as well as thermal aging at an elevated temperature. In thermal aging tests, the samples were exposed to a temperature of 130°C for 300 hours. In thermal cycling tests, the samples were subjected to temperatures from -40°C to 80°C at low (3°C/minute) and high (25°C/minute) ramp rates. Transient thermal measurements with the Nanoflash apparatus were performed to characterize the thermal performance of all samples prior to, during, and after accelerated testing. Acoustic microscopy was used to monitor the condition of the interfaces during the same analysis intervals.

Samples thermally aged at 130°C were inspected every 100 hours. After 300 hours, Performer A samples all showed an increase in thermal resistance, as shown in Table 2 and Fig. 5. In several cases, the thermal resistance of the bondline within samples approached 100 mm^2-K/W, indicating that a failure of the interface would occur shortly if thermal aging continued.

One sample that initially was measured at 4.6 mm^2-K/W did measure below 10 mm^2-K/W after the aging test concluded.

Table 2. Performer A thermal aging results (mm^2-K/W)

Number of Hours	Performer A Samples			
	1	2	3	4
0	28.8	16.7	13.3	4.6
100	68.3	30.7	27.9	5.1
200	72.2	22	36.6	6.5
300	86.5	24.3	43.3	7

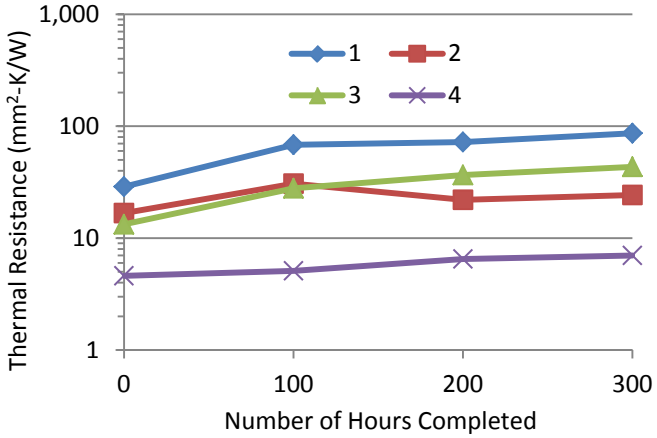

Fig. 5 Performer A thermal aging results (mm^2-K/W)

Performer B samples also showed an increase in thermal resistance, as shown in Table 3 and Fig. 5. This increase was less significant compared to Performer A, and all samples maintained a thermal resistance at or under 6 mm^2-K/W.

Table 3. Performer B thermal aging results (mm^2-K/W)

Number of Hours	Performer B Samples			
	1	2	3	13
0	3.3	3.4	2.7	3.6
100	3.7	4	2.9	3.9
200	5	4.6	3.5	4.4
300	6	3.7	3.9	4.9

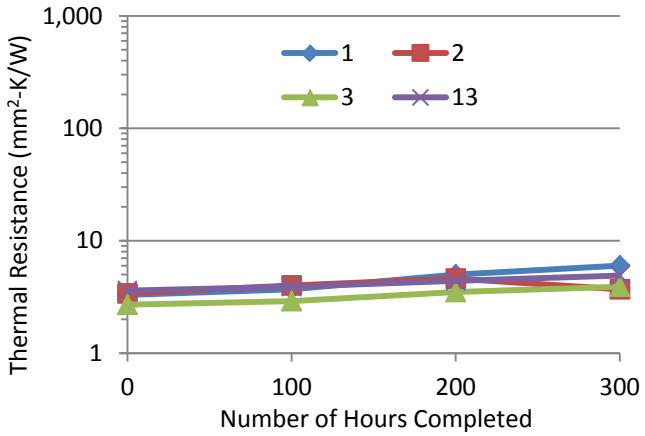

Fig. 6 Performer B thermal aging results (mm^2-K/W)

While all samples from Performer C were initially measured below 10 mm^2-K/W, a significant increase in thermal resistance was measured under aging conditions (Table 4 and Fig. 7). Initial measurements did not prove to be indicators for which samples would show a large increase in thermal resistance. The degradation mechanism was not identified as the acoustic imaging did not reveal a structural change within the bonded interface.

Table 4. Performer C thermal aging results (mm^2-K/W)

Number of Hours	Performer C Samples			
	1	2	3	4
0	8.4	3.4	2.2	2.1
100	8.9	3	14.2	47.8
200	12	4.2	56.9	175.6
300	23	5.5	75	254.8

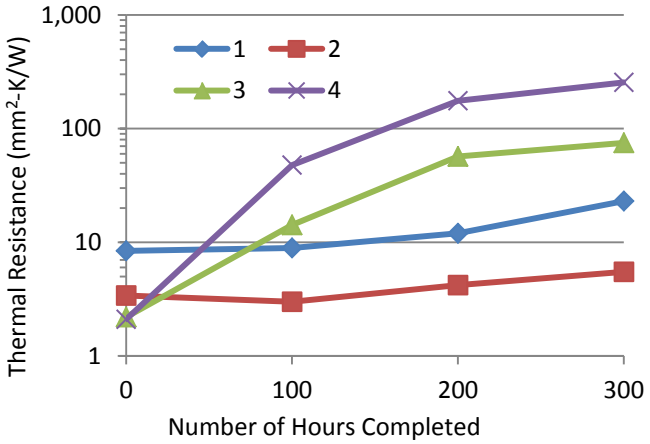

Fig. 7 Performer C thermal aging results (mm^2-K/W)

Under thermal cycling conditions, samples were subjected to temperature extremes from -40°C to 80°C and transitioned between the extremes at a low 3°C/minute ramp rate. Samples were inspected every 10 cycles with transient thermal measurements and acoustic imaging. Performer A samples showed an approximately 50% increase in thermal resistance from samples that were initially measured at 4 mm^2-K/W.

Samples that were initially measured at 10 mm^2-K/W or higher showed a significantly larger increase in thermal resistance. Performer A sample results are summarized in Table 5 and Fig. 8.

Table 5. Performer A thermal cycling (low ramp rate) results (mm^2-K/W)

Number of Cycles	Performer A Samples			
	5	6	8	13
0	13.4	9.8	4.3	3.9
10	20.9	13.1	3.8	4.3
20	23.2	16.3	4.4	4.9
30	31	22.5	5.4	5.5
40	28.4	23.6	5	5.8
50	37.9	29.5	6.1	6.3

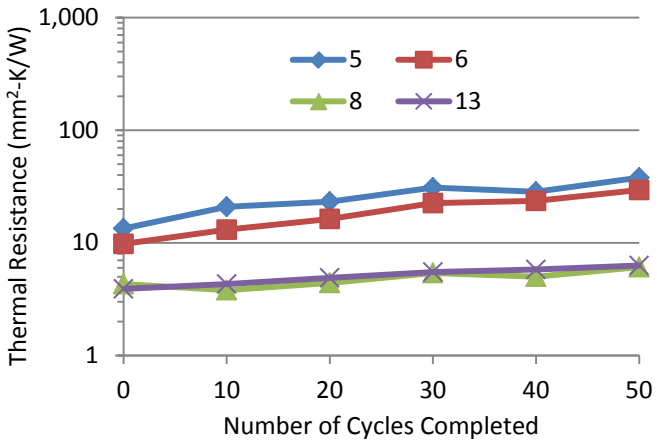

Fig. 8 Performer A thermal cycling (low ramp rate) results (mm^2-K/W)

Performer B samples showed significant degradation from thermal cycling conditions, with one sample's silicon diode completely separating from the copper coupon. Inspection of the delaminated interface that remained on the copper coupon revealed multiple fracture lines within the interface, as shown in Fig. 9.

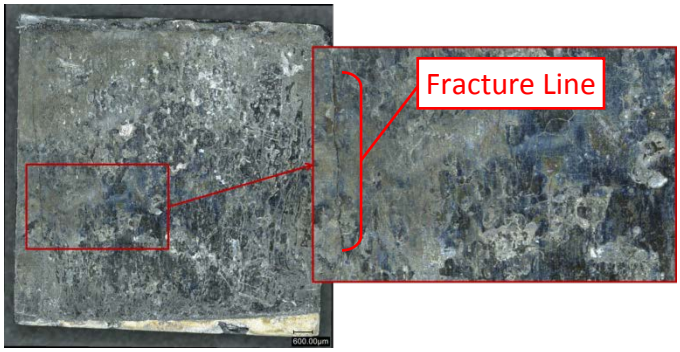

Fig. 9 Performer B sample failure

The thermal resistance measurements for the remaining three samples, presented in Table 6 and Fig. 9, indicated that additional failures via the interface would have occurred if the number of cycles in the test had been extended.

Table 6. Performer B thermal cycling (low ramp rate) results (mm^2-K/W)

Number of Cycles	Performer B Samples			
	5	6	7	8
0	2.9	84.1	19.1	78.4
10	4.9	149.8	23.7	99.7
20	8.8	229.4	87.9	fail
30	28.5	259.8	115.6	fail
40	14.5	279.2	129.7	fail
50	106.7	303.2	146.4	fail

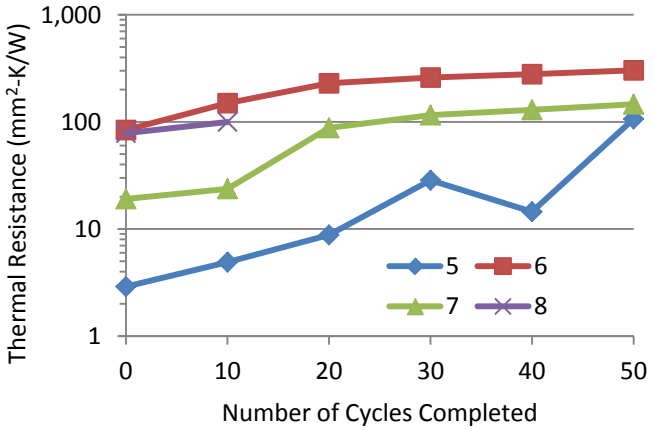

Fig. 10 Performer B thermal cycling (low ramp rate) results (mm^2-K/W)

Performer C samples showed an increase in thermal resistance after thermal cycling; however, all samples were measured at or below 7 mm^2-K/W. Additionally, between approximately 20 and 30 cycles, the rate of increase in thermal resistance tapered off, and measurements held constant for the remainder of the test. If cycling tests had continued, all samples from Performer C would possibly maintain their thermal resistance levels.

Table 7. Performer C thermal cycling (low ramp rate) results (mm^2-K/W)

Number of Cycles	Performer C Samples			
	5	6	7	8
0	1.2	0.9	2.4	1.5
10	1.7	0.9	2.6	1.2
20	2.3	1.6	4.4	2.4
30	4	2.4	8.3	3.5
40	3.1	1.1	6.4	2.7
50	3.7	1.3	7	2.9

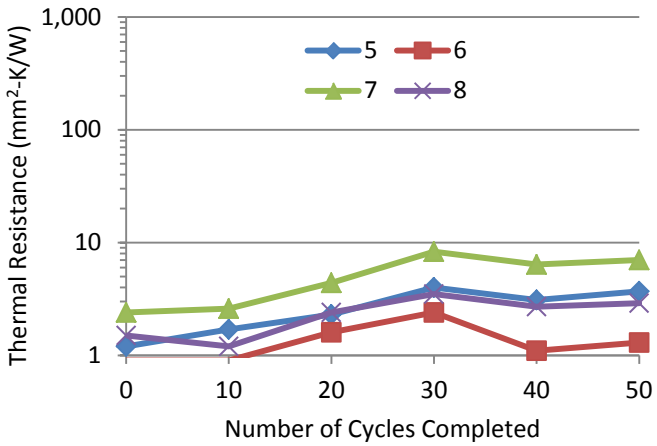

Fig. 11 Performer C thermal cycling (low ramp rate) results (mm^2-K/W).

Samples were subjected to a second accelerated test with temperature extremes again cycling between -40°C to 80°C. Ramp rates were greater than 25°C/minute to impart a more severe thermal shock condition onto the samples. All samples from Performer A showed a significant increase in thermal resistance after thermal cycling under high ramp conditions, as shown in Table 8 and Fig. 12.

Table 8. Performer A thermal cycling (high ramp rate) results (mm^2-K/W)

Number of Cycles	Performer A Samples			
	9	10	11	12
0	4.9	46.8	15.6	4.9
10	6.8	72.3	17.3	5.8
20	13	91	17.9	7.4
30	19.4	80.6	22.1	8.1
40	26.1	73.2	24.9	11.9
50	51	85.9	20.7	17.7

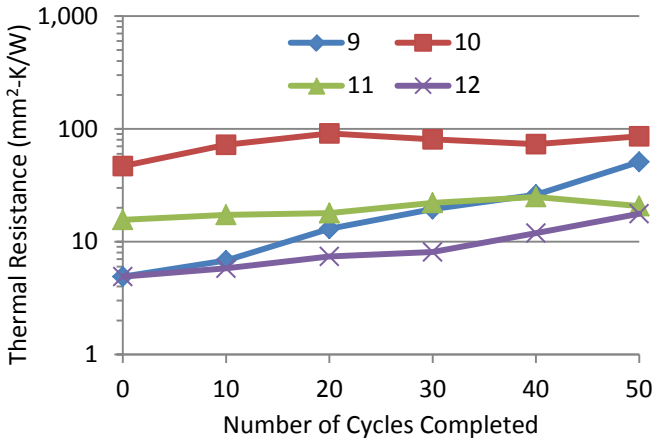

Fig. 12 Performer A thermal cycling (high ramp rate) results (mm^2-K/W)

Performer B samples under high ramp rate conditions reflected similar results to the results for samples under low ramp rate testing (Table 6 and Fig. 9). One sample exhibited a complete failure of the interface while other samples measured significantly increased bondline resistance values, as shown in Table 9 and Fig. 13.

Table 9. Performer B thermal cycling (high ramp rate) results (mm^2-K/W)

Number of Cycles	Performer B Samples			
	9	10	11	12
0	18.6	21.5	13.3	11.9
10	25.2	42.8	33.5	23
20	36.4	63.6	97.2	63.9
30	48.7	80.5	123.9	78.1
40	62.3	87.1	fail	81
50	80.1	110.8	fail	95.3

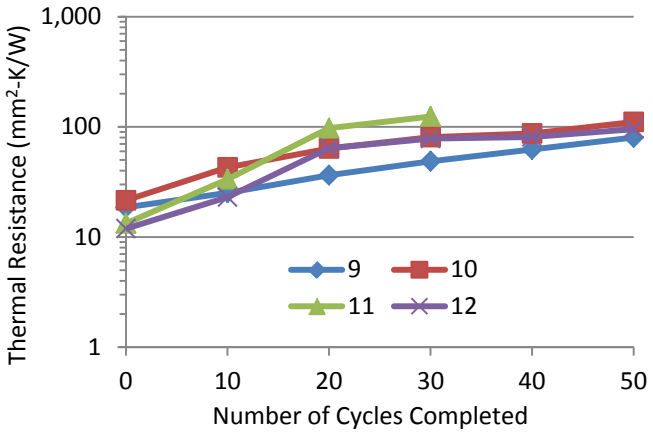

Fig. 13 Performer B thermal cycling (high ramp rate) results (mm^2-K/W)

Apart from one test sample that indicated a defect from the synthesis process, the thermal resistances of Performer C samples stabilized after initial increases under cycling conditions. The three samples that maintained thermal resistances below 4 mm^2-K/W would likely remain intact if the number of testing cycles was extended.

Table 10. Performer C thermal cycling (high ramp rate) results (mm^2-K/W)

Number of Cycles	Performer C Samples			
	9	10	11	13
0	1.4	1.2	1.3	2
10	1.6	1.7	2.5	2.8
20	2.4	2.5	3.4	6.8
30	1.9	1.7	2.8	14.3
40	2.3	1.7	3.7	22.5
50	2.1	1.8	3.7	31.7

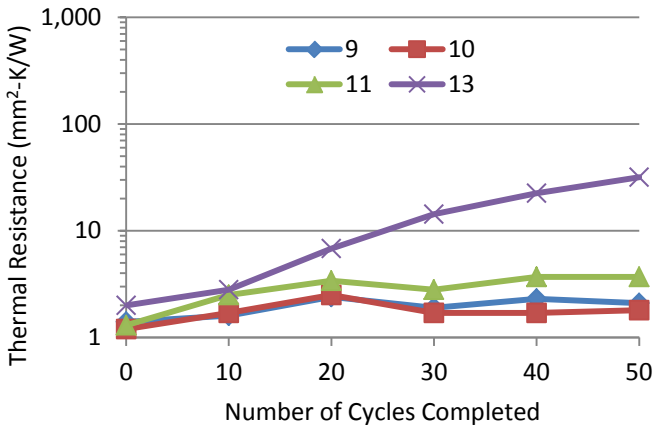

Fig. 14 Performer C thermal cycling (high ramp rate) results (mm^2-K/W)

For some of the samples/results presented above for aging as well as thermal cycling, acoustic images of the interfaces after the accelerated tests revealed voids/defects which correlated with the high thermal resistance measured. This has provided insight into the failure modes as well as their impact on the thermal resistance.

STEADY-STATE THERMAL CHARACTERIZATION

We have previously developed a steady-state thermal resistance tester for characterization of TIMs and BIMs [17] [1]. The operation of the steady-state apparatus follows the method outlined in ASTM D5470-12 [18]. This technique has been employed by other research entities, and results have been documented [19]. The basic configuration of the apparatus is shown in Fig. 15.

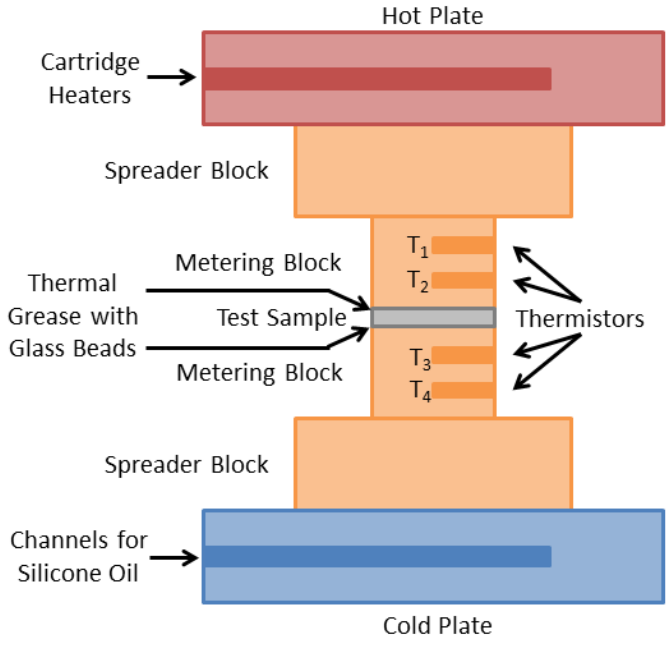

Fig. 15 Steady-state thermal resistance testing apparatus

Heater cartridges are embedded into an aluminum hot plate while silicone oil is circulated through an aluminum cold plate. Four thermistors are embedded in metering blocks which have the test sample between them. In testing of prior materials, thermal grease with glass beads of 25 µm diameter are applied between the metering blocks and test sample to ensure a consistent and known contact thermal resistance. The thicknesses of TIMs or multilayer test coupons are accurately measured before being placed within the apparatus. Due to the adhesive properties of the materials developed by the performers, metering blocks will be provided to them for direct bonding. This will eliminate the need for thermal grease and glass beads.

While the Nanoflash instrument using the transient thermal measurement technique provides measurements of the performers' sample interfaces within an accuracy of ±3%, prior knowledge of the materials' bulk densities and specific heats is a requirement. Additionally, the technique is measuring the resistance of the interface within the test samples where the diffusivity contribution of the silicon and copper coupons must be accounted for to obtain the performance of the bondline. Acoustic imagery has shown that variations of bond quality are present within the bonded interfaces. While the Nanoflash instrument only measures the thermal performance of interface within the central region of a test sample, the steady-state approach will average any quality variations by measuring the entire bonded interface. By allowing the performers to directly bond the metering blocks together with their interface material, a clean story on the bondline resistance can be obtained with only the bondline thickness needing to be measured.

The top and bottom heat fluxes through the metering blocks are first calculated through the following two equations:

$$Q_{top} = k \cdot A\,(T_1 - T_2)/\Delta x_1 \quad (4)$$

$$Q_{bot} = k \cdot A\,(T_3 - T_4)/\Delta x_1 \quad (5)$$

where:

Q_{top} = top metering block heat flux calculation in W
Q_{bot} = bottom metering block heat flux calculation in W
k = thermal conductivity of metering block
A = metering block cross-sectional area
$T_{1,2,3,4}$ = thermistor temperature measurements from hot plate side (1) to cold plate side (4)
Δx_1 = distance between T_1 and T_2 or T_3 and T_4

The average heat flux is determined from the top-side and bottom-side metering blocks by:

$$Q_{avg} = (Q_{top} + Q_{bot})/2 \quad (6)$$

The temperature at the interface between the top metering block and the top-side of the interface material is determined by:

$$T_{s\,top} = T_2 - \Delta x_2 \cdot ((T_1 - T_2)/\Delta x_1) \quad (7)$$

where:

$T_{s\,top}$ = calculated temperature of the test sample's top surface
Δx_2 = distance between T_2 or T_3 and sample interface

The temperature of the interface between the bottom metering block and the bottom-side of the interface material is

calculated in a similar manner:

$$T_{s\,bot} = T_3 + \Delta x_2 \cdot ((T_3 - T_4)/\Delta x_1) \quad (8)$$

The bulk and contact thermal resistance is calculated by:

$$R = \left((T_{s\,top} - T_{s\,bot}) \cdot A\right)/Q_{avg} \quad (9)$$

A finite element analysis was performed to optimize the metering block geometry for an approximately 1 cm^2 interface sample bond area and a 1 mm^2-K/W thermal resistance. The meshed model of the finalized geometry is shown in Fig. 16.

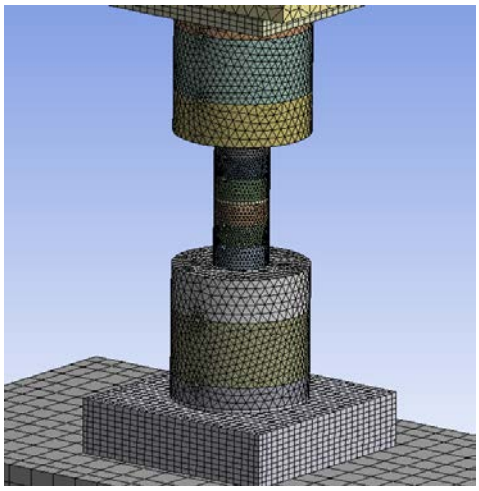

Fig. 16 Finite element analysis model of the testing apparatus

90 W of heat were transferred into the hot plate by the cartridge heaters while an 800 W/m^2-K film coefficient at 30°C was applied to the cold plate's internal tube surfaces. Appropriate convection coefficients and radiation emissivity values were applied to all exposed surfaces. The cross-sectional planes at which the four thermistors were embedded into the metering blocks were analyzed for temperature uniformity. It was found that temperature variations within the planes were approximately 0.13-0.16°C. This measurement uncertainty, along with thermistor calibration error, machine tolerances of the metering blocks, and deviation between the top and bottom meter block heat flux calculations due to radiation and convection losses, all contributed to measurement errors of the steady-state measurement method. These error sources and their tolerances are summarized in Table 11.

Table 11. Error sources and their tolerances

Error Source	Tolerance
ANSYS in plane temperature variation	±0.07-0.17°C
Thermistor, Inc. QT06005A thermistor calibration error	±0.03°C
Meter block diameter	±0.027*10^{-5}mm
Distance between T1 and T2 or T3 and T4	±0.027*10^{-5}mm
Distance between T2 or T3 and interface	±0.027*10^{-5}mm
Averaged heat flux error due to radiation and convection losses	±0.24-0.68W

These error sources were propagated through the steady-state measurement calculations and it was determined that the measurement uncertainty for one experimental test was approximately ±0.35 mm^2-K/W at 95% confidence intervals. A testing apparatus with the optimized metering block geometry was constructed for experimental testing of the performers' interface materials. This apparatus is shown in Fig. 17.

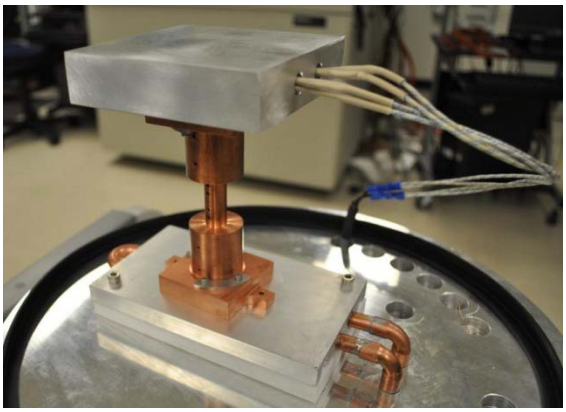

Fig. 17 Constructed steady-state testing apparatus

The four holes in the necked-down region are the locations for the thermistors to be inserted. The complete test apparatus can be sealed under a vacuum bell jar for elimination of convective losses on the metering block surfaces. Experiments were conducted with a joined metering block where both the top-side and bottom-side metering block halves were machined together as one piece. The heater cartridges imparted 60 W into the hot plate, and silicone oil at 50°C flowed through the cold plate. A plot of the thermistor readings from these experiments is shown in Fig. 18.

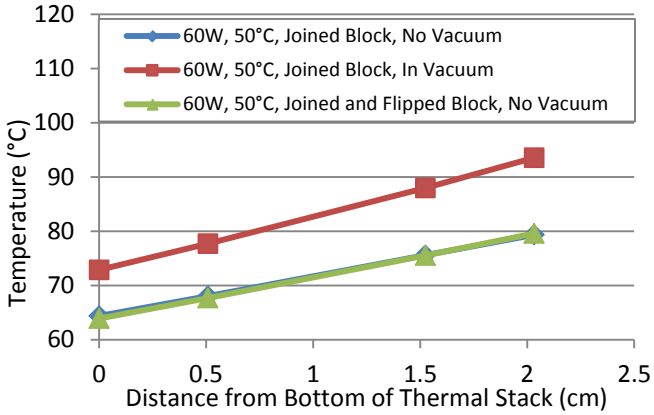

Fig. 18 Steady-state joined metering block measurements

The higher temperature measurements from the test conducted in a vacuum aided in the quantification of the convective heat losses. In all cases, the temperature drop across the four thermistor measurements followed a linear trend. Varying the application of vacuum as well as the orientation of the metering block (flipped block configuration) yielded measurement results to be within ±0.38 mm^2-K/W of the expected result (i.e. zero resistance). The results are summarized in Table 12.

Table 12. Steady-state joined metering block calculations

Experimental Iteration	Average Heat Flux (W)	ΔT Across TIM (°C)	Thermal Resistance (mm^2-K/W)
No Vacuum	36.18	0.11	0.38
In Vacuum	50.68	-0.12	-0.29
No Vacuum, Flipped Metering Block	38.26	-0.01	-0.03

After metering blocks are bonded together by the performers, steady-state tests will be completed.

CONCLUSIONS

The samples from Performer C showed very good thermal performance in the range of 1 to 3 mm^2-K/W, even after being subjected to 50 temperature cycles under low and high ramp rate conditions. The bonded samples from the other performers showed significant degradation after accelerated testing, even though a number of samples initially yielded thermal resistances less than 10 mm^2-K/W. Prior to accelerated testing, many of the samples from the performers met DARPA's initial thermal performance metrics. Based on the lessons learned from the first round of testing, revised 10-mm X 10-mm bonded samples were provided by the performers with altered processing/synthesis conditions. These samples are currently being characterized at the National Renewable Energy Laboratory. In addition, 12.5-mm diameter copper blocks will also be sent to one performer (and potentially other performers) for synthesizing the bonded interface between two copper blocks. Rigorous ASTM steady-state thermal resistance experiments will be performed at the National Renewable Energy Laboratory on these bonded copper blocks to confirm the thermal performance.

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