

# Thermal Stress Induced Delamination of Through Silicon Vias in 3-D Interconnects

Kuan H. Lu, Suk-Kyu Ryu\*, Qiu Zhao, Xuefeng Zhang, Jay Im, Rui Huang\*, and Paul S. Ho  
Microelectronics Research Center, University of Texas at Austin, Austin, TX 78758

\*Department of Aerospace Engineering and Engineering Mechanics, University of Texas at Austin, Austin, Texas 78712  
garylu@mail.utexas.edu

## Abstract

In this paper we investigated the interfacial delamination of through silicon via (TSV) structures under thermal cycling or processing. First finite element analysis (FEA) was used to evaluate the thermal stresses and the driving force of TSV delamination. Then, the modeling results were validated by analytical solutions of the crack driving force deduced for a long crack at the steady state. Both results were found to be in good agreement at the steady state and together they suggested a fracture mechanism to account for the TSV delamination observed. The analytical solution further provided a basic framework for studying the impact of materials, process and structural design on reliability of the TSV structure. In particular, we found that reducing the TSV diameter yields a definite advantage in lowering the crack driving force. In addition, annular TSVs and an overlaying metal pad on a TSV can reduce the crack driving force for delamination during thermal cycling. Finally, the metallization effect was investigated for four TSV materials: copper, aluminum, nickel, and tungsten. Tungsten was found to have the smallest crack driving force due to the least thermal mismatch with the surrounding silicon. The reliability implication was discussed.

## Introduction

The incorporation of TSVs poses a significant challenge to thermo-mechanical reliability of the 3-D interconnects. In particular, the mismatch in coefficients of thermal expansion (CTEs) between the conducting metal in TSV and the silicon matrix can generate thermal stresses inside and around TSVs [1-3]. Such stresses can be sufficient to degrade the performance of stress-sensitive devices [4], to induce cohesive cracking in the silicon [3], and to drive interfacial delamination between the TSV and the silicon matrix [5]. In fact, thermal stress-induced TSV delamination has been found to be one of the dominant failure modes for 3-D interconnects. During fabrication of 3-D interconnects, TSVs can “pop-up” from the silicon wafer and damage the Back-End-Of-Line (BEOL) structures. Finite element analysis (FEA) has been applied to simulate the driving force of TSV delamination [5]. In general, the crack driving force was found to increase with the diameter of TSVs and the circumferential crack length.

In this paper, the driving force and the delamination mechanism for TSV structures were further investigated. The paper is organized in three parts. First, for better understanding of the underlying mechanism, the energy release rate (ERR) that drives the TSV delamination was evaluated using analytical solutions deduced for simplified TSV structures. The results were supplemented and compared with finite element calculations. This was followed by a study on the impact of materials, process and structural design on the reliability of the TSV structure. The effect of TSV

geometry was first studied for three types of TSV structures: (a) full copper filling, (b) annular copper filling, and (c) full copper filling with an annular polymer liner between the copper and the silicon matrix. Here a previous study on thermal stress behavior [3] was extended to calculate the driving force for interfacial delamination. In addition, we investigated the effect of depositing a metal pad on top of the TSV on interfacial delamination. Finally, in the last part, the metallization effect was examined for four TSV materials: copper, aluminum, nickel, and tungsten. The implication on the thermo-mechanical reliability of TSVs will be discussed.

## Crack Driving Force for TSV Delamination: Steady-state Solutions

Thermal stresses can develop around TSVs during fabrication arising from the thermal expansion mismatch between constituent materials. Figure 1 shows the thermal stress from FEA simulations, consisting of both shear and normal stresses. Consider first the effect from the shear stresses. The FEA results reveal a shear stress concentration around the TSV boundary near the wafer surface where the shear stresses have opposite signs depending on whether a heating or a cooling thermal load. The different signs of the shear stress will drive the copper TSV to “pop up” or to cave in from the wafer surface. In both cases, the stress drives a shear-induced delamination along the TSV/silicon interface with the same magnitude of ERR. In contrast, the different signs of the normal stresses induce distinct effects on interfacial delamination. Only the tensile normal stress under a negative thermal load can drive the TSV delamination while the compressive stress under a positive thermal load will not contribute to the TSV delamination. The stress combination will result in delamination under a positive thermal load driven mainly by the shear stress near the wafer surface, i.e. a Mode II fracture. On the other hand, the delamination under a negative thermal load is driven by both the shear stress and the radial tensile stress, i.e. a mix-mode fracture, and the driving force is generally higher. The difference between two opposite thermal loads is further illustrated in Figure 2.

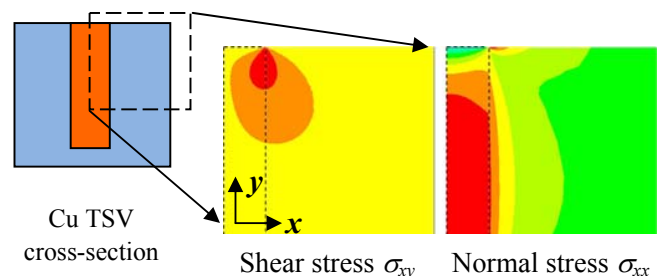


Figure 1. Thermal stress distribution around the TSV boundary near the wafer surface.

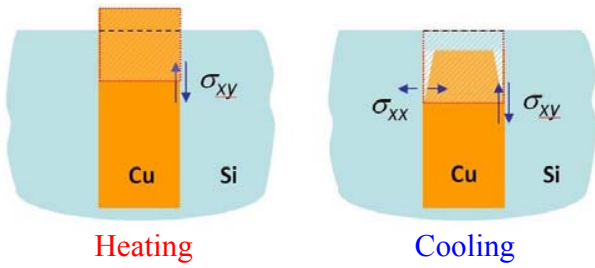


Figure 2. TSV delamination under opposite thermal loads.

The analytical solutions for steady-state TSV delamination have been derived for both the cooling and heating conditions [6]. Consider an isolated, infinitely long TSV embedded in an infinite matrix with a circumferential crack propagating along the axial direction under a thermal load. The steady-state ERR,  $G_{ss}$ , can be expressed as follows:

$$\text{Cooling: } G_{ss} = \frac{E(\Delta\alpha\Delta T)^2 D_f}{4(1-\nu)} \quad (1)$$

$$\text{Heating: } G_{ss} = \frac{E(\Delta\alpha\Delta T)^2 D_f(1+\nu)}{8(1-\nu)} \quad (2)$$

where  $E$ ,  $\Delta\alpha$ ,  $\Delta T$ ,  $D_f$  and  $\nu$  represents Young's modulus, CTE mismatch, thermal load, TSV diameter and Poisson's ratio, respectively. The elastic mismatch between TSV and the matrix was neglected here for simplicity. The analytic solutions indicate that the steady-state ERR is proportional to the diameter of TSV, and scales with the square of the thermal load and the square of CTE mismatch. Comparing between Eq. 1 and 2, the steady-state ERR in the cooling process is ~35% higher than that in the heating process under the same thermal load. It implies that the TSV delamination is more likely to occur during the cooling processes. Figure 3 depicts the steady-state ERR for delamination of copper TSVs as a function of the TSV diameter and the thermal load.

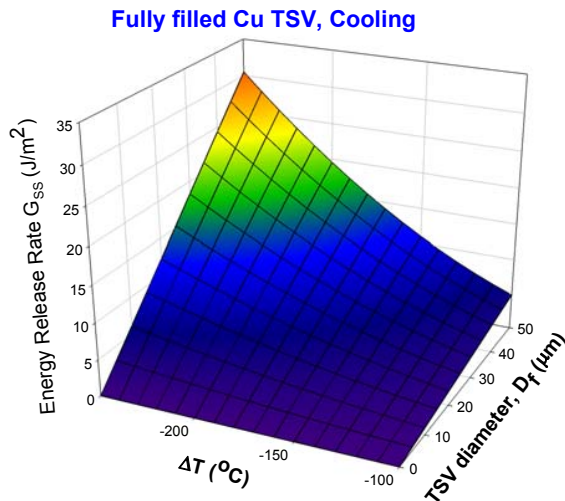


Figure 3. Crack driving force for TSV delamination under cooling.

The steady-state ERR solutions apply to a TSV structure for a long, circumferential crack with its crack tip away from the wafer surface. At the onset of spontaneous crack propagation, the ERR will be lower than the steady-state ERR. To illustrate this behavior, the non-steady state ERRs for short cracks with increasing crack length was calculated using FEA simulations. The results are superimposed to the steady-state solution under a thermal load of  $-250^\circ\text{C}$  (Figure 4).

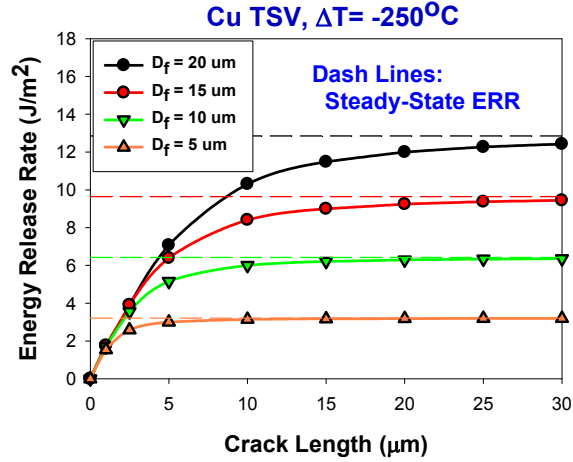


Figure 4. Energy release rate vs. crack length at circumference of Cu TSV for various TSV diameters. Dash lines indicate the steady-state ERR solution ( $\Delta T = -250^\circ\text{C}$ ).

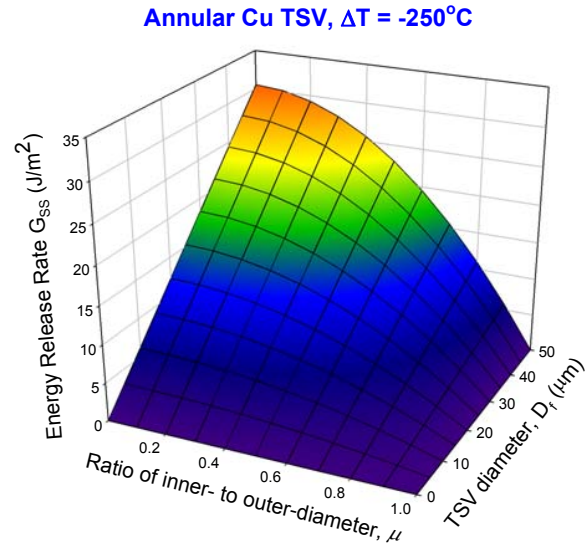


Figure 5. Plot of steady-state ERR, Eq. 3, as functions of  $\mu$  and the outer-diameter of TSV ( $\Delta T = -250^\circ\text{C}$ ).

Figure 4 shows a good agreement between the steady-state ERR solution and the FEA simulations at a long crack length  $> 2D_f$ . The figure also shows that the ERR increases with the crack length and TSV diameter, and can exceed  $10 \text{ J/m}^2$  for a TSV with  $20 \mu\text{m}$  diameter under a  $-250^\circ\text{C}$  of thermal load.

#### TSV Filling Structures: Annular and Lined TSVs

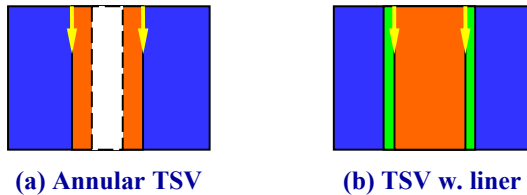
The steady-state solution for annular TSV delamination has been derived as well for the cooling conditions [6]. By

ignoring the elastic mismatch between TSV and the matrix for simplicity, the steady-state ERR,  $G_{ss}$ , can be expressed as

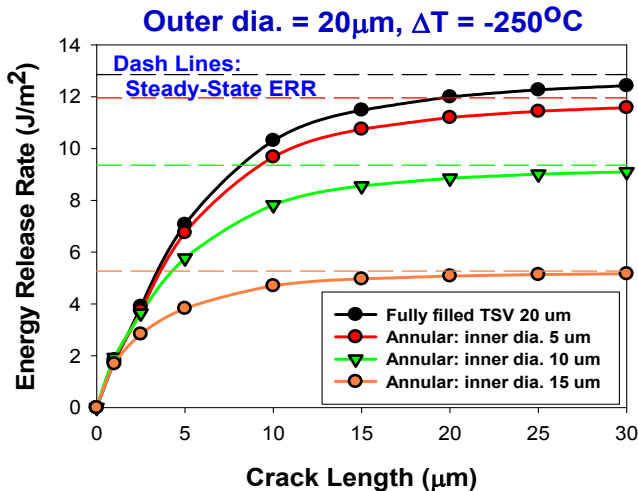
$$G_{ss} = \frac{E(\Delta\alpha\Delta T)^2 D_f}{4(1-\nu)} (1-\mu^2) \quad (3)$$

where  $\mu$  represents the ratio of the inner- to the outer-diameters of an annular TSV. Figure 5 depicts the steady-state ERR as a functions of the ratio  $\mu$  and the TSV diameter. According to Equation 3, ERR will decrease significantly with decreasing metal thickness in the annular TSV. For a very thin layer of metallization, delamination energy can reduce to nearly zero. This suggests that the driving force for TSV delamination can be effectively reduced using an annular structural design.

The steady-state ERR solution for annular structures was compared with FEA simulations. The cross-section of the annular TSV model used in the calculation is depicted in Figure 6a. The inner diameters of copper TSVs range from  $5\mu\text{m}$  to  $15\mu\text{m}$  while the outer diameter is fixed at  $20\mu\text{m}$ . The non-steady state ERR for copper TSV delamination was simulated for a  $-250^\circ\text{C}$  of thermal load. Figure 7 shows a good agreement between the steady-state solution and the FEA simulations for a long crack length. The results also indicate that the larger the inner diameter, the shorter the crack length to reach the steady-state.

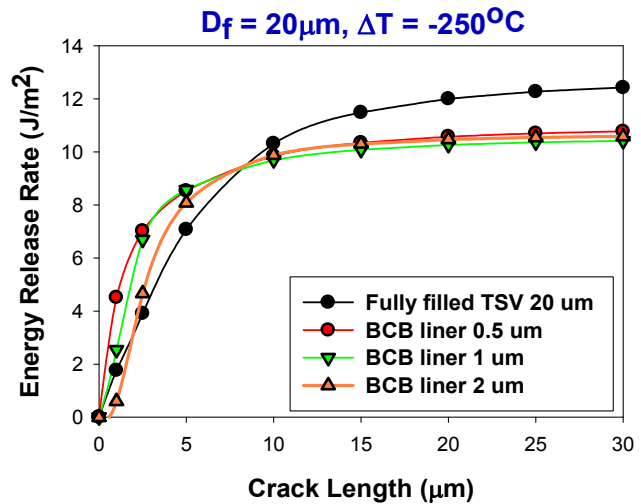


**Figure 6.** Cross-section of TSV structures considered in FEA simulations: (a) annular TSV and (b) TSV with liner. The yellow arrows indicate circumferential crack propagation from the wafer surface.

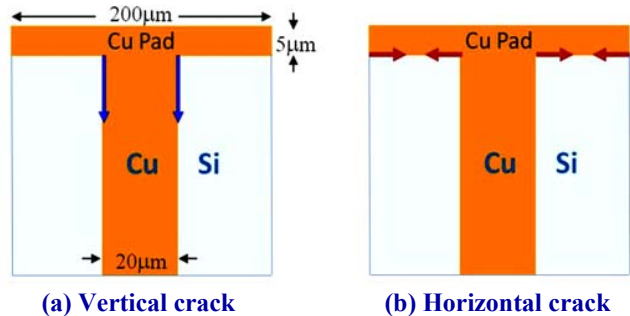


**Figure 7.** Simulated ERR for annular TSVs with various inner diameters and fixed outer diameter.

The effect of a compliant liner on the TSV delamination was also investigated. The cross-section of the lined TSV model used is depicted in Figure 6b. The liner is assumed to be BCB polymer. The thickness of the liner ranges from  $0.5\mu\text{m}$  to  $2\mu\text{m}$  while the inner diameter is fixed at  $20\mu\text{m}$ . Delamination is assumed to occur at the interface between the copper and the BCB liner. The crack driving force for three lined TSVs were simulated and compared with the fully filled copper TSV, as shown in Figure 8. At a crack length  $> 10\mu\text{m}$ , the ERRs among three lined structures are similar and all lower than the fully filled TSV. However, the ERRs of the lined TSVs can be higher than the fully filled TSV at a shorter crack length at below  $5\mu\text{m}$ . This can be attributed to a larger out-of-plane displacement in the BCB liner near the wafer surface. Although a soft polymer liner can reduce the thermal stress in the silicon matrix [3], it may influence the driving force for interfacial delamination in two ways: higher ERR than fully filled TSV for a shorter crack and lower ERR for a longer crack.



**Figure 8.** Comparison between BCB lined and fully filled TSVs for a fixed diameter of  $20\mu\text{m}$ .



**Figure 9.** Schematics of various interfacial crack geometries considered.

### TSV Delamination under Overlaying Metal Pad

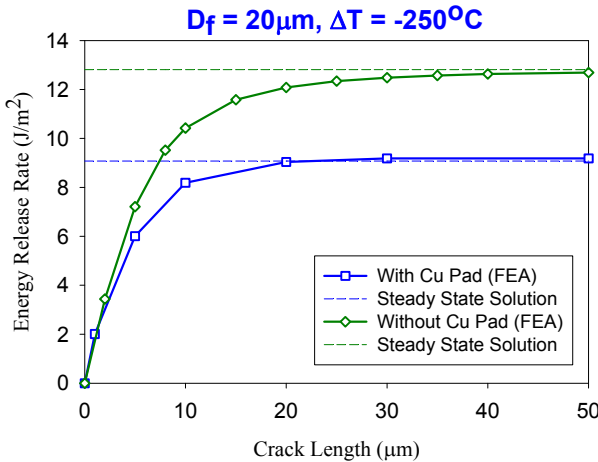
Simplified TSV structures have been discussed in the previous sections. The actual TSVs integrated in 3-D infrastructures are much more complicated. To add more complexity to the model, a TSV with a “nail head” was analyzed (Figure 9). The overlaying metal pad is required to

form electrical interconnects. The overlaying flange of metal pad is expected to constrain the crack propagation along the vertical interface, and thus reduce the ERR for TSV delamination.

The TSV delamination under an overlaying metal pad was previously examined [5, 6]. Consider a vertical, circumferential crack propagating downward underneath a rigid metal pad (Figure 9a). The delamination is mainly driven by a negative thermal load because the crack driving force generated by a positive thermal load was found to be one order of magnitude smaller. An analytic solution for the crack driving force under a negative thermal load has been derived [6]. The steady-state ERR,  $G_{ss}$ , can be expressed as follows:

$$G_{ss} = \frac{E_m(\Delta\alpha\Delta T)^2 D_f}{4} \left( \frac{(1+\nu_f)^3(1-2\nu_f)(1-\alpha_D^2) + (1+\nu_m)(1+\nu_f)^2(1+\alpha_D)^2}{((1+\nu_f)(1-2\nu_f)(1-\alpha_D) + (1+\nu_m)(1+\alpha_D))^2} \right) \quad (4)$$

where  $\alpha_D$  is the first Dundurs' parameter and the subscripts  $m$  and  $f$  stands for the matrix and the fiber, respectively. If the elastic mismatch between the TSV and the matrix is neglected, Equation 4 can be simplified to become Equation 2. FEA simulations were performed to validate the analytical solution. An axial-symmetric FEA model was built according to the geometry in Figure 9a, and the crack driving force was simulated as a function of the vertical crack length for a 20 $\mu\text{m}$  copper TSV under a -250 $^\circ\text{C}$  thermal load. The calculated ERR was plotted and compared with another 20 $\mu\text{m}$  copper TSV without the nail head, as shown in Figure 10. The results show a good agreement between the analytical solution and the FEA simulations for the steady state with a long crack length. An overlaying metal pad with the thickness of a quarter of TSV diameter is shown rigid enough to restrict the crack opening and to reduce the ERR for TSV delamination by ~30%.



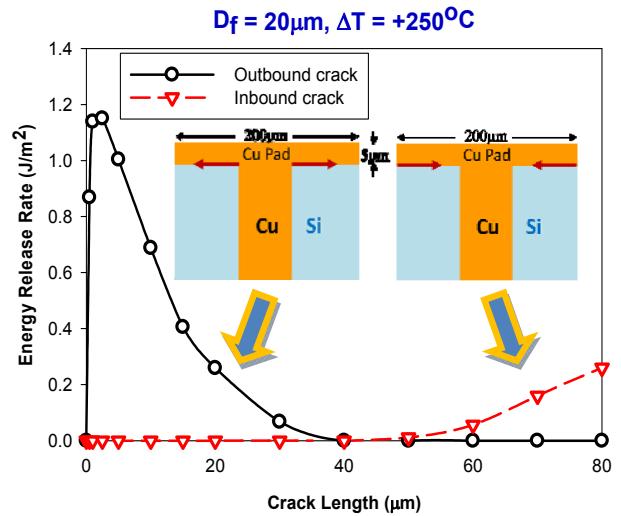
**Figure 10.** Effect of an overlaying Cu pad on ERR for delamination at the vertical interface ( $\Delta T = -250^\circ\text{C}$ ).

The overlaying metal pad can reduce the risk of TSV delamination, and the metallization process for TSVs can be engineered accordingly. For instance, an overburden of copper layer always comes with the electroplating process and

has to be removed using a chemical-mechanical polishing (CMP) process after annealing. The copper overburden is rigid and can keep the TSV/matrix interfaces from delaminating. If the overburden is fully removed, the ERR for TSV delamination will increase by ~35% as mentioned earlier. Without the protection of the overlaying copper film, such TSV structure needs to go through another thermal process to form the metal contact on top, which can further increase the risk of delamination. Therefore, a metallization process without fully depleting the copper overburden is expected to mitigate the type of TSV delamination along the axial direction as discussed here.

Another type of TSV delamination can occur with the crack propagating horizontally at the interface between the silicon top surface and the flange part of the nail head (Figure 9b). Such delamination is mainly driven by a positive thermal load. Under a positive thermal load, the TSV tends to extrude out of the silicon matrix due to the larger thermal expansion of copper, resulting in a peeling stress at the horizontal interface. The peeling stress can drive crack propagation from the inner- to the outer-portion of the flange.

Based on the geometry in Figure 9b, two axial-symmetric FEA models were built to evaluate the crack driving force for horizontal cracks under a +250 $^\circ\text{C}$  of thermal load. FEA simulations were performed separately for both the outward and the inward circumferential cracks, and the results are shown in Figure 11. For the outward crack, the ERR reaches a maximum at ~2 $\mu\text{m}$  away from the edge of the TSV. As the crack tip extends away from the edge of the TSV, the crack driving force gradually decreases to zero. On the other hand, the ERR for the inward crack generally increases as the crack tip approaches the edge of the TSV. According to our simulations, the ERR for the horizontal cracks under heating is much smaller than the vertical crack under cooling. The result suggests that the delamination is more likely to initiate from the vertical interface during thermal cycling.

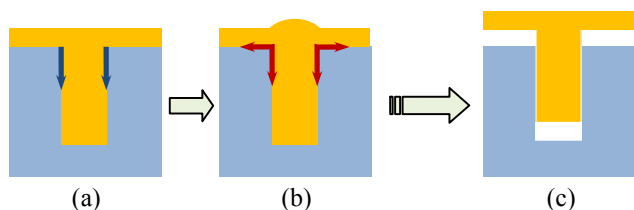


**Figure 11.** ERR for outbound and inbound crack along the Cu flange/Si interface ( $\Delta T = +250^\circ\text{C}$ ).

Both the horizontal and the vertical interfaces will have to be damaged for the “nail-head” TSV to pop up. A possible



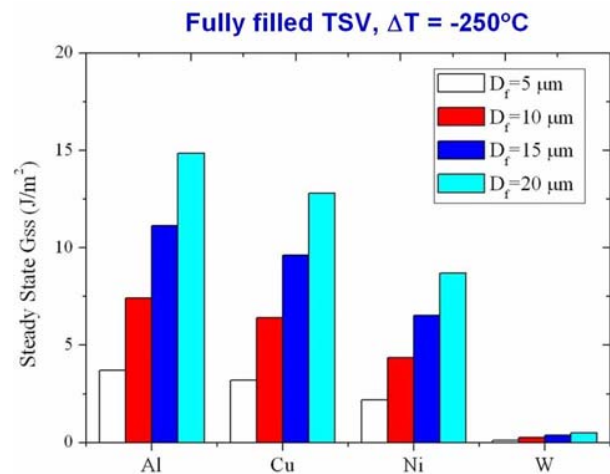
mechanism is as follows. First, the vertical interface between the TSV and the silicon matrix is debonded during temperature cycles. Once the vertical interface is debonded, the copper via is easier to stick out of the wafer upon heating, resulting in an increased crack driving force on the horizontal interface. After repeated thermal cycles, both interfaces can be sufficiently delaminated to induce the TSV pop-up from the wafer. This process is illustrated in Figure 12.



**Figure 12.** Illustration of TSV pop-up process: (a) Vertical interface debonding under cooling, (b) Horizontal interface debonding under heating, (c) TSV pop-up after repeated thermal cycles.

### Effect of TSV Metallization on Delamination

Current TSVs in the 3-D infrastructure are fabricated with various metals, such as copper, tungsten, and nickel. The difference in thermo-mechanical reliability among these materials is of interest. Based on the steady-state ERR equations, a metal with a low modulus and a low CTE is favored for reducing the driving force for delamination. Unfortunately, a metal with low modulus usually comes with a high CTE, and vice versa. The thermo-mechanical properties of four commonly used metals are listed in Table 1, in which aluminum has the smallest modulus while tungsten has the smallest CTE. To compare these four materials, the ERRs for TSV delamination have been calculated for the same thermal load, and the results are plotted in Figure 13.



**Figure 13.** Steady-state ERR: TSVs filled with four kinds of metals.

Figure 13 indicates that the driving force for TSV delamination significantly decreases with reduced CTE of the metal. This can be attributed to the fact that ERR is proportional to the square of the CTE mismatch between the metal and the silicon matrix. Given the same thermal load and TSV dimension, tungsten, which has the lowest CTE among the four materials, exhibits the least ERR for delamination. However, the tendency to delamination cannot be judged by

the crack driving force alone. The interfacial adhesion between the metallization material and the barrier layer of TSVs also play an important role in controlling the delamination. In this case, copper material can develop more plastic deformation compared with tungsten. Therefore, copper can absorb energy by plastic deformation near the crack tip and increase the fracture resistance to crack propagation. This interesting and important aspect of fracture characteristics for TSV will be further investigated.

**Table 1.** Thermo-mechanical properties of Al, Cu, Ni, W, and Si.

Material	CTE (ppm/°C)	Young's Modulus (GPa)	Poisson's Ratio
Al	20	70	0.35
Cu	17	110	0.35
Ni	13	207	0.31
W	4.4	400	0.28
Si	2.3	130	0.28

### Summary

The characteristics of thermal stress-induced TSV delamination were investigated using analytic solutions and FEA simulations. The driving force for TSV delamination was found to be different depending on whether a positive or a negative thermal load. Under a positive thermal load, the fracture mode was primarily a shear mode (mode II) delamination. On the other hand, the fracture mode under a negative thermal load was a mixture of peeling (mode I) and shear (mode II). Based on the analytic solutions, the driving force for TSV delamination can be reduced by scaling down the diameter of TSVs and by using lower CTE metals. TSVs with various filling structures were compared. Annular structure exhibited lower ERRs than the fully filled TSV structure, and an overlaying metal pad can constrain the crack opening and thus reduce the ERR for delamination along the axial direction. The effect of metallization on TSV delamination was investigated using four materials: aluminum, copper, nickel and tungsten. Tungsten exhibited the least ERR due to the smallest CTE mismatch with the silicon substrate. Nevertheless, the thermo-mechanical reliability of TSV structures also depends on other factors such as processing temperature, interfacial adhesion, and the plasticity of the materials. These effects will be further investigated.

### Acknowledgments

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