AIP Conference Proceedings

Thermal Stresses Analysis of 3D Interconnect

Kuan H. Lu, Xuefeng Zhang, SukKyu Ryu, Rui Huang, and Paul S. Ho

Citation: AIP Conf. Proc. **1143**, 224 (2009); doi: 10.1063/1.3169263
View online: http://dx.doi.org/10.1063/1.3169263
View Table of Contents: http://proceedings.aip.org/dbt/dbt.jsp?KEY=APCPCS&Volume=1143&Issue=1
Published by the American Institute of Physics.

Related Articles

Strain-compensation measurement and simulation of InGaAs/GaAsP multiple quantum wells by metal organic vapor phase epitaxy using wafer-curvature
J. Appl. Phys. 110, 113501 (2011)

Temperature stability of the pentacene thin-film phase
Appl. Phys. Lett. 99, 221911 (2011)

Ab-initio aprroach to the electronic, structural, elastic, and finite-temperature thermodynamic properties of Ti2AX (A=Al or Ga and X=C or N)
J. Appl. Phys. 110, 093504 (2011)

Micro-scale measurement and modeling of stress in silicon surrounding a tungsten-filled through-silicon via
J. Appl. Phys. 110, 073517 (2011)

Thermal expansions in wurtzite AlN, GaN, and InN: First-principle phonon calculations
J. Appl. Phys. 110, 043528 (2011)

Additional information on AIP Conf. Proc.

Journal Homepage: http://proceedings.aip.org/
Journal Information: http://proceedings.aip.org/about/about_the_proceedings
Top downloads: http://proceedings.aip.org/dbt/most_downloaded.jsp?KEY=APCPCS
Information for Authors: http://proceedings.aip.org/authors/information_for_authors

ADVERTISEMENT

Submit Now

Explore AIP's new open-access journal

- Article-level metrics now available
- Join the conversation! Rate & comment on articles

Downloaded 19 Dec 2011 to 146.6.102.108. Redistribution subject to AIP license or copyright; see http://proceedings.aip.org/about/rights_permissions

Thermal Stresses Analysis of 3-D Interconnect

Kuan H. Lu[a], Xuefeng Zhang[a], Suk-Kyu Ryu[b], Rui Huang[b], Paul S. Ho[a]

[a] *Microelectronics Research Center, the University of Texas at Austin, Austin, TX 78758*
[b] *Department of Aerospace Engineering and Engineering Mechanics, the University of Texas, Austin, TX 78712*

Abstract. In 3-D interconnect structures, process-induced thermal stresses around through silicon vias (TSVs) raise serious reliability issues such as silicon cracking and performance degradation of devices. In this study, the thermo-mechanical reliability of 3-D interconnect was investigated using finite element analysis (FEA) combined with analytical methods. The thermal stress in silicon was found to decrease as a function of distance from an isolated TSV but increase with the TSV diameter. Additional simulation results demonstrated that hybrid TSV structures can significantly reduce thermal stresses. An analytical solution was introduced to deduce the stress distribution around an isolated TSV, which was applied to deduce the stress interaction in TSV arrays based on linear superposition of the analytical solution. The stress interaction is directional dependent, thus the TSV array configuration can be optimized to improve the keep-away-zone design for stress-sensitive devices.

Keywords: Thermal stress; 3-D integration; 3-D interconnect; Through Silicon Via.
PACS: 65.40.De

INTRODUCTION

The 3-D interconnects (wafer-to-wafer, die-to-wafer, and die-to-die) are being developed to meet the ITRS scaling requirements of global wiring. Through silicon via (TSV) technology is an important enabling technology for 3-D integration. However, the incorporation of TSV raises significant challenges to the thermo-mechanical reliability of the 3-D interconnects, especially for copper TSV, which has a thermal expansion coefficient (CTE) 6~7 times that of silicon. Thermal stresses generated during manufacturing process can impact the performance of stress-sensitive devices [1] as well as initiate cracks to fail 3-D interconnects [2]. The mixed-signal chips contain various stress-sensitive components with distinctive characteristics for analog and digital circuits. The stress impact on the performance and reliability of the mixed-signal chip is not well understood. A better understanding of such thermo-mechanical issues is essential to ensure successful development of 3-D interconnects.

Various approaches have been applied in the past to address these reliability issues. For example, FEA was performed to determine the stresses developed during the manufacturing process [3,4], and various via filling designs [5,6] were proposed to minimize the thermal stresses generated by the TSVs. In this study, we calculate first the thermal stress characteristics of single TSV for various structural configurations. These include: a. full copper filling, b. annular copper filling, and c. full copper filling with a polymer liner between copper and silicon. FEA simulation is used to characterize the stress distribution around an isolated copper TSV embedded in silicon matrix. The mechanical properties of copper required for FEA modeling such as the elastic modulus and yield stress were obtained experimentally using a bending beam technique [7]. To extend the thermal stress analysis, a 2-D plane-strain solution [8] is introduced to evaluate the stress distribution around an isolated TSV. Then the solution is used as a base in a linear superposition to evaluate the stress interaction in TSV arrays. This enables us to examine the constructive/destructive stress interaction between TSVs and to develop a basic

CP1143, *Stress-Induced Phenomena in Metallization: 10th International Workshop,* edited by P. S. Ho, S. Ogawa, and E. Zschech
© 2009 American Institute of Physics 978-0-7354-0680-3/09/$25.00

Downloaded 19 Dec 2011 to 146.6.102.108. Redistribution subject to AIP license or copyright; see http://proceedings.aip.org/about/rights_permissions

approach to optimize the TSV array configuration with improved thermo-mechanical reliability for 3-D interconnects.

Material Characterization and Model Verification

The material properties of copper TSV were characterized by bending beam experiments combined with finite element modeling. The biaxial stress of a copper film on a silicon substrate was first measured by the bending beam technique under thermal cycling, and the experimental data were fitted using a bi-linear FEA model to extract the properties of the copper film. The bending beam samples were prepared by electroplating a thin copper film on a silicon wafer, and then diced into 5mm x 40mm test slices. During bending beam experiments, samples were thermal cycled between 30ºC and 300ºC in a vacuum chamber. Due to thermal mismatch between the copper film and the silicon substrate, the sample will bend under thermal loading, as depicted in Figure 1. By monitoring the sample curvature using laser beams, the biaxial stress of the thin copper film can be calculated by the Stoney's equation [7]:

$$\sigma = \frac{E_s t_s^2}{6(1-\nu_s)t_f}\left(\frac{1}{R}-\frac{1}{R_o}\right) \qquad (1)$$

where σ is the film stress, ν is the Poisson's ratio, $E_s/(1-\nu_s)$ is the biaxial modulus of the substrate, t is the thickness, R is the sample curvature and R_0 is the initial curvature. The subscripts s and f denote the substrate and the film, respectively. Typical thermal stress of copper film obtained is shown in figure 2.

A FEA model was set up for the material characterization, where the model has the same geometry and thermal history as the test sample. A bi-linear strain-hardening plastic model was used to simulate copper behavior during thermal cycling. The temperature dependent elastic modulus and the yield stress of the copper film were derived by an iteration scheme as shown in Figure 2 until the experimental curve is in agreement with the simulation result. The calculated film stress is plotted as the red line in figure 2.

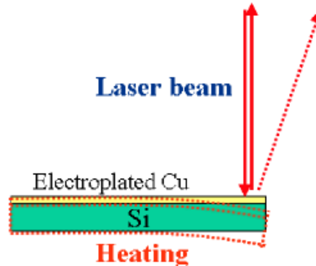

FIGURE 1. Bending beam thermal stress measurement

Downloaded 19 Dec 2011 to 146.6.102.108. Redistribution subject to AIP license or copyright; see http://proceedings.aip.org/about/rights_permissions

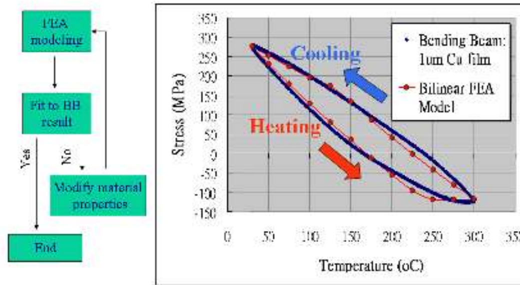

FIGURE 2. Material characterization by bending beam experiment

Thermo-Mechanical Simulation by Finite Element Analysis (FEA)

The properties of the Cu film were used as inputs for finite element analysis to study the thermo-mechanical reliability of TSV structures. Figure 3 shows a rotationally symmetric model representing an isolated TSV in a silicon substrate. An element birth and death technique was applied in the FEA to calculate process induced thermal stresses in the silicon matrix. Table 1 lists the simplified process steps for the FEA simulation:

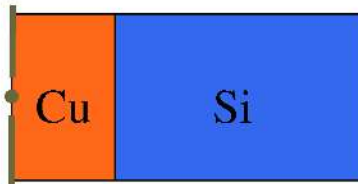

FIGURE 3. TSV model with rotational symmetry

TABLE 1. Simplified process steps for FEA simulation

Process Step	Description	Temperature (oC)
1	TEOS deposition	400
2	Ti barrier layer deposition	375
3	Cu electroplating	25
4	Annealing	200
5	Cooling	25

Three TSV structures were investigated using this approach. Here we first describe the thermal stress distribution of fully filled copper TSVs. Figure 4 shows the radial stress on silicon surface induced by fully filled TSVs of three via radii. In general, the thermal stress in silicon decreases as a function of distance from the TSV but increases with the TSV radius, therefore, down scaling of the via size can reduce the processes induced thermal stress. Then we compared the thermal stresses for three different TSV structures, including fully filled TSVs, partially filled TSVs, and TSVs with hybrid filling materials. As shown in Figure 5, for TSVs with the same radius the thermal stress in silicon is reduced for the annular structure and the effect increases with a thinner copper filling. For the hybrid TSV structure, when a layer of soft material such as Benzocyclobutene (BCB) is inserted between the copper and the

Downloaded 19 Dec 2011 to 146.6.102.108. Redistribution subject to AIP license or copyright; see http://proceedings.aip.org/about/rights_permissions

silicon matrix, the buffer layer can significantly lower the stress level. The result is also shown in Figure 5. In combination, the simulation results suggest that the material combination of TSV filling can be optimized to improve the thermo-mechanical reliability.

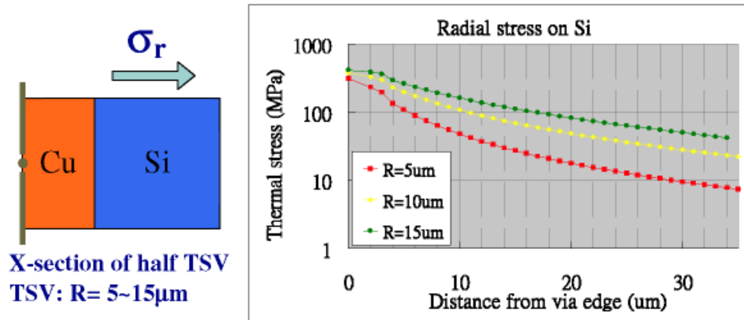

FIGURE 4. Thermal stress of TSVs with various radii

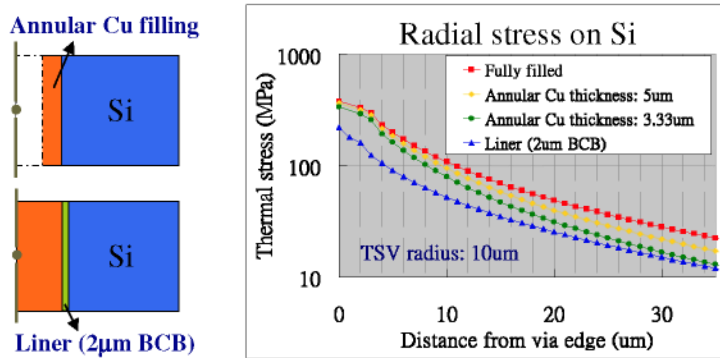

FIGURE 5. Thermal stress of TSVs with various structures

Thermal Stress Solution (Plane Strain Approximation)

Here an analytical solution known as the Lamé stress solution [8] is introduced to evaluate the thermal stresses around an isolated TSV. Consider an infinite long TSV embedded in an infinite matrix, the stress field in the matrix induced by a differential thermal load can be expressed as:

$$\sigma^m{}_r = -\sigma^m{}_\theta = -\frac{B\Delta\alpha\Delta T}{2}\left(\frac{R}{r}\right)^2 \qquad (2)$$
$$\sigma^m{}_z = \sigma^m{}_{rz} = \sigma^m{}_{\theta z} = 0$$

where the superscript m, B, $\Delta\alpha$, ΔT, R, and r signify the matrix, biaxial modulus, mismatch of coefficients of thermal expansion (CTEs), differential thermal load, radius of TSV, and the distance away from the

Downloaded 19 Dec 2011 to 146.6.102.108. Redistribution subject to AIP license or copyright; see http://proceedings.aip.org/about/rights_permissions

center of TSV, respectively. The elastic mismatch between TSV and the matrix is neglected for simplicity. The analytical solution clearly shows the radial dependence of the thermal stresses around an isolated TSV where the thermal stress increases with the square of the TSV radius but decreases with the square of the distance away from the TSV. This stress behavior can be shown readily by plotting the stress distributions around three fully filled TSVs as a function of the normalized distance, r/R. As shown in Figure 6, the stress distributions merge to become an universal curve with a slope of -2 in a logarithmic plot, as expected from the analytical solution. The result shows a good agreement between the 3-D FEA simulation and the 2-D plane-strain approximation.

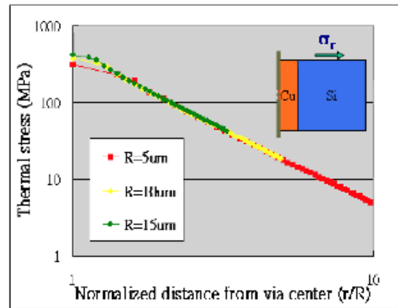

FIGURE 6. Thermal stress of fully filled TSVs

In a cylindrical coordinate system, the thermal stress distribution around an isolated TSV is axial symmetric. Nevertheless, microelectronic devices are commonly manufactured in rectangular configurations, where the thermal stress distribution in a Cartesian coordinate system is not axial symmetric. Figure 7 shows the stress distribution around an isolated TSV calculated from the 2-D stress solution under a thermal load of -175°C. In a Cartesian coordinate system, tensile and compressive stresses concentrate along perpendicular directions around a copper TSV. The results suggest that the keep-away-zone for stress sensitive devices should be of two-fold rotational symmetry around TSVs.

The stress interaction between adjacent TSVs can be obtained using a linear superposition of the analytical solution. Figure 8 shows the stress interaction between two TSVs, where stresses can be intensified or suppressed as a result of the elastic interaction between TSVs.

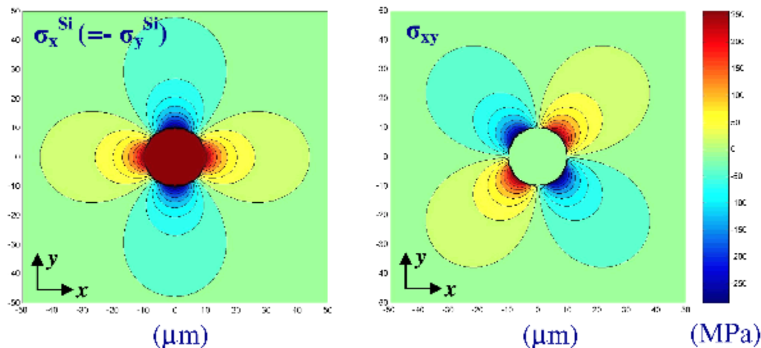

FIGURE 7. Analytical stress solution of an isolated TSV

Downloaded 19 Dec 2011 to 146.6.102.108. Redistribution subject to AIP license or copyright; see http://proceedings.aip.org/about/rights_permissions

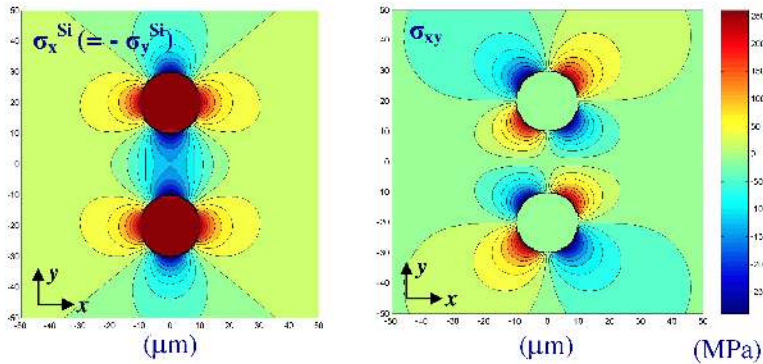

FIGURE 8. Stress interaction between two TSVs

Figure 9 shows the stress distribution in two 2x2 rectangular TSV arrays. In a Cartesian coordinate system, the normal stresses (σ_x and σ_y) are intensified between neighboring TSVs if the array is aligned in the configuration as shown in Figure 9(a). By rotating the TSV array by 45 degrees, the normal stresses become suppressed between neighboring TSVs, as shown in Figure 9(b). In this way, there is more area with larger σ_x in Figure 9(a) than in Figure 9(b), although the net stress intensity remains the same after array rotation. Given that piezoresistance coefficients of silicon are highly anisotropic depending on the stress orientation [1], rearranging TSV array direction or configuration can be used to optimize the keep-away-zone design for stress sensitive devices. For instance, if the MOS devices can properly function within 100 MPa of normal stresses but not sensitive to shear stresses, the TSV array configuration in Figure 9(b) yields a smaller keep-away-zone compared to the configuration in Figure 9(a). The keep-away-zone is marked by blue rectangles and the channel direction of the MOS device is indicated in both figures.

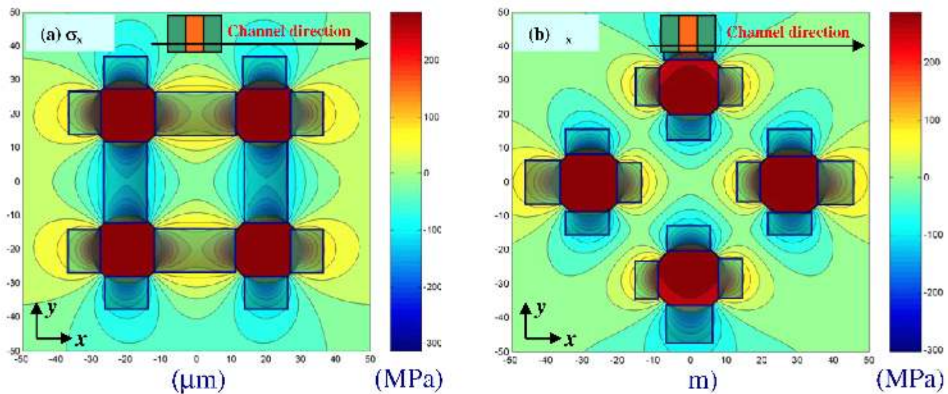

FIGURE 9. Stress interaction in 2x2 rectangular TSV arrays

Downloaded 19 Dec 2011 to 146.6.102.108. Redistribution subject to AIP license or copyright; see http://proceedings.aip.org/about/rights_permissions

SUMMARY

In summary, FEA modeling was used to evaluate process induced stresses of 3-D TSV structures. The distance-to-diameter ratio was identified as an important parameter to determine the thermal stress level near an isolated TSV. Significant stress reduction can be achieved by introducing hybrid TSV structures. An analytical solution was developed to deduce the stress field around an isolated TSV, which was used to evaluate the interaction of thermal stresses obtained by linear superposition of stress solutions. The stress interaction is directional dependent, thus the area of keep-away-zone can be optimized by rearranging TSV array configurations.

REFERENCES

1. S. Thompson *et al.*, "Uniaxial-Process-Induced Strained-Si: Extending the CMOS Roadmap," *IEEE Trans. Electron Devices*, Vol. 53, No. 5, May 2006.
2. S. Savastiouk, Semetech 3D ICs Workshop, San Diego, CA, Sept. 2008.
3. B. Wunderle *et al.*, "Thermo-Mechanical Reliability of 3D-Integrated Microstructures in Stacked Silicon," *Mater. Res. Soc. Symp. Proc.*, Vol. 970, 2007.
4. C. Okoro *et al.*, "Analysis of the Induced Stresses in Silicon During Thermcompression Cu-Cu Bonding of Cu-Through-Vias in 3D-SIC Architecture," *Proc 57th Electronic Components and Technology Conf*, 2007.
5. C. K. Tsang *et al.*, "CMOS-Compatible Through Silicon Vias for 3D Process Integration," *Mater. Res. Soc. Symp. Proc.*, Vol. 970, 2007.
6. M. Bonkohara *et al.*, "Current and Future Three-Dimensional LSI Integration Technology by "Chip on Chip","Chip on Wafer" and "Wafer on Wafer"," *Mater. Res. Soc. Symp. Proc.*, Vol. 970, 2007.
7. J. Zhao *et al.*, " On-wafer characterization of thermomechanical properties of dielectric thin films by a bending beam technique," *J. Appl. Phys.*, Vol 88, No.5, Sept. 2000.
8. T. C. Lu, *et al.*, "Matrix Cracking in Intermetallic Composites Caused by Thermal Expansion Mismatch," *Acta Metall. Mater.*, Vol. 39, No. 8, 1991.

Downloaded 19 Dec 2011 to 146.6.102.108. Redistribution subject to AIP license or copyright; see http://proceedings.aip.org/about/rights_permissions